

MOS FIELD EFFECT TRANSISTOR μ PA2717AGR

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA2717AGR is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Lithium-Ion battery protection circuit.

FEATURES

• Low on-state resistance

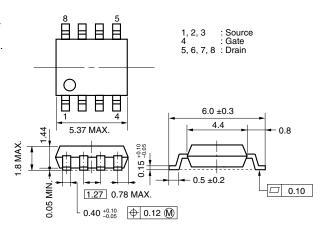
 $R_{DS(on)1}$ = 5.5 m Ω MAX. (VGS = -10 V, ID = -7.5 A) $R_{DS(on)2}$ = 8.9 m Ω MAX. (VGS = -4.5 V, ID = -7.5 A)

• Low input capacitance

Ciss = 3550 pF TYP.

- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

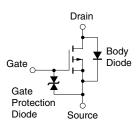
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Ves = 0 V)	VDSS	-30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC)	I _{D(DC)}	∓15	Α
Drain Current (pulse) Note1	I _{D(pulse)}	∓150	Α
Total Power Dissipation Note2	P _{T1}	2	W
Total Power Dissipation Note3	P _{T2}	2	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note4	las	-15	Α
Single Avalanche Energy Note4	Eas	22.5	mJ

EQUIVALENT CIRCUIT



- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 2. Mounted on ceramic substrate of 1200 mm² x 2.2 mm
 - 3. Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm, PW = 10 sec
 - **4.** Starting T_{ch} = 25°C, V_{DD} = -15 V, R_G = 25 Ω , L = 100 μ H, V_{GS} = $-20 \rightarrow 0$ V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

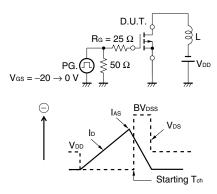
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ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

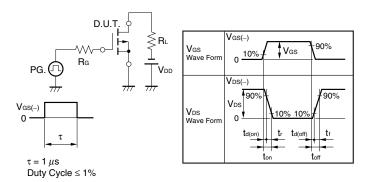
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	loss	V _{DS} = -30 V, V _{GS} = 0 V			-1	μΑ
Gate Leakage Current	Igss	V _{GS} = ∓20 V, V _{DS} = 0 V			∓10	μΑ
Gate to Source Cut-off Voltage	V _{GS(off)}	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-1.0		-2.5	V
Forward Transfer Admittance Note	yfs	$V_{DS} = -10 \text{ V}, I_{D} = -7.5 \text{ A}$	13			S
Drain to Source On-state Resistance Note	RDS(on)1	$V_{GS} = -10 \text{ V}, I_D = -7.5 \text{ A}$		4.7	5.5	mΩ
	RDS(on)2	V _{GS} = -4.5 V, I _D = -7.5 A		6.1	8.9	mΩ
	RDS(on)3	V _{GS} = -4.0 V, I _D = -7.5 A		6.9	10.4	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V		3550		pF
Output Capacitance	Coss	V _{GS} = 0 V		1260		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		600		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = -15 V, I _D = -7.5 A		17		ns
Rise Time	tr	V _{GS} = -10 V		32		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		920		ns
Fall Time	tf			510		ns
Total Gate Charge	Q _G	V _{DD} = -24 V		130		nC
Gate to Source Charge	Qgs	V _{GS} = -10 V		11		nC
Gate to Drain Charge	Q _{GD}	I _D = -15 A		36		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 15 A, V _{GS} = 0 V		0.82		V
Reverse Recovery Time	trr	I _F = 15 A, V _{GS} = 0 V		500		ns
Reverse Recovery Charge	Qrr	di/dt = 50 A/μs	_	1320	_	nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T. & \\ \hline \\ I_G = -2 \text{ mA} \\ \hline \\ PG. & \\ \hline \\ \end{array} \begin{array}{c} S_{RL} \\ \hline \\ \end{array}$$

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Data Sheet G19279EJ1V0DS

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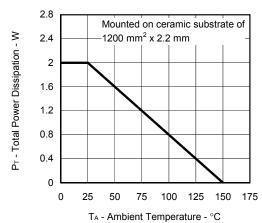
0 25

TYPICAL CHARACTERISTICS (TA = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA 120 dT - Percentage of Rated Power - % 100 80 60 40 20

50

TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



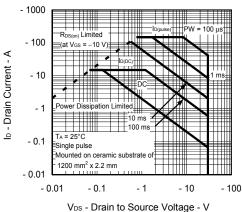
FORWARD BIAS SAFE OPERATING AREA

T_A - Ambient Temperature - °C

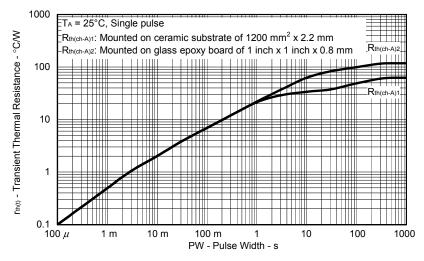
75

100 125

150



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

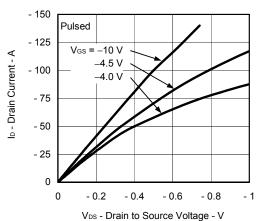


Data Sheet G19279EJ1V0DS

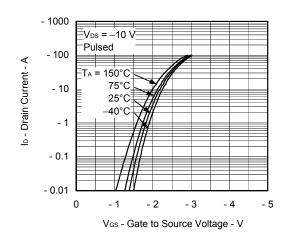
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DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

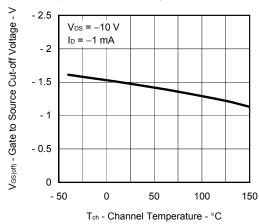
NEC



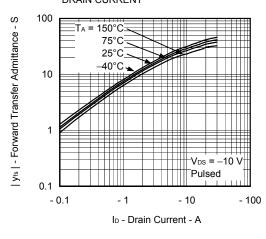
FORWARD TRANSFER CHARACTERISTICS



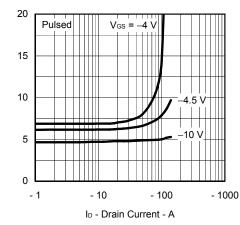
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



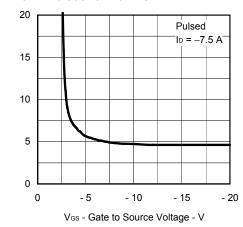
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

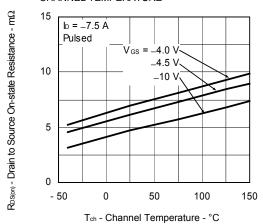


R_{DS(m)} - Drain to Source On-state Resistance - mΩ

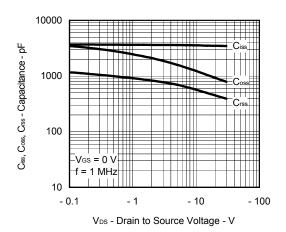
4 Data Sheet G19279EJ1V0DS

Ros(ση) - Drain to Source On-state Resistance - mΩ

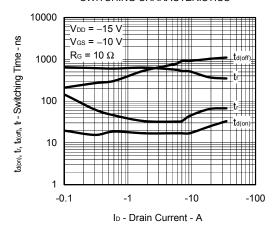
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



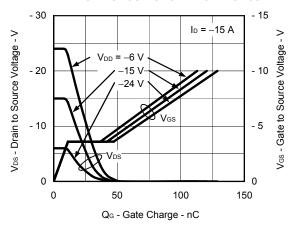
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



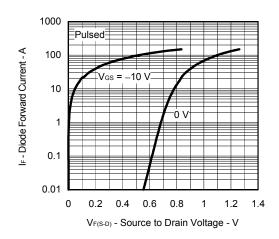
SWITCHING CHARACTERISTICS



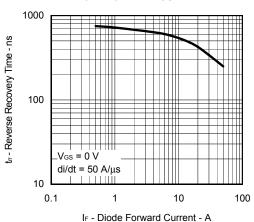
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



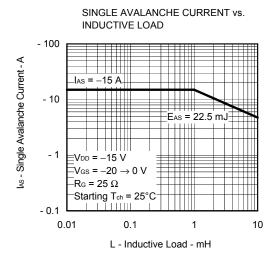
SOURCE TO DRAIN DIODE FORWARD VOLTAGE

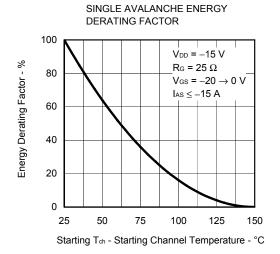


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μPA2717AGR-E1-AT Note			Power SOP8
μPA2717AGR-E2-AT Note	Pure Sn (Tin)	Tape 2500 p/reel	0.08 g TYP.

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

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