DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR
μPA2720AGR

SWITCHING
N-CHANNEL POWER MOSFET

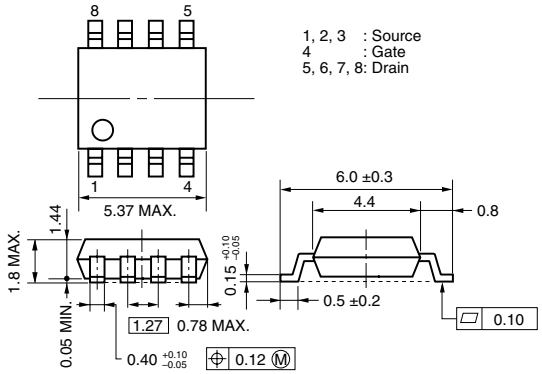
DESCRIPTION

The μPA2720AGR is N-channel MOS Field Effect Transistor designed for power management applications of a notebook computer and Lithium-Ion battery protection circuit.

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 6.6 mΩ MAX. (V_{GS} = 10 V, I_D = 7 A)
  $R_{DS(on)2}$ = 14 mΩ MAX. (V_{GS} = 5.0 V, I_D = 7 A)
- Low input capacitance
  C_{iss} = 3600 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)
- RoHS Compliant

PACKAGE DRAWING (Unit: mm)



ORDERING INFORMATION

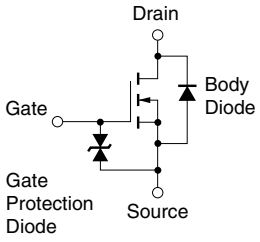
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μPA2720AGR-E1-AT Note	Pure Sn	Tape 2500 p/reel	Power SOP8 0.08 g TYP.
μPA2720AGR-E2-AT Note			

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±14	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±150	A
Total Power Dissipation Note2	P_{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) Note2	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Single Avalanche Current Note3	I_{AS}	14	A
Single Avalanche Energy Note3	E_{AS}	19.6	mJ

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt

3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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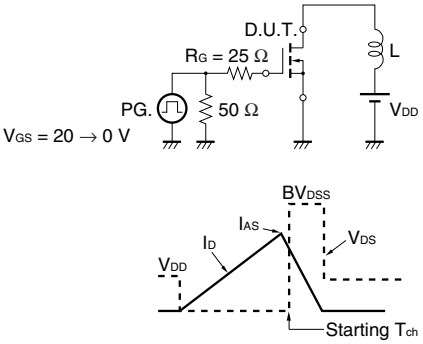
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

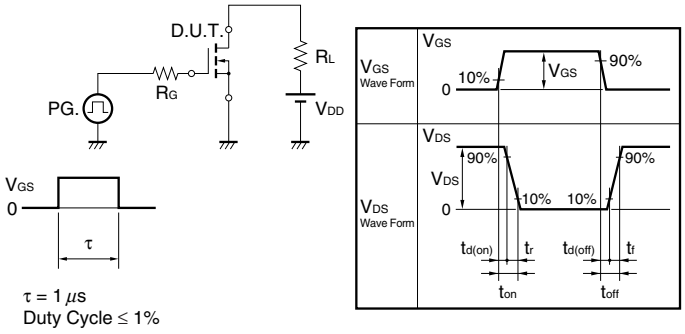
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5		3.0	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 7 A	7			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 7 A		5.5	6.6	mΩ
	$R_{DS(on)2}$	V_{GS} = 5.0 V, I_D = 7 A		7.0	14	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V,		3600		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		490		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		250		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 7 A,		22		ns
Rise Time	t_r	V_{GS} = 10 V,		22		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		73		ns
Fall Time	t_f			17		ns
Total Gate Charge	Q_G	V_{DD} = 15 V,		28		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 5 V,		10		nC
Gate to Drain Charge	Q_{GD}	I_D = 14 A		11		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 14 A, V_{GS} = 0 V		0.8		V
Reverse Recovery Time	t_{rr}	I_F = 14 A, V_{GS} = 0 V,		31		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		25		nC

Note Pulsed

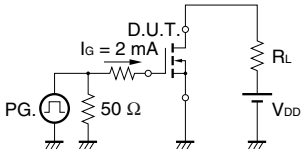
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

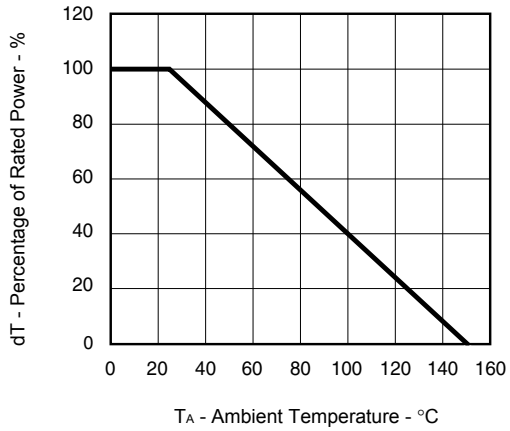


TEST CIRCUIT 3 GATE CHARGE

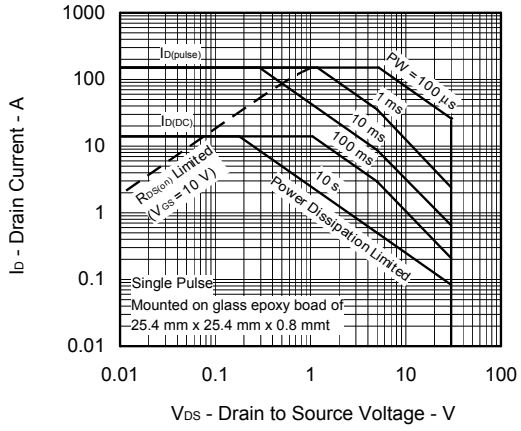


TYPICAL CHARACTERISTICS (T_A = 25°C)

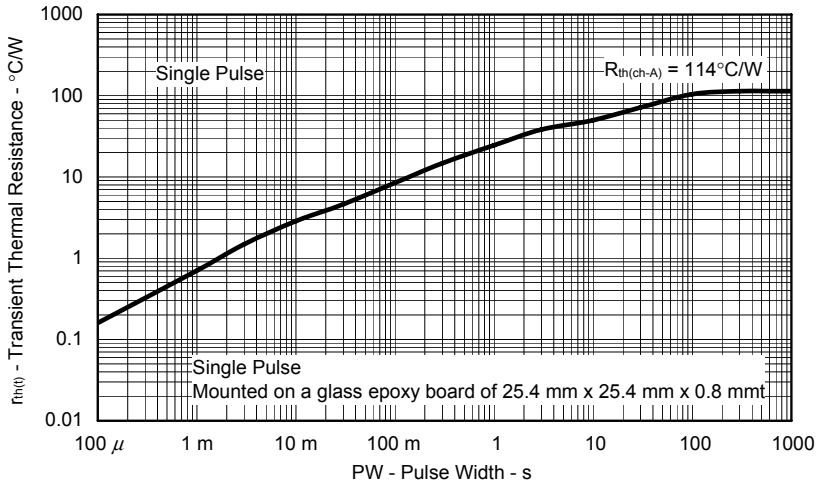
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



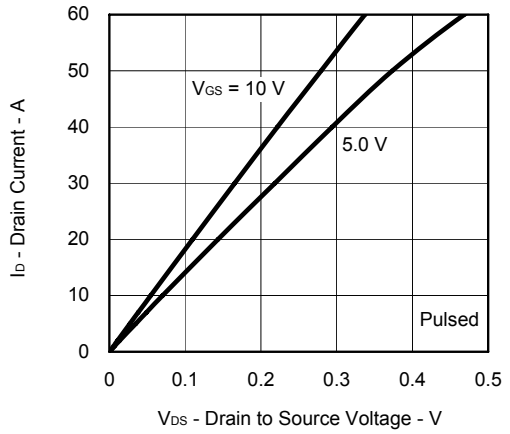
<R> FORWARD BIAS SAFE OPERATING AREA



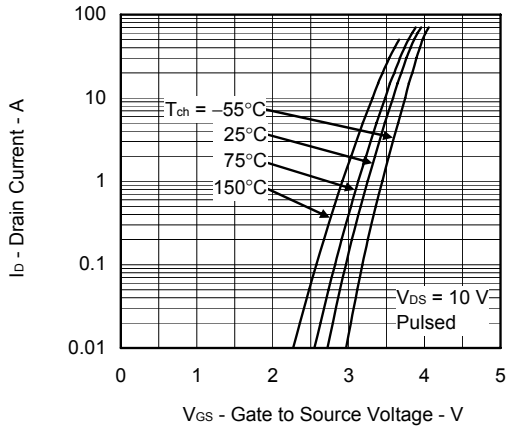
<R> TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



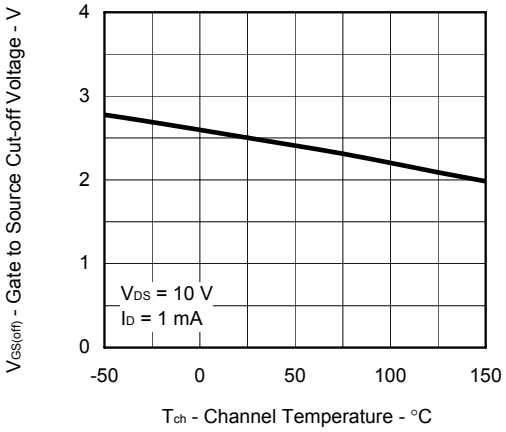
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



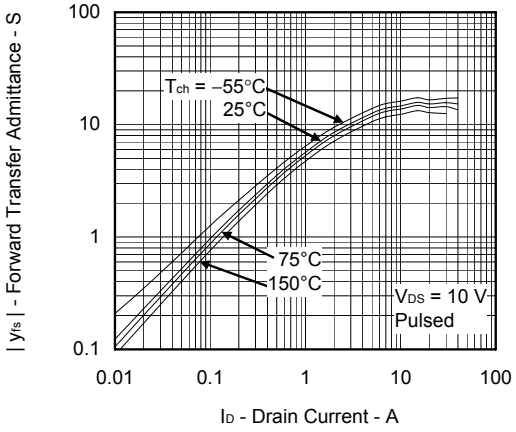
FORWARD TRANSFER CHARACTERISTICS



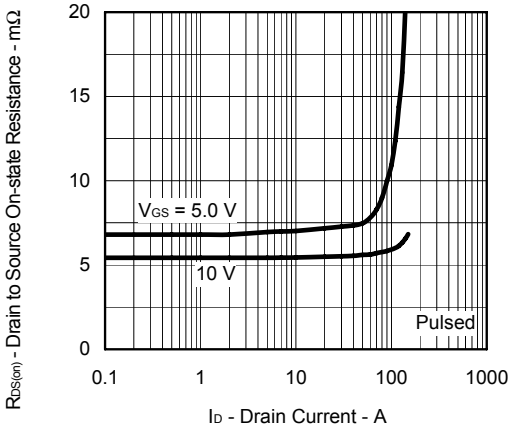
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



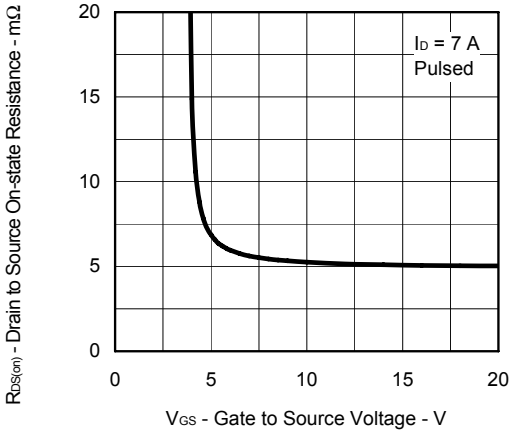
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



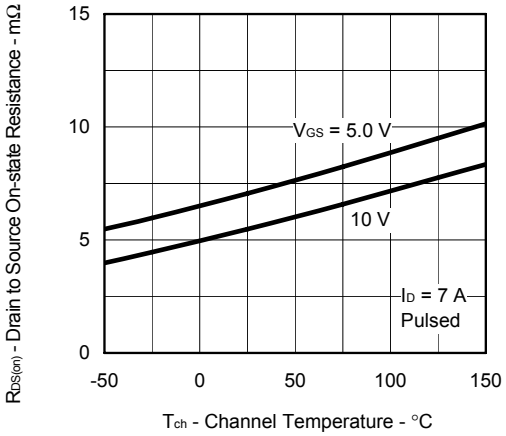
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



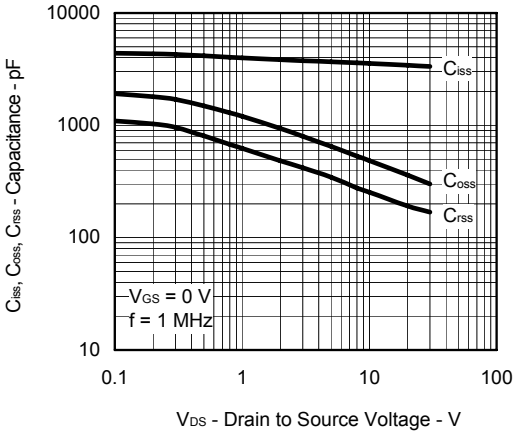
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



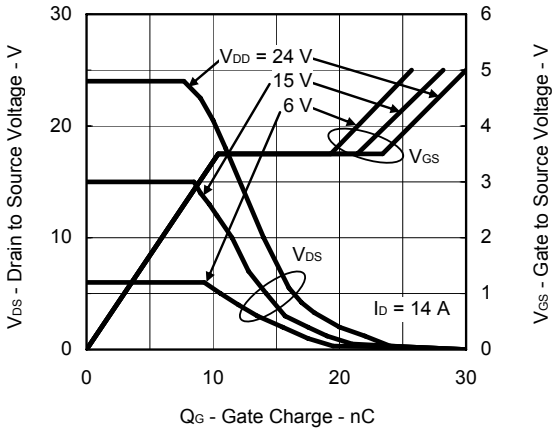
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



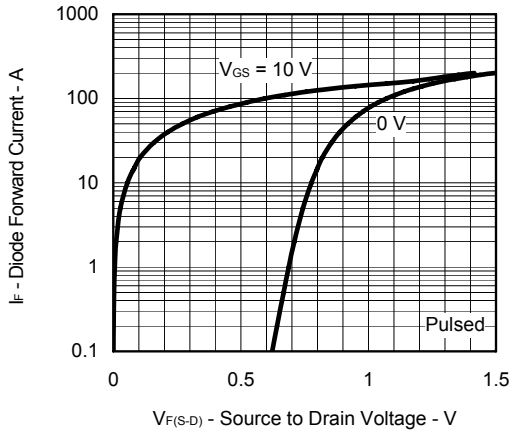
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



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