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SEMICONDUCTOR
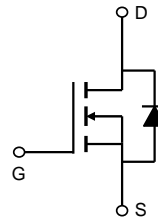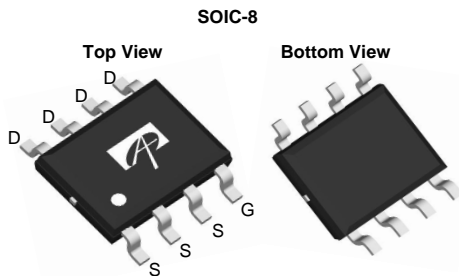
AO4494
30V N-Channel MOSFET

General Description

The AO4494 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is for PWM applications.

Product Summary

V_{DS} (V) = 30V

I_D = 18A   (V_{GS} = 10V)

$R_{DS(ON)}$ < 6.5mΩ   (V_{GS} = 10V)

$R_{DS(ON)}$ < 9.5mΩ   (V_{GS} = 4.5V)

100% UIS Tested

100% R_g Tested

Green Product

SOIC-8

Top View

Bottom View

Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	18	A
	T_C=70℃		14	
Pulsed Drain Current [C]		I_{DM}	130	
Avalanche Current [C]		I_{AR}	32	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	51	mJ
Power Dissipation [B]	T_C=25℃	P_D	3.1	W
	T_C=70℃		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	28	40	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		59	75	℃/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	16	24	℃/W

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Electrical Characteristics (T$_J$=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V		30			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=30V, V$_{GS}$=0V				1	µA
			T$_J$=125°C			5	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$= ±20V				±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$ I$_D$=250µA		1.5	2	2.5	V
I$_{D(ON)}$	On state drain current	V$_{GS}$=10V, V$_{DS}$=5V		130			A
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=18A			5.4	6.5	mΩ
			T$_J$=125°C		8.4	10.1	
		V$_{GS}$=4.5V, I$_D$=16A			7.5	9.5	mΩ
g$_{FS}$	Forward Transconductance	V$_{DS}$=5V, I$_D$=18A			70		S
V$_{SD}$	Diode Forward Voltage	I$_S$=1A,V$_{GS}$=0V			0.75	1	V
I$_S$	Maximum Body-Diode Continuous Current					3	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=15V, f=1MHz		1270	1590	1900	pF
C$_{oss}$	Output Capacitance			170	240	310	pF
C$_{rss}$	Reverse Transfer Capacitance			87	145	200	pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz		0.8	1.5	2.3	Ω
SWITCHING PARAMETERS							
Q$_g$(10V)	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=15V, I$_D$=18A		24	30	36	nC
Q$_g$(4.5V)	Total Gate Charge			12	15	18	nC
Q$_{gs}$	Gate Source Charge			4.2	5.2	6.2	nC
Q$_{gd}$	Gate Drain Charge			4.7	7.8	11	nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=15V, R$_L$=0.83Ω, R$_{GEN}$=3Ω			6.7		ns
t$_r$	Turn-On Rise Time				3.5		ns
t$_{D(off)}$	Turn-Off DelayTime				22.5		ns
t$_f$	Turn-Off Fall Time				4		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=18A, dI/dt=500A/µs		22	28	34	ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=18A, dI/dt=500A/µs		19	24	30	nC

A. The value of R$_{θJA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$ =25°C. The Power dissipation P$_{DSM}$ is based on R$_{θJA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T$_J$ =25°C.

D. The R$_{θJA}$ is the sum of the thermal impedence from junction to case R$_{θJC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=150°C. The SOA curve provides a single pulse ratin g.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
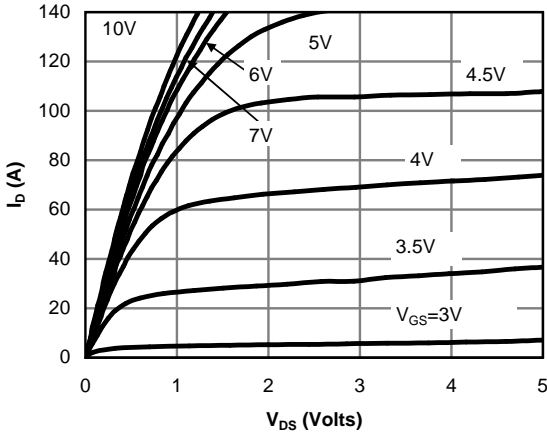

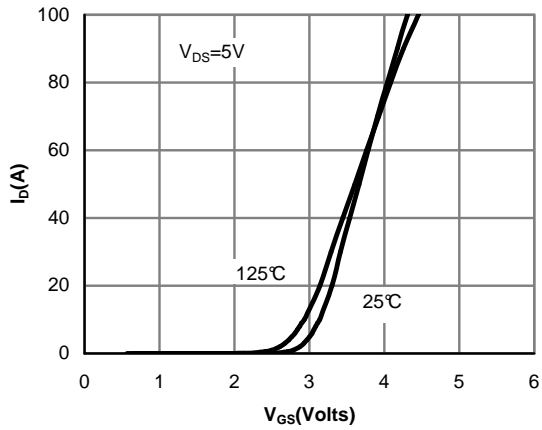**Fig 1: On-Region Characteristics (Note E)**

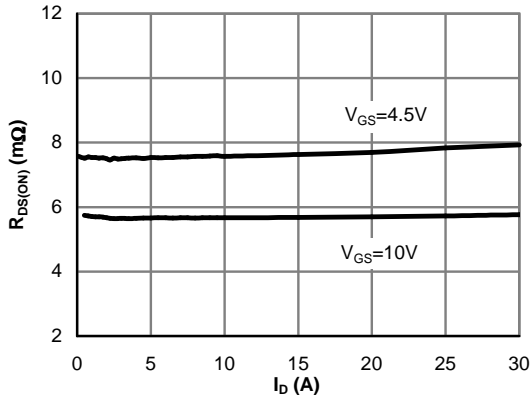**Figure 2: Transfer Characteristics (Note E)**

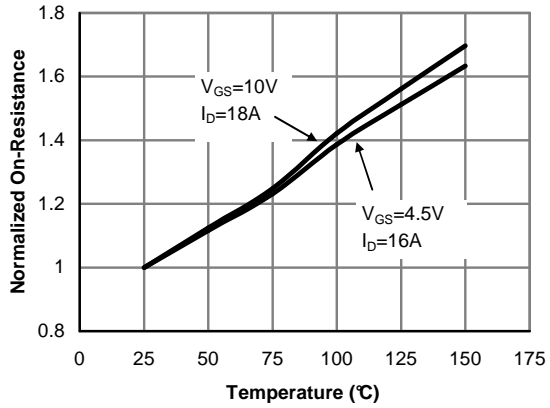**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**

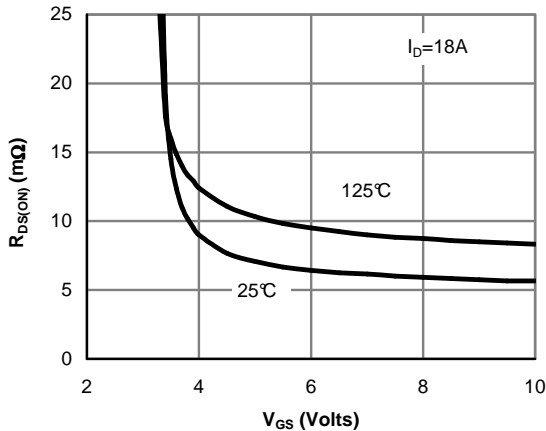**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

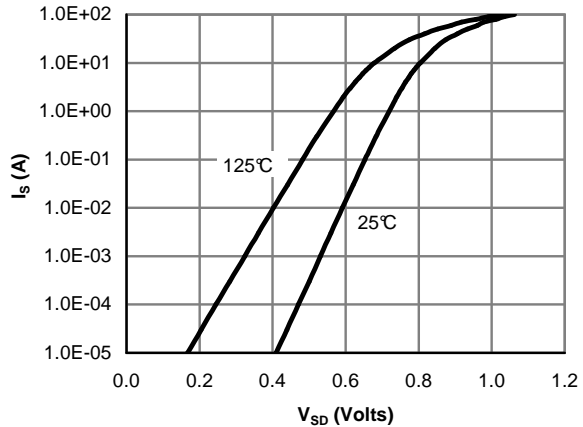**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

Figure 6: Body-Diode Characteristics (Note E)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
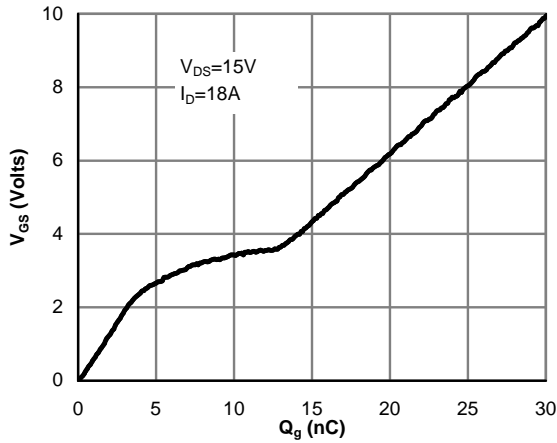
Figure 7: Gate-Charge Characteristics

V_{DS}=15V
I_D=18A
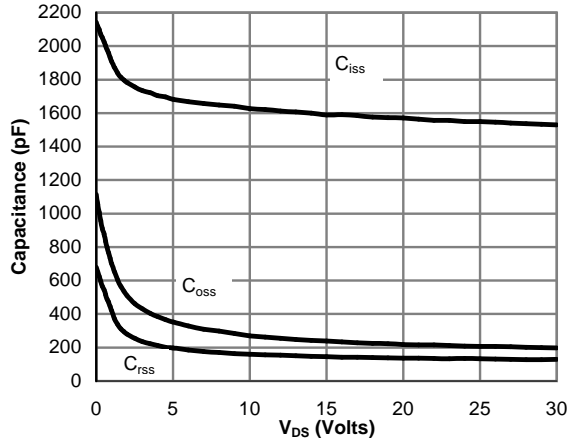
Figure 8: Capacitance Characteristics

C_{iss}
C_{oss}
C_{rss}
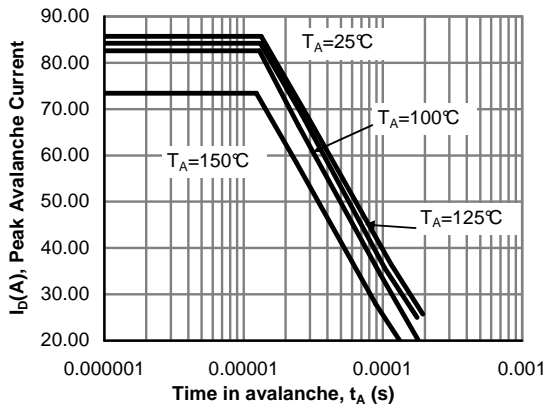
Figure 12: Single Pulse Avalanche capability (Note C)

T_A=25℃
T_A=100℃
T_A=150℃
T_A=125℃
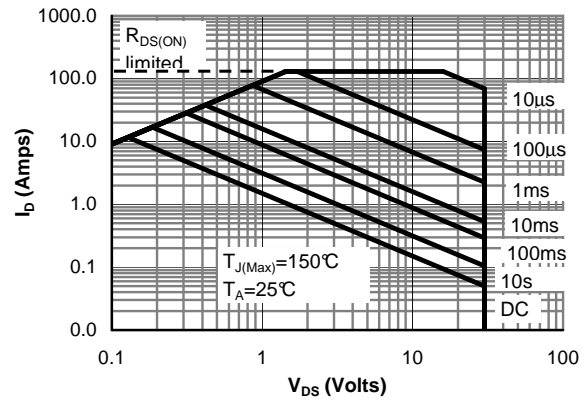
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

$R_{DS(ON)}$ limited
10µs
100µs
1ms
10ms
100ms
10s
DC
$T_{J(Max)}$=150℃
T_A=25℃
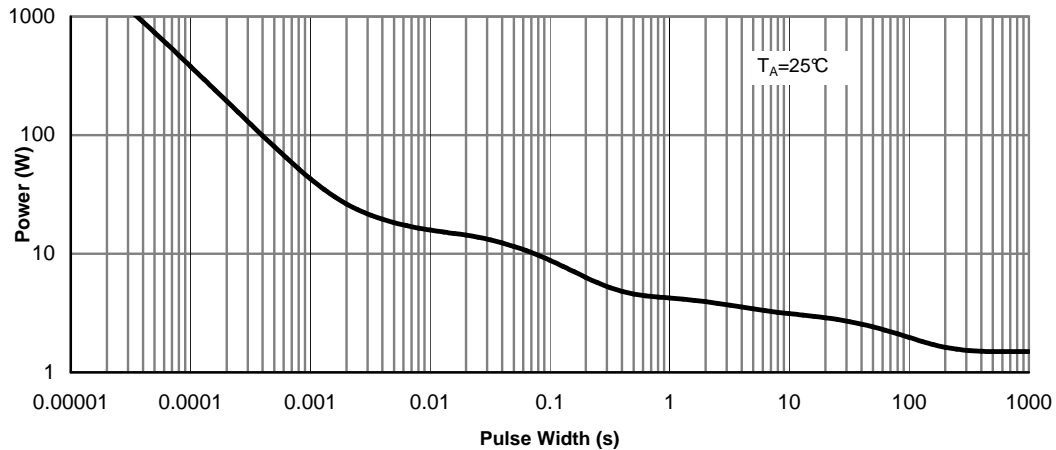
Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note F)

T_A=25℃

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
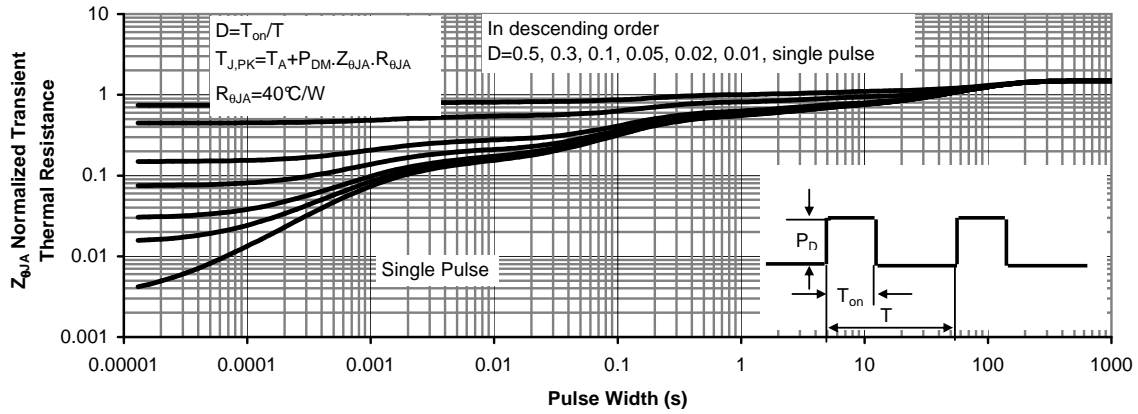
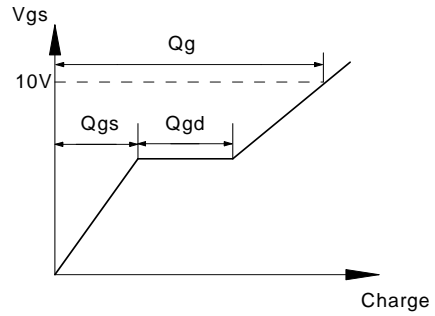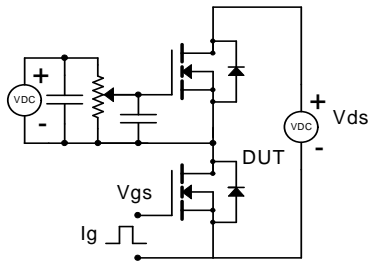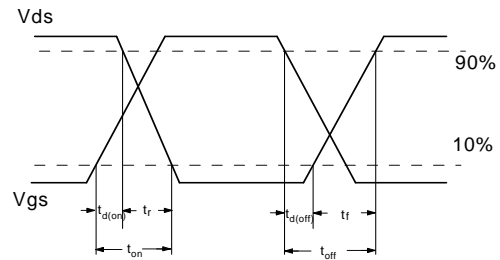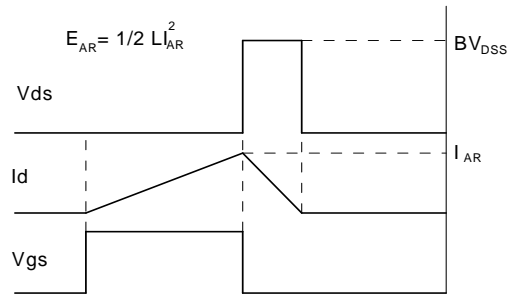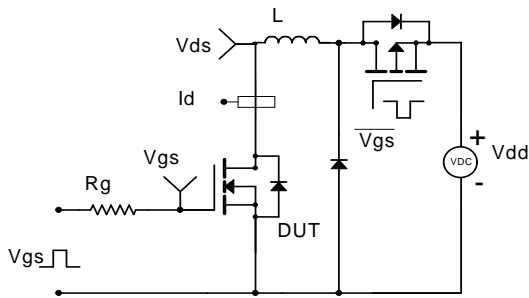
Figure 16: Normalized Maximum Transient Thermal Impedance (Note F)

Gate Charge Test Circuit & Waveform

Vgs

Qg

10V

Qgs Qgd

Charge

+ −
VDC

Vgs

Ig

DUT

+ Vds −
VDC

Resistive Switching Test Circuit & Waveforms

RL

Vds

Vgs

Rg

DUT

+ Vdd −
VDC

Vgs

Vds

90%

10%

Vgs

$t_{d(on)}$ t_r $t_{d(off)}$ t_f

t_{on} t_{off}
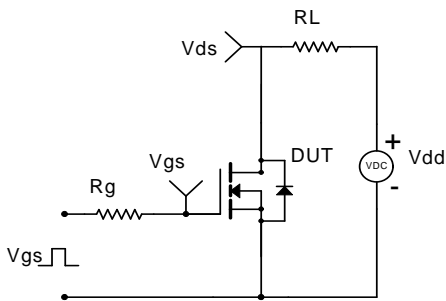
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

L

Vds

Id

Vgs

Rg

$\overline{Vgs}$

+ Vdd −
VDC

DUT

Vgs

$E_{AR} = 1/2\ LI_{AR}^2$

Vds

Id

Vgs

BV_{DSS}

I_{AR}

Diode Recovery Test Circuit & Waveforms

Vds +

Vds −

DUT

Isd

L

Vgs

Ig

+ Vdd −
VDC

$Q_{rr} = -\int Idt$

Vgs

Isd

I_F

dI/dt

t_{rr}

I_{RM}

Vds

Vdd

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