



SANYO Semiconductors

DATA SHEET

LV51134T — CMOS IC 2-Cell Lithium-Ion Secondary Battery Protection IC

Overview

The LV51134T is a protection IC for 2-cell lithium-ion secondary batteries.

Features

- Monitoring function for each cell: Detects overcharge and over-discharge conditions and controls the charging and discharging operation of each cell.
- High detection voltage accuracy: Over-charge detection accuracy $\pm 25\text{mV}$
Over-discharge detection accuracy $\pm 100\text{mV}$
- Hysteresis cancel function: The hysteresis of over-discharge detection voltage is made small by sensing the connection of a load after overcharging has been detected.
- Discharge current monitoring function: Detects over-currents, load shorting, and excessively high voltage of a charger and regulates charging and discharging operations.
- Low current consumption: Normal operation mode typ. $6.0\mu\text{A}$
Stand by mode max. $0.2\mu\text{A}$
- 0V cell charging function: Charging is enabled even when the cell voltage is 0V by giving a potential difference between the V_{DD} pin and V- pin.

- Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.
- Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

N2107 MS 20071031-S00002 / 52307 MS IM / 32207 MS IM 20070208-S00009 No.A0716-1/8

LV51134T

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|--|------------------|----------------|------------------------------|------------------|
| Power supply voltage | V_{DD} | | -0.3 to +12 | V |
| Input voltage Charger minus voltage | V^- | | $V_{DD}-28$ to $V_{DD}+0.3$ | V |
| Output voltage | Cout pin voltage | V_{cout} | $V_{DD}-28$ to $V_{DD}+0.3$ | V |
| | Dout pin voltage | V_{dout} | $V_{SS}-0.3$ to $V_{DD}+0.3$ | V |
| Allowable power dissipation | P_d max | Independent IC | 170 | mW |
| Operating ambient temperature | T_{opr} | | -30 to +80 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -40 to +125 | $^\circ\text{C}$ |

Electrical Characteristics at $T_a = 25^\circ\text{C}$, unless especially specified.

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|------------|--|---------------------|---------------------|---------------------|---------------|
| | | | min | typ | max | |
| Operation input voltage | V_{cell} | Between V_{DD} and V_{SS} | 1.5 | | 10 | V |
| 0V cell charging minimum operation voltage | V_{min} | Between $V_{DD}-V_{SS}=0$ and $V_{DD}-V^-$ | | | 1.5 | V |
| Over-charge detection voltage | V_{d1} | | 4.225 | 4.250 | 4.275 | V |
| Over-charge reset voltage | V_{r1} | $V^- \leq V_{d3}$ | 4.000 | 4.050 | 4.100 | V |
| | | $V^- > V_{d3}$ | 4.150 | | 4.260 | V |
| Over-charge detection delay time | t_{d1} | $V_{DD}-V_c=3.5V \rightarrow 4.5V$, $V_c-V_{SS}=3.5V$ | 0.5 | 1.0 | 1.5 | s |
| Over-charge reset delay time | t_{r1} | $V_{DD}-V_c=4.5V \rightarrow 3.5V$, $V_c-V_{SS}=3.5V$ | 20.0 | 40.0 | 60.0 | ms |
| Over-discharge detection voltage | V_{d2} | | 2.40 | 2.50 | 2.60 | V |
| Over-discharge reset hysteresis voltage | V_{h2} | | 10.0 | 20.0 | 44.0 | mV |
| Over-discharge detection delay time | t_{d2} | $V_{DD}-V_c=3.5V \rightarrow 2.2V$, $V_c-V_{SS}=3.5V$ | 50 | 100 | 150 | ms |
| Over-discharge reset delay time | t_{r2} | $V_{DD}-V_c=2.2V \rightarrow 3.5V$, $V_c-V_{SS}=3.5V$ | 0.5 | 1.0 | 1.5 | ms |
| Over-current detection voltage | V_{d3} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ | 0.270 | 0.300 | 0.330 | V |
| Over-current reset hysteresis voltage | V_{h3} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ | 5.0 | 10.0 | 20.0 | mV |
| Over-current detection delay time | t_{d3} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ | 10.0 | 20.0 | 30.0 | ms |
| Over-current reset delay time | t_{r3} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ | 0.5 | 1.0 | 1.5 | ms |
| Short circuit detection voltage | V_{d4} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ | 1.0 | 1.3 | 1.6 | V |
| Short circuit detection delay time | t_{d4} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ | 0.125 | 0.250 | 0.500 | ms |
| Over-charger detection voltage | V_{d5} | Between $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ (V^-)- V_{SS} | -0.60 | -0.45 | -0.30 | V |
| Overcharge reset hysteresis voltage | V_{h5} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ | 25.0 | 50.0 | 100.0 | mV |
| Standby reset voltage | V_{stb} | Between $V_{DD}-V_c=2.0V$, $V_c-V_{SS}=2.0V$ (V^-)- V_{SS} | $V_{DD} \times 0.4$ | $V_{DD} \times 0.5$ | $V_{DD} \times 0.6$ | V |
| Excessively high voltage charger detection delay time | t_{d5} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ * | 0.5 | 1.5 | 3.0 | ms |
| Excessively high voltage charger reset delay time | t_{r5} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ | 0.5 | 1.5 | 3.0 | ms |
| Reset resistance (connected to V_{DD}) | R_{DD} | | 100 | 200 | 400 | $k\Omega$ |
| Reset resistance (connected to V_{SS}) | R_{SS} | | 15 | 30 | 60 | $k\Omega$ |
| Cout Nch ON voltage | V_{OL1} | $I_{OL}=50\mu\text{A}$, $V_{DD}-V_c=4.4V$, $V_c-V_{SS}=4.4V$ | | | 0.5 | V |
| Cout Pch ON voltage | V_{OH1} | $I_{OL}=50\mu\text{A}$, $V_{DD}-V_c=3.9V$, $V_c-V_{SS}=3.9V$ | $V_{DD}-0.5$ | | | V |
| Dout Nch ON voltage | V_{OL2} | $I_{OL}=50\mu\text{A}$, $V_{DD}-V_c=2.2V$, $V_c-V_{SS}=2.2V$ | | | 0.5 | V |
| Dout Pch ON voltage | V_{OH2} | $I_{OL}=50\mu\text{A}$, $V_{DD}-V_c=3.9V$, $V_c-V_{SS}=3.9V$ | $V_{DD}-0.5$ | | | V |
| V_c input current | I_{vc} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ | | 0.0 | 1.0 | μA |
| Current drain | I_{DD} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ | | 6.0 | 13.0 | μA |
| Standby current | I_{stb} | $V_{DD}-V_c=2.2V$, $V_c-V_{SS}=3.5V$ | | | 0.2 | μA |
| T-terminal input ON voltage | V_{test} | $V_{DD}-V_c=3.5V$, $V_c-V_{SS}=3.5V$ | $V_{DD} \times 0.4$ | $V_{DD} \times 0.5$ | $V_{DD} \times 0.6$ | V |

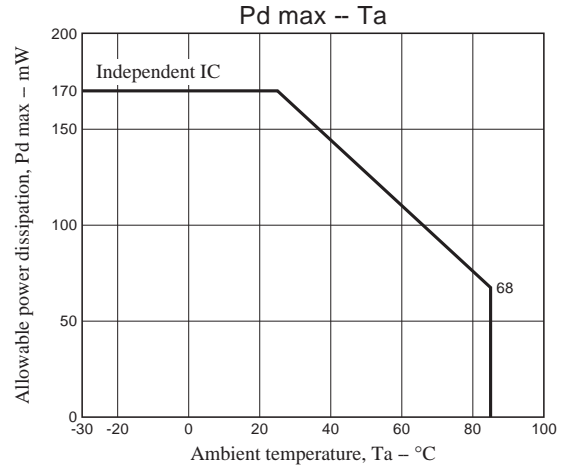
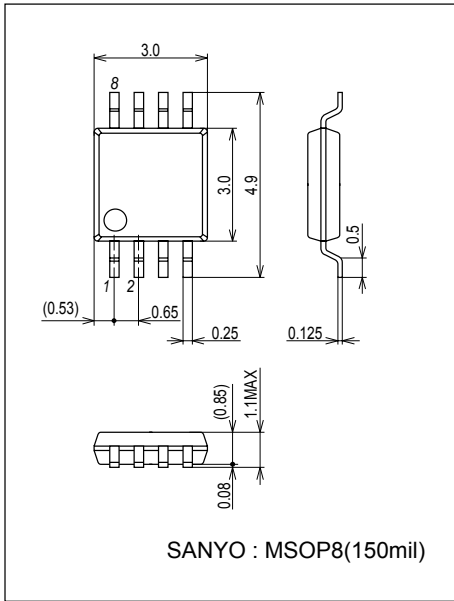
* Upon connecting to charger upon over-discharge, the delay time after recovery from over-discharge.

LV51134T

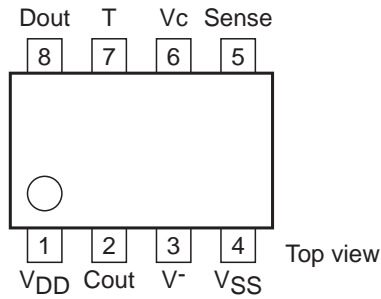
Package Dimensions

unit : mm (typ)

3245B



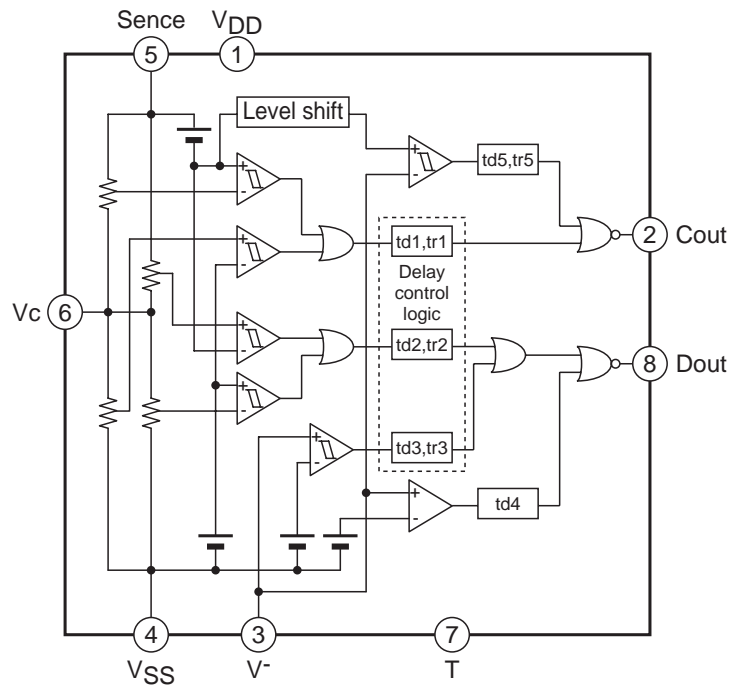
Pin Assignment



Pin Functions

| Pin No. | Symbol | Description |
|---------|-----------------|--|
| 1 | V _{DD} | V _{DD} pin |
| 2 | Cout | Overcharge detection output pin |
| 3 | V ⁻ | Charger minus voltage input pin |
| 4 | V _{SS} | V _{SS} pin |
| 5 | Sense | Sense pin |
| 6 | V _c | Intermediate voltage input pin |
| 7 | T | Pin to shorten detection time ("H":Shortening mode, "L":Normal mode) |
| 8 | Dout | Overdischarge detection output pin |

Block Diagram



Functional Description**Over-charge detection**

If either of the cell voltage is equal to or more than the over-charge detection voltage, stop further charging by turning “L” the Cout pin and turning off external Nch MOS FET after the over-charge detection delay time. This delay time is set by the internal counter.

The over-charge detection comparator has the hysteresis function. Note that this hysteresis can be cancelled by connecting the load after detection of over-charge detection. and it becomes small to hysteresis peculiar to a comparator.

Over-charge release

If both cell voltages become equal to or less than the over-charge release voltage ($V_M \leq V_{d3}$) when charger is connected, or if it become equal to or less than the over-charge release voltage ($V_M > V_{d3}$) when load is connected, the Cout pin returns to “H” after the over-charge release delay time set by the internal counter.

When load is connected and either cell or both cell voltages are equal to or more than the over-charge release voltage ($V_M > V_{d3}$), the Cout pin does not return to “H”. But the load current flows through the parasitic diode of external Nch MOS FET on Cout, consequently each cell voltage becomes equal to or less than over-charge release voltage, ($V_M > V_{d3}$) the Cout pin returns to “H.” after the over-charge release delay time.

However, excessive voltage charger is connected as mentioned below, Cout pin does not return to “H” because excessive charger detection starts after over-charge release operation.

Over-discharge detection

When either cell voltage is equal to or less than over-discharge voltage, the IC stops further discharging by turning the Dout pin “L” and turning off external Nch MOS FET after the over-charge detection delay time.

The IC goes into stand-by mode after detecting over-discharge and its consumption current is kept at about 0A. After over-discharge detection, the V- pin will be connected to V_{DD} pin via internal resistor (typ 200k Ω).

Over-discharge release

Release from over-discharge is made by only connecting charger. If the V- pin voltage becomes equal to or lower than the stand-by release voltage by connecting charger after detecting over-discharge, The IC is released from the stand-by state to start cell voltage monitoring. If both cell voltages become equal to or more than the over-discharge detection voltage by charging, the Dout pin returns to “H” after the over-discharge release delay time set by the internal counter.

Over-current detection

When excessive current flows through the battery, the V- pin voltage rises by the ON resistor of external MOS FET and becomes equal to or more than the over-current detection voltage, the Dout pin turns to “L” after the over-current detection delay time and the external Nch MOS FET is turned off to prevent excessive current in the circuit. The detection delay time is set by the internal counter. After detection, the V- pin will be connected to V_{SS} via internal resistor (typ 30k Ω). It will not go into stand-by mode after detecting over-current.

Short circuit detection

If greater discharging current flows through the battery and the V- pin voltage becomes equal to or more than the short-circuit detection voltage, it will go into short-circuit detection state after the short circuit delay time shorter than the over-current detection delay time. When short-circuit is detected, just like the time of over-current detection, the Dout pin turns to “L” and external Nch MOS FET is turned off to prevent high current in the circuit. The V- pin will be connected to V_{SS} after detection via internal resistor (typ. 30k Ω). It will not go into stand-by mode after detecting short circuit.

Over-current/short-detection release

After detecting over-current or short circuit, the internal resistor (typ. 30k Ω) between V- pin and V_{SS} pin becomes effective. If the load resistor is removed, the V- pin voltage will be pulled down to the V_{SS} level. Thereafter, the IC will be released from the over-current/short-circuit detection state when the V- pin voltage becomes equal to or less than the over-current detection voltage, and the Dout pin returns to “H” after over-current release delay time set by the internal counter.

Excessive charger detection/release

If the voltage between V⁻ pin and V_{SS} pin becomes equal to or less than the excessive charger detection voltage by connecting a charger, no charging can be made by turning the Cout pin “L” after delay time and turning off the external Nch MOS FET. If that voltage returns to equal to or more than the excessive charger detection voltage during detection delay time, the excessive charger detection will be stopped. If the voltage between V⁻ pin and V_{SS} pin becomes equal to or more than the excessive charger detection voltage after excessive charger detection, the Cout returns to “H” after delay time. The detection/return delay time is set internally.

If Dout pin is “L”, charging will be made through the parasitic diode of external Nch FET on Dout pin. In that case, the voltage between V⁻ pin and V_{SS} pin is nearly -V_f which is less than the over-charger detection voltage, therefore no excessive charger detection will be made during over-discharge, over-current and short-circuit detection.

Furthermore, if excessive voltage charger is connected to the over-discharged battery, no excessive charger detection is made while the Dout pin is “L”. But the battery is continued charging through the parasitic diode. If the battery voltage rises to the over-discharge detection voltage and the voltage between V⁻ pin and V_{SS} pin remains equal to or less than the excessive charger detection voltage, the delay operation will be started after Dout pin turns to “H.”

0V cell charging operation

If voltage between V_{DD} and V becomes equal to or more than the 0V cell charging lowest operation voltage when the cell voltage is 0V, the Cout pin turns to “H” and charging is enabled.

Shorten the test time

By turning T pin to the V_{DD}, the delay times set by the internal counter can be cut. If T pin is open, the delay times are normal. Delay time not set by the counter just like as short circuit detection delay cannot be controlled by this pin. And we recommend that T pin is connected to V_{SS} to prevent malfunction when excessive current flows in short circuit operation.

Operation in case of detection overlap

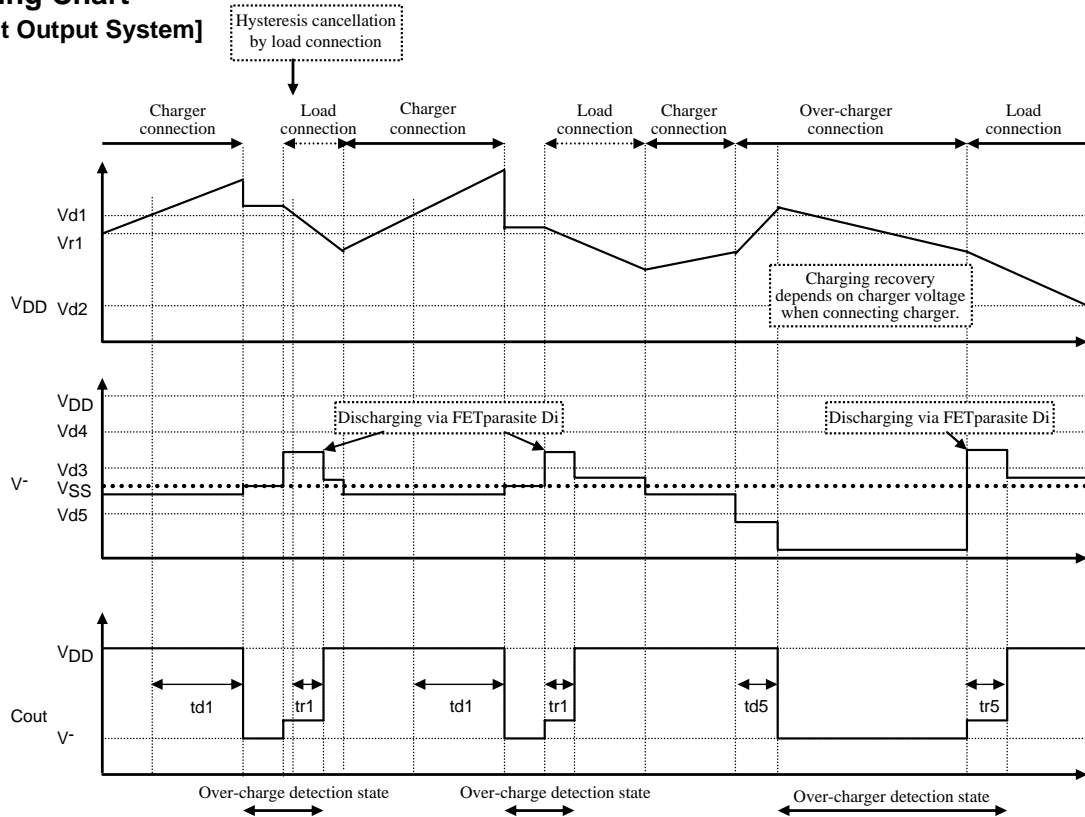
| Overlap state | | Operation in case of detection overlap | State after detection |
|--|-----------------------------------|---|---|
| When, during over-charge detection, | Over-discharge detection is made, | Over-charge detection is preferred. If over-discharge state continues even after over-charge detection, over-discharge detection is resumed. | When over-charge detection is made first, V ⁻ is released. When over-discharge is detected after over-charge detection, the standby state is not effectuated. Note that V ⁻ is connected to V _{DD} via 200kΩ. |
| | Over-current detection is made, | (*1) Both detections' can be made in parallel. Over-charge detection continues even when the over-current state occurs. If the over-charge state occurs first, over-current detection is interrupted. | (*2) When over-current is detected first, V ⁻ is connected to V _{SS} via 30kΩ. When over-charge detection is made first, V ⁻ is released. |
| When, during over-discharge detection, | Over-charge detection is made, | Over-discharge detection is interrupted and over-charge detection is preferred. When over-discharge state continues even after over-charge detection, over-discharge detection is resumed. | The standby state is not effectuated when over-discharge detection is made after over-charge detection. Note that V ⁻ is connected to V _{DD} via 200kΩ. |
| | Over-current detection is made, | (*3) Both detections can be made in parallel. Over-discharge detection continues even when the over-current state is effectuated first. Over-current detection is interrupted when the over-discharge state is effectuated first, | (*4) If over-current is detected in advance, V will be connected to V _{SS} via 30kΩ. After detecting over-discharge, V will be connected to V _{DD} via 200kΩ to get into standby state. If over-discharge is detected in advance, V will be connected to V _{DD} via 200kΩ to get into standby state. |
| When, during over-current detection, | Over-charge detection is made, | (*1) | (*2) |
| | Over-discharge detection is made, | (*3) | (*4) |

(Note) Short-circuit detection can be made independently.

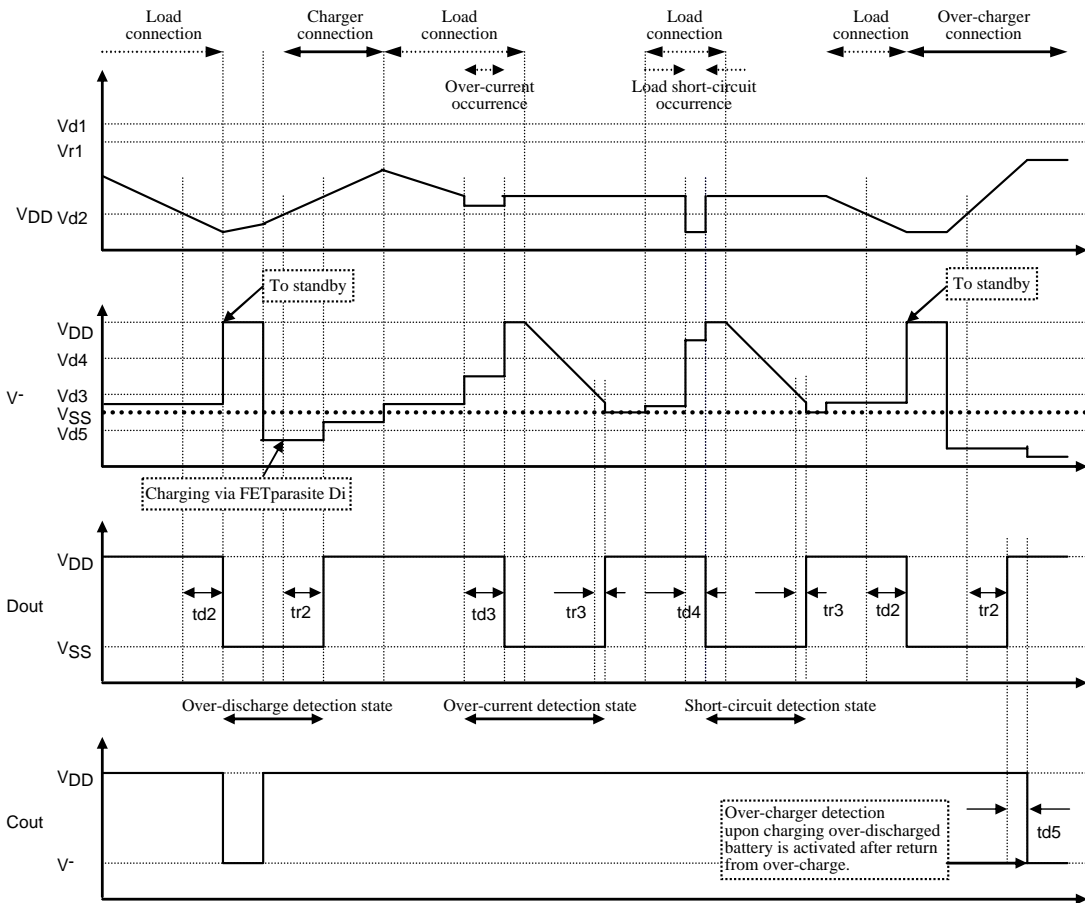
Over-charger detection does not work during over-discharge, over-current or short-circuit detection and the delay time starts after return from these states.

Timing Chart

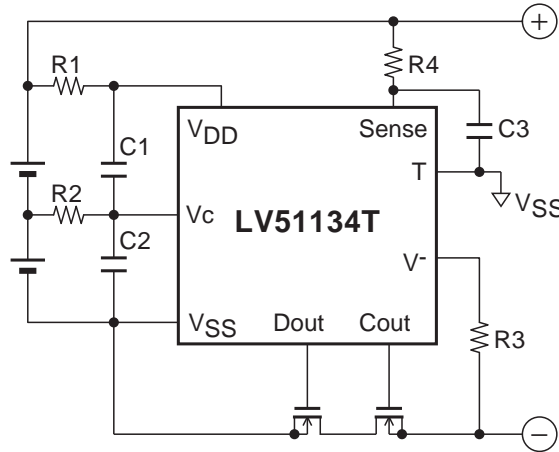
[Cout Output System]



[Dout Output System]



Application Circuit Example



| Components | Recommended value | max | unit |
|------------|-------------------|---------|----------|
| R1, R2 | 100 | 1k | Ω |
| R3 | 2k | 4k | Ω |
| R4 | 100 | 10k | Ω |
| C1, C2, C3 | 0.1 μ | 1 μ | F |

* These numbers don't mean to guarantee the characteristic of the IC.

* In addition to the components in the upper diagram, it is necessary to insert a capacitor with enough capacity between VDD and VSS of the IC as near as possible to stabilize the power supply voltage to the IC.

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of November, 2007. Specifications and information herein are subject to change without notice.