LA6557H



Five-Channel Bridge Driver for MD and CD Players

Overview

The LA6557H is a five-channel bridge driver developed for use in CD and MD players. It provides four BTL power amplifier channels and one H-bridge power amplifier channel.

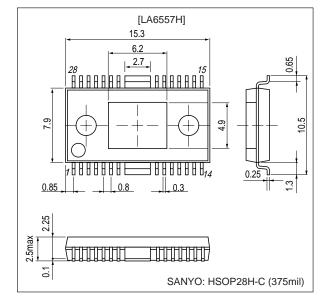
Features and Functions

- Four BTL power amplifier channels and one H-bridge power amplifier channel
- I_Omax: 700 mA (each channel)
- Built-in level shifter circuits (BTL amplifiers)
- One muting circuit (output on/off control) system that operates for the BTL amplifiers
- · Thermal shutdown circuit built in

Package Dimensions

unit: mm

3234-HSOP28H-C



Specifications

Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC} max		14	V
Maximum output current	I _O max	For each channel in channels 1 to 5	0.7	Α
Maximum input voltage	V _{IN} Bmax		13	V
Mute pin voltage	V _{MUTE}		13	V
Allowable newer dissipation	Dd man	Independent IC	0.82	W
Allowable power dissipation	Pd max	Mounted on the specified printed circuit board*	2.0	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

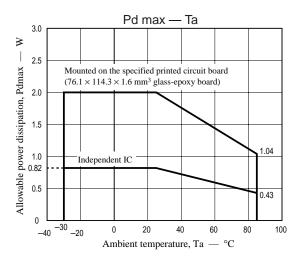
Note: * Specified printed circuit board: $76.1 \times 114.3 \times 1.6 \text{ mm}^3 \text{ glass-epoxy PCB}$

Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	Vcc		5.6 to 13	V

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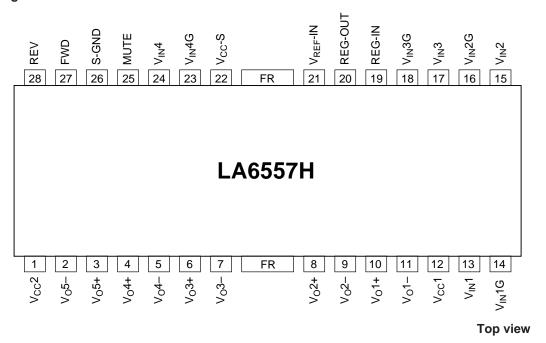


Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = $V_{CC}2$ = 8 V, V_{REF} = 1.65 V

Parameter	Crumb al	Conditions	Ratings			Unit	
Parameter	Symbol	Conditions	min	typ	max	Unit	
No-load current drain: on	I _{CC} -ON	All outputs on*1, FWD = REV = 0 V		30	50	mA	
No-load current drain: off	I _{CC} -OFF	All outputs off*1, FWD = REV = 0 V		10	20	mA	
V _{REF} input voltage range	V _{REF} -IN		1		V _{CC} -1	V	
[BTL Amplifier Block]	[BTL Amplifier Block]						
Output offset voltage	V _{OFF}	The voltage difference between outputs for the BTL amplifiers	-50		+50	mV	
Input voltage range	V _{IN}	The input voltage range	0		V _{CC}	V	
Output voltage	Vo	The voltage between V _O + and V _O – for each channel when R _L = 8 Ω .*2	4	5		V	
Closed-circuit voltage gain	V _G	Gain from input to output		12		dB	
Slew rate	SR	For independent amplifiers. Twice when measured between outputs *4		0.5		V/µs	
Mute on voltage	V _{MUTE} -ON	For each MUTE *3			0.5	V	
Mute off voltage	V _{MUTE} -OFF	For each MUTE *3	2			V	
[H Bridge Block]							
Output voltage	V _O -LOAD	The voltage between V _O + and V _O – for each channel when R _L = 8 Ω .*2		6		V	
Low-level input voltage	V _{IN} -L				1	V	
High-level input voltage	V _{IN} -H		2			V	
[Regulator Block]							
Output voltage	Vreg	I _L = 100 mA	4.75	5	5.25	V	
Output load regulation	ΔV_{RL}	I _L = 0 to 200 mA	-50	0	10	mV	
Supply voltage regulation	ΔVV _{CC}	V _{CC} = 6 to 12 V, I _L = 100 mA	-15	21	60	mV	

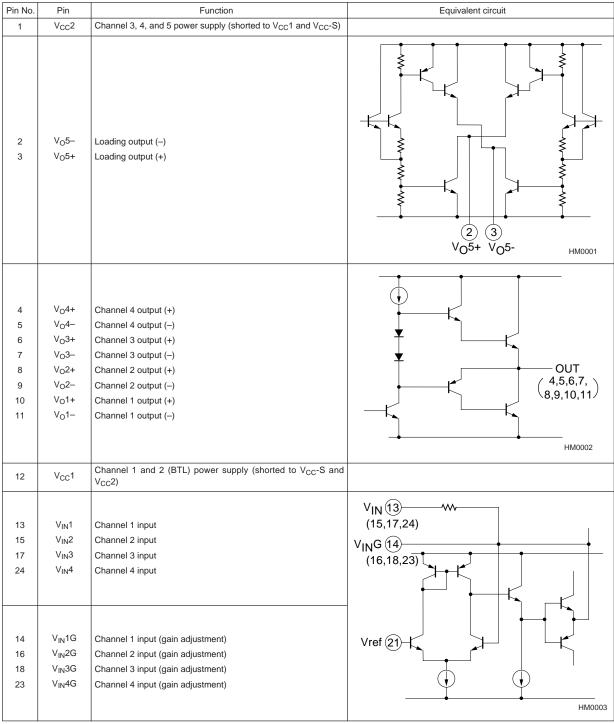
- Notes:1. The total current drain for V_{CC}1 and V_{CC}2 with no load.
 2. The voltage across an 8 Ω load. With the output saturated.
 3. MUTE: When the MUTE pin is high, the outputs will be on, and when low, off (high impedance)
 4. These values are design guarantee values, and are not tested.

Pin Assignment



LA6557H

Pin Description



Notes: The center frame (FR) functions as the power system ground. It must be, along with S-GND, at the lowest potential in the system. The power supply pins, V_{CC} -S, V_{CC} -1, and V_{CC} 2 must be shorted together externally to the IC.

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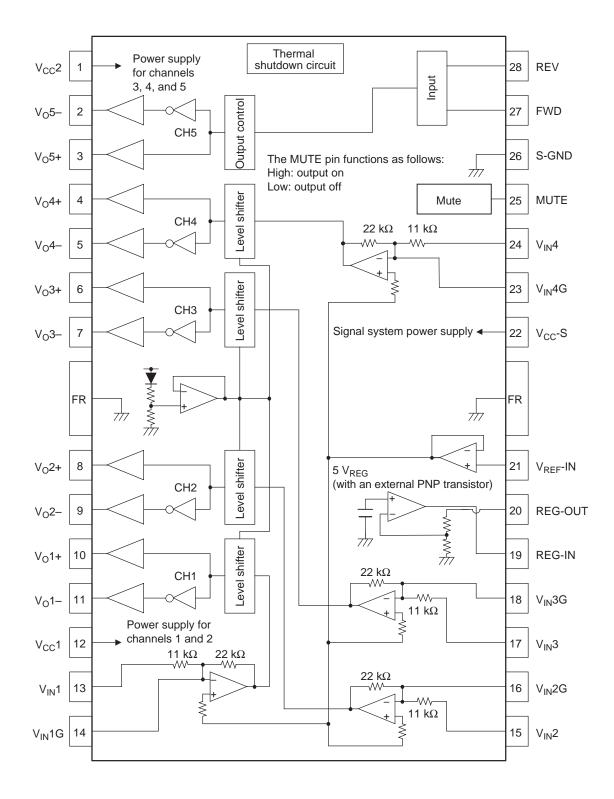
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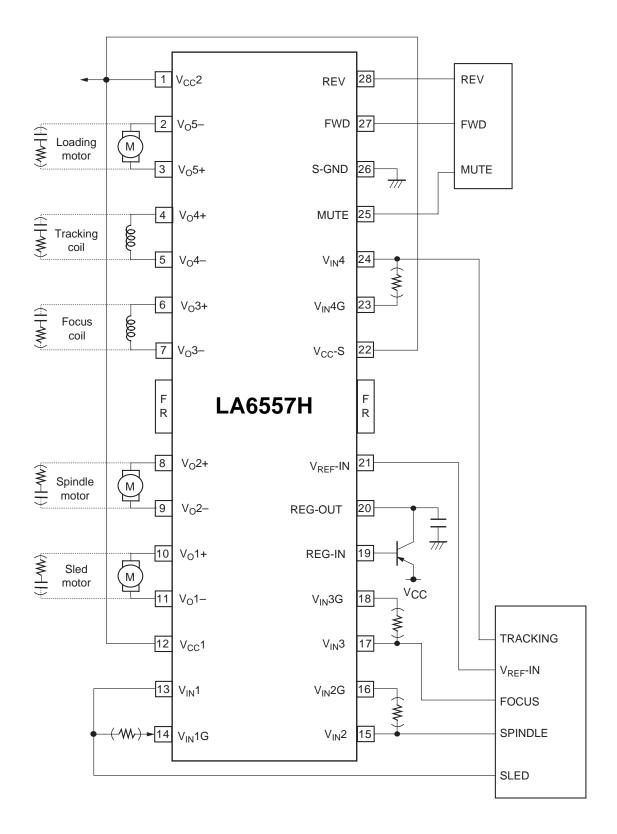
Pin No.	Pin	Function	Equivalent circuit
19	REG-IN	Regulator input (base of the external pnp transistor)	
20	REG-OUT	Regulator output (collector of the external pnp transistor)	
21	V _{REF} -IN	Reference voltage input	
22	V _{CC} -S	Signal system power supply (shorted to V _{CC} 1 and V _{CC} 2)	
25	MUTE	Output on/off control for channels 1 to 4 (the BTL amplifiers)	VCC 1 (12) MUTE 25 100 kΩ \$ S-GND 26
26	S-GND	Signal system ground	
27	FWD REV	Channel 5 (VLO) output switching (FWD), logic input to the loading block Channel 5 (VLO) output switching (REV), logic input to the loading block	27 FWD
			HM0005

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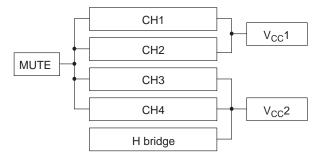
Block Diagram



Sample Application Circuit



System Diagram (Relationship between MUTE and the power supplies (V_{CC}^*))



Note: * V_{CC}1 and V_{CC}2 must be connected externally.

H Bridge Block

FWD	REV	V _O 5+	V _O 5-	Mode
L	L	OFF	OFF	Open *1
L	Н	Н	L	Forward
Н	L	L	Н	Reverse
Н	Н	L	L	Brake *2

Notes: 1. The outputs are in the high-impedance state in this mode.

2. During braking, the sink side transistor will be turned on (short braking).

V_{LO}+ and V_{LO}- will be close to the ground level.

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