Ordering number : ENA0597

SANYO Semiconductors
DATA SHEET

LA6559 — Monolithic Linear IC For CD 5-Channel Driver (BTL : Four-Channel, H Bridge : One-Channel)

Overview

The LA6559 is a 5-channel driver (BTL : 4-channel, H bridge : 1-channel) for CD players.

Functions

- Power amplifier 5-channel built-in. (Bridge-connection (BTL) : 4-channel, H bridge : 1-channel)
- I_O max 1A
- Level shift circuit built-in (except H bridge).
- Mute circuit (output ON/OFF) built-in.
  (Operable with BTL AMP with MUTE1 : CH1 and MUTE2 : CH2 to 4 and not operable for the H bridge of 3.3VREG)
- 3.3V regulator built-in (external PNP transistor).
- With a function to set the loading output voltage
- Overheat protection circuit (thermal shutdown) built-in.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Allowable power dissipation	Pd max	Independent IC	0.8	W
		Mounted on a standard board. *	2	W
Maximum output current	I_O max	Each output for H bridge, channel 1 to 4.	1	A
Maximum input voltage	$V_{IN}B$		13	V
MUTE pin voltage	VMUTE		13	V
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Standard board size : 76.1×114.3×1.6mm^3, glass epoxy.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}	Same for V_{CC}-VREG	5.6 to 13	V

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Electrical Characteristics at Ta = 25°C, $V_{CC}1 = V_{CC}2 = 8V$, VREF = 1.65V, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
ALL Blocks						
No-load current drain ON	I_{CC}-ON	BTL-AMP output ON, LOADING block OFF *1		30	50	mA
No-load current drain OFF	I_{CC}-OFF	All outputs OFF *1		10	20	mA
VREF input voltage range	VREF-IN		1		V_{CC}-1.5	V
Thermal shutdown temperature	TSD	*2	150	175	200	°C
BTL AMP Block (CH1 to CH4)						
Output offset voltage	V_{OFF}	Voltage difference between outputs for BTL AMP, each channel. *3	-60		60	mV
Input voltage range	V_{IN}	Input voltage range for input for OP-AMP.	0		V_{CC}-1.5	mA
Output voltage	V_O	Each voltage between V_0+ and V_0- when R_L = 8Ω. *4	5.7	6.5		V
Closed-circuit voltage gain	VG	Input and output gain. *3	5.4	6	6.6	Times
Slew rate	SR	AMP Independent Multiply 2 between outputs. *2		0.5		V/μs
MUTE ON voltage	VMUTE-ON	Each MUTE *5	2			V
MUTE OFF voltage	VMUTE-OFF	Each MUTE *5			0.5	V
Input AMP Block (CH1 to 4)						
Input voltage range	V_{IN}-OP		0		V_{CC}-1.5	V
Output current (SINK)	SINK-OP		2			mA
Output current (SOURCE)	SOURCE-OP	*6	300	500		μA
Output offset voltage	V_{OFF}-OP		-10		10	mV
Loading Block (CH5, H bridge)						
Output voltage	V_O-LOAD	Forward, reverse, R_L = 8Ω, VCONT=8V *4	5.7	6.5		V
Break output saturation voltage	V_{CE}-BREAK	Output voltage at braking *7			0.3	V
Input low level	V_{IN}-L				1	V
Input high level	V_{IN}-H		2			V
Output set voltage	VCONT	I_O = 200mA (Between outputs), VCONT = 3V	2.9	3.15	3.4	V
Power Supply Block (PNP transistor : 2SB632K-use)						
3.3V supply voltage	V_{OUT}	I_O = 200mA	3.15	3.3	3.45	V
REG-IN SINK current	REG-IN-SINK	Base current of external PNP *8		10		mA
Line regulation	ΔV_OLN	6V ≤ V_{CC} ≤ 12V		20	150	mV
Load regulation	ΔV_OLD	5mA ≤ I_O ≤ 200mA		50	200	mV

Note *1 : Current dissipation that is a sum of $V_{CC}1$ and $V_{CC}2$ and S-V_{CC} at no load.

*2 : Design guarantee value

*3 : Input AMP is a BUFFER AMP.

*4 : Voltage difference between both ends of load (8Ω). Output saturated.

*5 : Output ON with MUTE : [H] and OFF with MUTE : [L] (HI impedance).

*6 : The source of input OP-AMP is a constant current. As the 11kΩ resistance to the next stage is a load, pay due attention when setting the input OP-AMP gain.

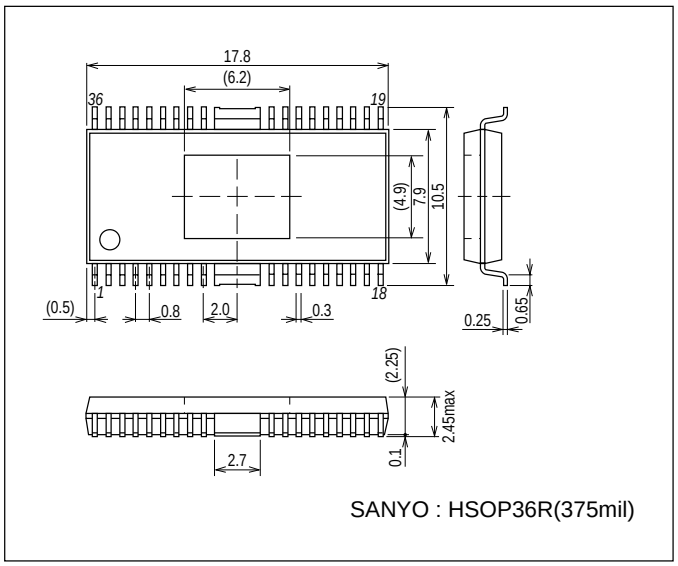
*7 : Short (GND) brake used. SINK side output ON.

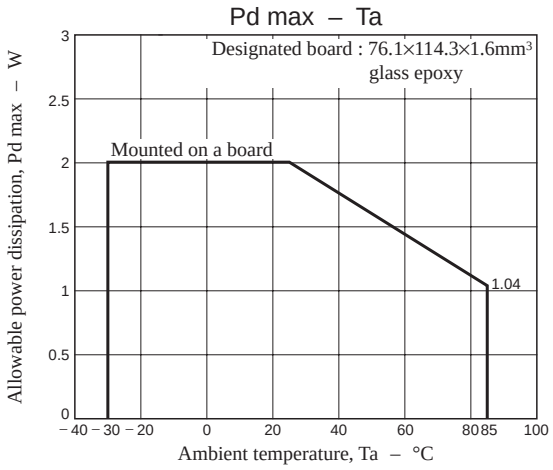
*8 : 3.3VREG incorporates a drooping protection circuit and operated when the base current is 10mA (TYP).

Package Dimensions

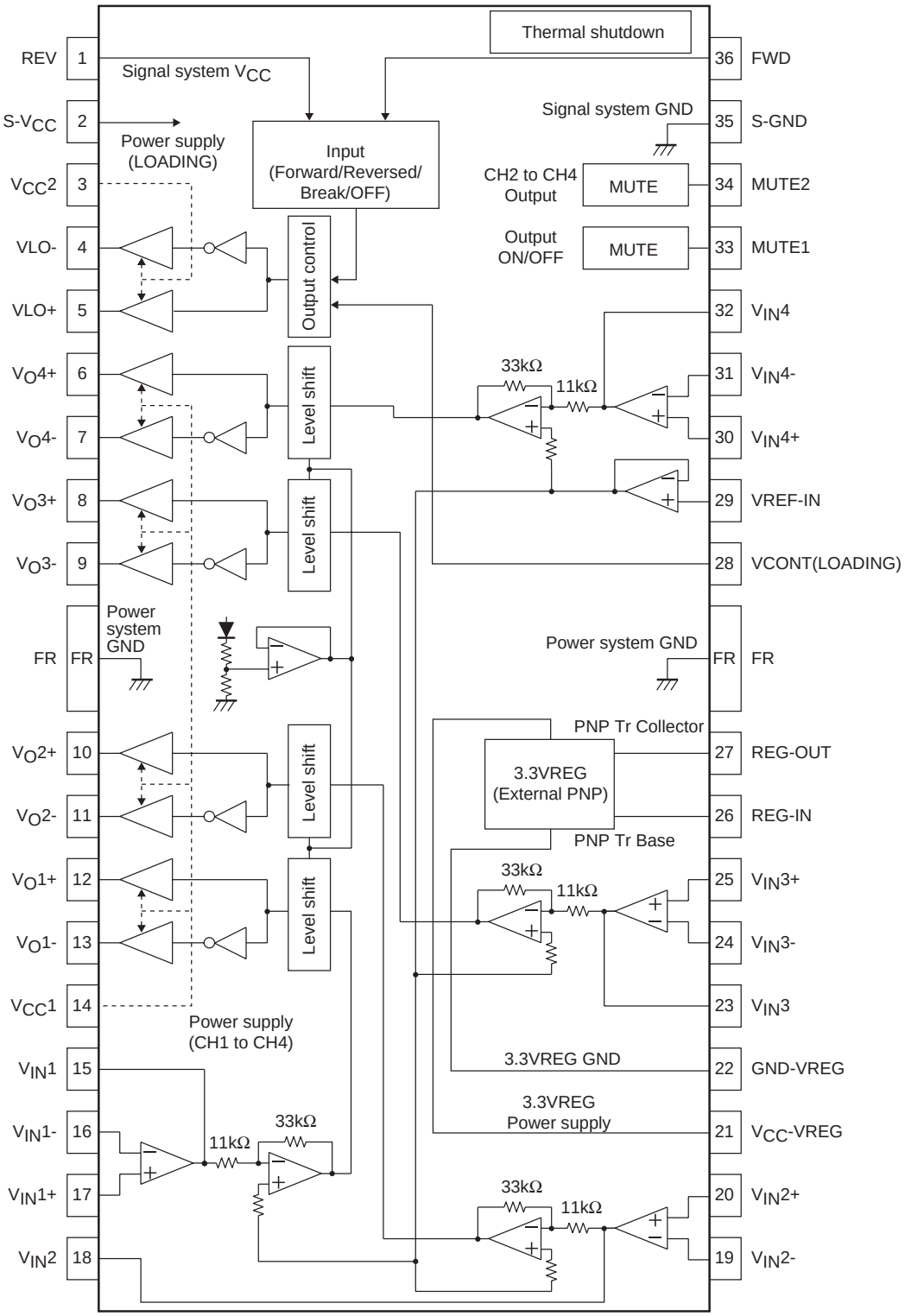
unit : mm (typ)

3251





Block Diagram



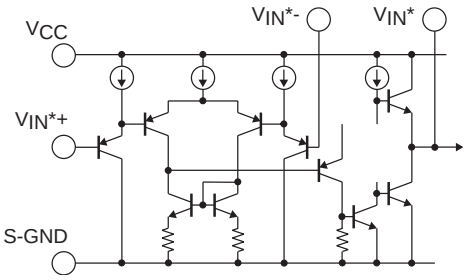
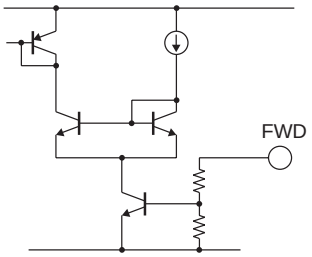
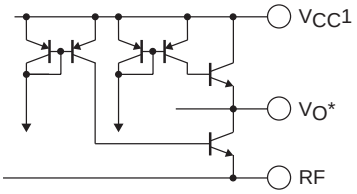
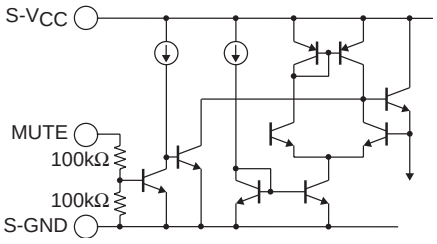
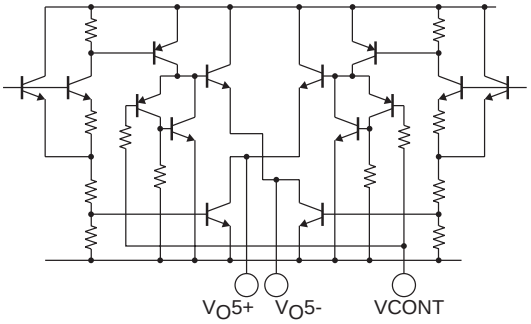
Pin Functions

Pin No.	Symbol	Pin descriptions
1	REV	5CH (VLO) Output change pin (REV), logic input for loading block.
2	S-V_{CC}	Signal system power supply (BTL-AMP : CH1 to 4)
3	$V_{CC}2$	Power supply for loading block
4	VLO-	Loading output (-)
5	VLO+	Loading output (+)
6	V_O4+	Output pin (+) for channel 4
7	V_O4-	Output pin (-) for channel 4
8	V_O3+	Output pin (+) for channel 3
9	V_O3-	Output pin (-) for channel 3
10	V_O2+	Output pin (+) for channel 2
11	V_O2-	Output pin (-) for channel 2
12	V_O1+	Output pin (+) for channel 1
13	V_O1-	Output pin (-) for channel 1
14	$V_{CC}1$	CH1 to CH4 (BTL-AMP) output stage power supply
15	$V_{IN}1$	Input pin for channel 1
16	$V_{IN}1$-	OP-AMP input AMP-A input pin (-)
17	$V_{IN}1$+	OP-AMP input AMP-A input pin (+)
18	$V_{IN}2$	Input pin for channel 2, input AMP output
19	$V_{IN}2$-	Input pin (-) for channel 2
20	$V_{IN}2$+	Input pin (+) for channel 2
21	V_{CC}-VREG	3.3VREG power supply
22	GND-VREG	3.3VREG GND
23	$V_{IN}3$	Input pin for channel 3, input AMP output
24	$V_{IN}3$-	Input pin (-) for channel 3
25	$V_{IN}3$+	Input pin (+) for channel 3
26	REG-IN	PNP transistor base connected
27	REG-OUT	3.3V power output to which the PNP transistor collector connected.
28	VCONT (LOADING)	Output voltage set pin for loading block
29	VREF-IN	Reference voltage applied pin
30	$V_{IN}4$+	Input pin (+) for channel 4
31	$V_{IN}4$-	Input pin (-) for channel 4
32	$V_{IN}4$	Input pin for channel 4, input AMP output
33	MUTE1	Output ON/OFF, channel 1 (BTL AMP)
34	MUTE2	Output ON/OFF, channel 2 to 4 (BTL AMP)
35	S-GND	Signal system GND
36	FWD	Output change pin (FWD) for loading output (VLO+ -), logic input for loading block.

Note 1 : Center frame (FR) becomes GND for the power system (P-GND). Set this to the minimum potential together with S-GND.

Note 2 : Short-circuit each of $V_{CC}1$, $V_{CC}2$, V_{CC}-VREG, and S-V_{CC} power pins externally.

Pin Description

Pin No.	Symbol	Pin function	Description	Equivalent circuit
17 16 15 20 19 18 25 24 23 30 31 32	$V_{IN}1+$ $V_{IN}1-$ $V_{IN}1$ $V_{IN}2+$ $V_{IN}2-$ $V_{IN}2$ $V_{IN}3+$ $V_{IN}3-$ $V_{IN}3$ $V_{IN}4+$ $V_{IN}4-$ $V_{IN}4$	Input (CH1 to 4)	Input pin (CH1 to 4)	
36 1	FWD REV	Input (LOADING)	Logic input pin. By combining H and L of this pin, any one of four modes (forward/ reversed/brake/idling) can be selected.	
12 13 10 11 8 9 6 7	V_O1+ V_O1- V_O2+ V_O2- V_O3+ V_O3- V_O4+ V_O4-	Output (CH1 to 4)	Output for channel 1 to 4.	
33 34	MUTE1 MUTE2	MUTE	BTL AMP output. Output ON/OFF for CH1 to CH4. MUTE : H Output OFF MUTE : L Output OFF	
5 4 28	VLO- VLO+ VCONT	Output (LOADING)	Output voltage set pin for loading block	

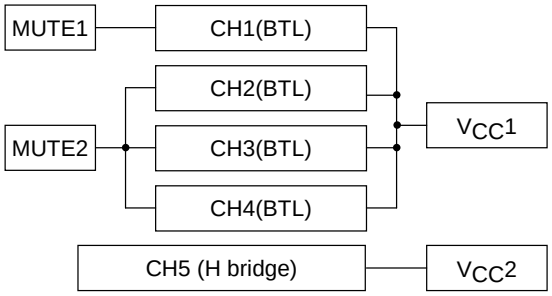
Truth Table (loading (H bridge) section)

FWD	REV	Loading output
L	L	OFF *1
	H	Forward
H	L	Reversed
	H	(Short) brake *2

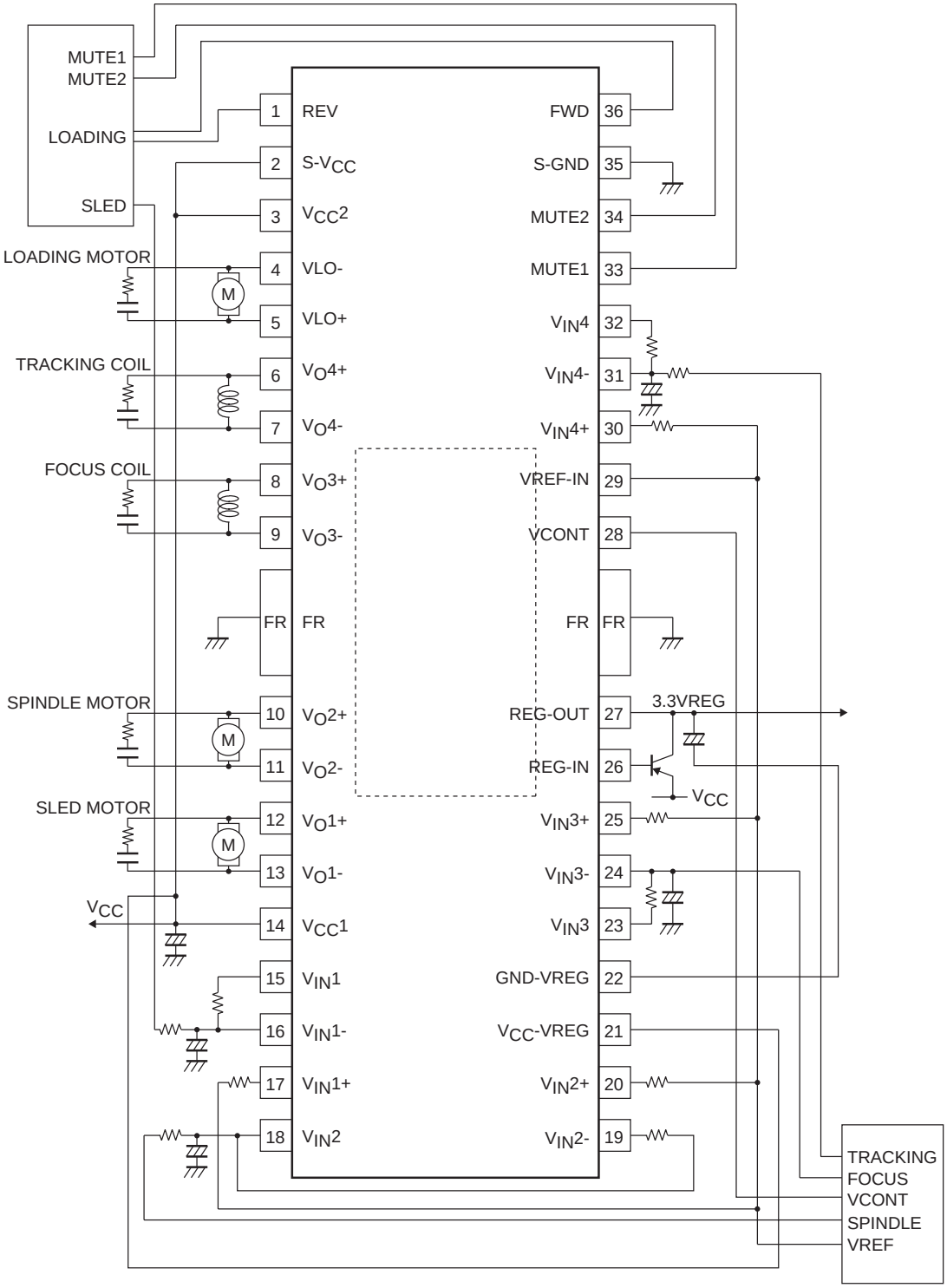
*1 The output has a high impedance.

*2 At brake, the SINK side transistor is ON (short brake).
VLO+ and VLO- are approximately on the GND level.

Relation of MUTE and Power (V_{CC}*)



Sample Application Circuit



Note : Add CR between outputs or to a circuit to GND when oscillation occurs in the output
(Example : R = 2.2Ω, C = 0.1μF). Apply 4.5V or more to the external PNPTr emitter pin.