

SANYO Semiconductors DATA SHEET

LA6502-

Monolithic Linear IC 5ch driver for CD and DVD Spindle driver : 3-phase linear sensor-less drive BTL 4ch

Overview

This LA6502 is a 5ch driver for CD and DVD Spindle driver : 3-phase linear sensor-less drive BTL 4ch.

Features

- Spindle driver block
- 1) 3-phase sensor-less motor driver
- 2) Soft switching drive
- 3) Analog input V type control
- 4) Current limiter incorporated
- 5) Counter electromotive FG output
- 6) Reverse prevention circuit incorporated
- Threading, focusing, tracking, and loading blocks
- 1) BTL-AMP type
- Common block
- 1) Thermal shutdown circuit incorporated (design guarantee)
- 2) MUTE function incorporated (pin 3)
- 3) OP-AMP (1ch) incorporated (open collector output)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor Supply Voltage 1	V _{CC} 1	SPINDLE, SLED, LOADING power supply	14.5	V
Motor Supply Voltage 2	V _{CC} 2	FOCUS, TRACKING power supply	14.5	V
Allowable power dissipation	Pd max1	Independent IC	0.8	W
	Pd max2	Mounted on a specified board. *	1.7	W

* Mounted on a board : 114.3×76.1×1.6mm³, glass epoxy board.

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Parameter	Symbol	Conditions	Ratings	Unit
Maximum input voltage	V _{IN} max		-0.3 to V _{CC} +0.3	V
Maximum output current 1	IO max1	SPINDLE output	1.0	Α
Maximum output current 2	I _O max2	SLED output	0.6	А
Maximum output current 3	I _O max3	FOCUS, TRACKING output	0.85	А
Maximum output current 4	I _O max4	LOADING output	0.6	Α
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

Recommended Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Motor Supply Voltage 1	V _{CC} 1	SPINDLE, SLED, LOADING power supply	4.5 to 13.8	V
Motor Supply Voltage 2	V _{CC} 2	FOCUS, TRACKING power supply	4.5 to 13.8	V

Electrical Characteristics at Ta = 25°C, $V_{CC}1 = 8V$, $V_{CC}2 = 8V$, VREF = 1.65V

Latination Opinion Opinion min typ max Other Common Contront drain I_CC_0 MUTE1.2, 3: H, V_C = VREF I.0. 0.3 0.5 mA Standby current I_CC_0 MUTE1.2, 3: L I.0. 0.3 0.5 mA VREF pin input voltage range VREF V_C= VREF 1.0.0 0.4 0.5 V MUTE1.2, 3: Loutage VMUTE-L 0.0.5 V MUTE1.2, 3: Loutage VMUTE-L 0.0.5 V MUTE1.2, 3: Loutage VMUTE-L 2.8 0.60 10.0 µA MUTE1.2, 3: Loutage VMUTE-L V 0.80 10.0 µA MUTE1.2, 3: Input current IMUTE VMUTE-3V 0.60 10.0 µA MUTE1.2, 3: Input current TSD Designed target value 150 180 210 °C Thermal shutdown hysteresis width ΔTSD Designed target value 1.8 2.4 V CTL pin input voltage range VCT_SP V_C = VREF = 1.65V	Parameter	Symbol	Symbol Conditions		Ratings		
Common Current drain ILCC MUTE1, 2, 3; H, VC = VREF 30 40 mA Standby current ILCC MUTE1, 2, 3; L 0.3 0.5 mA VREF pin input current IVCREF VEF 1.0 0.3 0.5 mA VREF pin input current IVCREF VEF = 1.85V -0.2 -0.1 µA MUTE1, 2, 3 I voltage VMUTE-H 2.8 0.5 V MUTE1, 2, 3 I voltage VMUTE-H 2.8 0.65 V MUTE1, 2, 3 I voltage VMUTE-H 2.8 0.60 100 µA Thermal shutdown operation TSD Designet target value 1.60 180 210 °C Note) Designe guarantee values, nor measured: Designet target value 0 1.8 2.4 V CTL pin input voltage range VCL_SP Iog =0.5A, Source+Sink 1.8 2.4 V CTL pin input voltage range VCL_SP Iog =0.5A, Source+Sink 1.8 2.4 V CTL pin input current IVCL_SP <td></td> <td>Symbol</td> <td>typ</td> <td>max</td> <td>Onit</td>		Symbol			typ	max	Onit
Current drain I _{CC} MUTE1, 2, 3 : H, V _C = VREF 30 40 mA Standby current I _{CC0} MUTE1, 2, 3 : L 0.3 0.3 0.5 mA VREF pin input voltage range VREF I 0.5 V MUTE1, 2, 3 L voltage VMUTE-L 0.5 V MUTE1, 2, 3 L voltage VMUTE-L - 0.6 10 0.5 V MUTE1, 2, 3 L voltage VMUTE-L - 0.6 10.0 µA MUTE1, 2, 3 L voltage VMUTE-H - 0.6 10.0 µA MUTE1, 2, 3 L voltage VMUTE + M - - 0.0 10.0 µA MUTE1, 2, 3 L voltage VMUTE + M - - 0.0 1.0 µA MUTE1, 2, 3 L voltage VMUTE + M - - 0.0 1.0 .0 .0 .0 .0 .0 .0 .0 .0 .0 .0 .0 .0 .0 .0 .0 .0 .0 .0 .0	Common						
Shandby current I _{CCQ} MUTE1, 2, 3 : L 0.0 0.3 0.5 mA VREF pin input voltage range VREF V -0.0 -0.1 () A.3.3 V MUTE1, 2, 3 L voltage VMUTE-L -0.0 -0.0 () A.3.5 V MUTE1, 2, 3 L voltage VMUTE-H -0.0 2.8 -0.5 V MUTE1, 2, 3 hvoltage VMUTE-H 2.8 -0.5 V MUTE1, 2, 3 hvoltage VMUTE-H 2.8 -0.5 V MUTE1, 2, 3 input current IMUTE VMUTE = 3V -0.0 6.0 10.0 µA Thermal shutdown operation TSD Designed target value 10.8 2.10 'C c Output saturation voltage VCGSAT_SP IO =0.5A, Source+Sink 1.8 2.4 V CTL pin input voltage range VCT_SP VC = VREF = 1.6SV -0.2 -0.5 µA Control dead zone width 1 VCDZ_SP Revers -150 -00 mV Control dead z	Current drain	ICC	MUTE1, 2, 3 : H, V _C = VREF		30	40	mA
VREF pin input voltage range VREF 1.0 3.3 V VRE pin input current IVCREF VC_C = VREF = 1.6SV -0.2 -0.1 44 VITE1, 2, 1 voltage VMUTE-H 2.8 -0.1 4.5 V MUTE1, 2, 3 input current IMUTE VMUTE+4 2.8 -0.0 4.5 V MUTE1, 2, 3 input current IMUTE VMUTE+3V -0.0 6.0 10.0 µA Thermal shutdown operation emperature TSD Designe target value -0.0 -0.0 -0.0 Note) Design guarante evalues, not=wet wet Wet -0.0<	Standby current	ICCQ	MUTE1, 2, 3 : L		0.3	0.5	mA
VREF pin input current IVCREF V _C = VREF = 1.85V -0.2 -0.1 μ A MUTE 1, 2, 3 L voltage VMUTE-L 0.5 V MUTE 1, 2, 3 L voltage VMUTE + 0.6 0.0 μ A MUTE 1, 2, 3 Input current IMUTE VMUTE = 3V 60 100 μ A Thermal shutdown operation TSD Designed target value 150 180 210 °C Itemperature A D C °C Note Note Note Note °C Note	VREF pin input voltage range	VREF		1.0		3.3	V
MUTE1. 2, 3 L voltage VMUTE-L VMUTE 1, 2, 3 L voltage VMUTE 4 VMUTE 3/V C V MUTE1, 2, 3 L voltage VMUTE 4 VMUTE 3/V C C V MUTE1, 2, 3 L voltage VMUTE 4 VMUTE 3/V C C V MUTE1, 2, 3 L voltage VMUTE 4 VMUTE 3/V C C V MUTE1, 2, 3 L voltage VMUTE 4 VMUTE 4 V C C Immar Shutdown operation TSD Designed target value 10 0 C C NoteD Design guaranee values, not	VREF pin input current	IVCREF	V _C = VREF = 1.65V	-0.2	-0.1		μA
MUTE1, 2, 3 hvoltage VMUTE-H VMUTE = 3V C 60 100 μA MUTE1, 2, 3 input current IMUTE VMUTE = 3V C 60 100 μA Thermal shutdown operation TSD Designed target value 150 180 210 °C Note) Design guarantee values, not measured. 400 Image: C °C Spindle Driver Output saturation voltage V_OSAT_SP Ip =0.5A, Source+Sink 1.8 2.4 V CTL pin input current IVCT_SP V_C = VREF = 1.65V 0.02 0.0.5 μA Control gain GVCD_SP Forward 0.02 0.0.4 0.0.9 V/V Control dead zone width 1 VCD21_SP Forward 0.03 0.4 0.44 V Control dead zone width 2 VCD22_SP Revers -150 -90 mV 0 Current limiter voltage VLIM_SP CX = 0.01µF, VCOIN = 0PEN 0.35 0.455 kHz VCO max frequency FVCOMIN_SP CX = 0.01µF, VCOIN = 5V 36<	MUTE1, 2, 3 L voltage	VMUTE-L				0.5	V
MUTE 1, 2, 3 input current IMUTE VMUTE = $3V$ 60 100 μA Thermal shutdown operation temperature TSD Designed target value 150 180 210 °C Internal shutdown hysteresis width ΔTSD Designed target value 40 °C Notb) Design guarantee values, not ===================================	MUTE1, 2, 3 H voltage	VMUTE-H		2.8		4.5	V
Thermal shutdown operation temperature TSD Designed target value 150 180 210 °C Intermal shutdown hysteresis width Δ TSD Designed target value 40 °C Note) Design guarantee values, not measured. State 40 °C °C Spindle Driver Ottput saturation voltage VO_SAT_SP Ip-0.5A, Source+Sink 1.8 2.4 V CTL pin input voltage range VCT_SP V_C = VREF = 1.65V 0.0 0.2 0.55 µA Control gain GVCO_SP Forward 0.29 0.34 0.39 V/V Control dead zone width 1 VCD2_SP Revers 1.160 -90 mV Current limiter voltage VLM_SP VCOIN = 0 0.36 0.4 0.44 kHz VCOIN input current IVCOMIN_SP CX = 0.01µF, VCOIN = 0PEN 0.38 0.45 0.55 kHz VCO min frequency FVCOMIN_SP CX = 0.01µF, VCOIN = 0PEN 0.38 0.40 44 kHz C1.2 source current tatio RSOURCE_SP <td>MUTE1, 2, 3 input current</td> <td>IMUTE</td> <td>VMUTE = 3V</td> <td></td> <td>60</td> <td>100</td> <td>μΑ</td>	MUTE1, 2, 3 input current	IMUTE	VMUTE = 3V		60	100	μΑ
temperature Image: Control of Contro	Thermal shutdown operation	TSD	Designed target value	150	180	210	°C
Thermal shutdown hysteresis width ATSD Designed target value 40 °C Note) Design guarantee values, not measured. Spindle Driver <	temperature						
Note) Design guarantee values, not measured. Spindle Driver Output saturation voltage V_OSAT_SP I_O =0.5A, Source+Sink 1.8 2.4 V CTL pin input voltage range VCTL_SP V_C = VREF = 1.65V 0.02 -0.2 -0.5 µA Control gain GVCO_SP 0.29 0.34 0.39 V/V Control dead zone width 1 VCDZ_SP Forward 490 150 mV Control dead zone width 2 VCDZ_SP Revers -150 -90 mV Control dead zone width 2 VCDZ_SP Revers -150 -90 mV Current limiter voltage VLIM_SP VCOIN = 3V 1 µA VCO nin frequency FVCOMIN_SP CX = 0.01µF, VCOIN = 0PEN 0.35 0.45 0.55 kHz VCO max frequency FVCOMIN_SP CX = 0.01µF, VCOIN = 5V 36 40 444 kHz C1.2 source current ratio RSINK_SP 1-(CI SOURCE/IC2 SOUCE) -10 10 % % C12 source,	Thermal shutdown hysteresis width	ΔTSD	Designed target value		40		°C
Spinle Driver Output saturation voltage $V_{O}SAT_SP$ $I_{O}=0.5A$, Source+Sink I 1.8 2.4 V CTL pin input voltage range VCTL_SP VCT 0 5 V CTL pin input voltage range VCTL_SP V_C = VREF = 1.85V -0.2 -0.5 μ A Control gain GVCO_SP 0.29 0.34 0.39 V/V Control dead zone width 1 VCD2_SP Forward +90 150 mV Control dead zone width 2 VCD2_SP Revers -150 -90 mV Current limiter voltage VLIM_SP VCOIN = 3V - 1 μ A VCO Onin frequency FVCOMIN_SP CX = 0.01 μ F, VCOIN = OPEN 0.35 0.45 0.55 kHz VCO max frequency FVCOMAX_SP CX = 0.01 μ F, VCOIN = SV 36 40 44 kHz C1.22 source current ratio RSINK_SP 1-(IC1 SOURCE/IC2 SINK) -10 10 % C1.22 source, sink current ratio RC1_SP IC1 SOURCE/IC2 SINK	Note) Design guarantee values, not r	neasured.					
Output saturation voltage V_0SAT_SP $I_0 = 0.5A$, Source+Sink 1.8 2.4 V CTL pin input voltage range VCTL_SP 0 5 V CTL pin input voltage range VCTL_SP V_C = VREF = 1.65V -0.2 -0.5 μA Control gain GVCO_SP Porvard 1.90 0.34 0.39 V/V Control dead zone width 1 VCD2L_SP Forward 4.90 150 mV Control dead zone width 2 VCD2_SP Revers -1.15 -9.0 mV Current limiter voltage VLIM_SP VCOIN = 3V 0.36 0.44 0.44 VCO min frequency FVCOMIN_SP CX = 0.01 μ F, VCOIN = 0PEN 0.35 0.45 0.55 kHz VCO max frequency FVCOMAX_SP CX = 0.01 μ F, VCOIN = 5V 36 40 44 kHz C1,C2 source current ratio RSOURCE_SP 1-(ICI SOURCE/IC2 SOUCE) -10 10 % C1,C2 source sink current ratio RC1_SP ICI SOURCE/IC2 SINK 40 60 %	Spindle Driver		l .				
CTL pin input voltage range VCT_SP 0 5 V CTL pin input current IVCT_SP $V_C = VREF = 1.65V$ 0.29 0.34 0.39 V/V Control gain GVCO_SP 0.29 0.34 0.39 V/V Control dead zone width 1 VCDZ1_SP Forward 1.90 mV Control dead zone width 2 VCDZ2_SP Revers -150 9.90 mV Current limiter voltage VLIM_SP VCOIN = $3V$ 0.36 0.4 V VCOIN input current IVCOIN_SP VCS = 0.01μ F, VCOIN = $0PEN$ 0.35 0.45 0.55 KHz VCO max frequency FVCOMAX_SP CX = 0.01μ F, VCOIN = $0PEN$ 0.35 0.45 0.55 KHz VCO max frequency FVCOMAX_SP CX = 0.01μ F, VCOIN = $0V$ 0.35 0.45 0.55 KHz VCO max frequency FVCOMAX_SP CX = 0.01μ F, VCOIN = $5V$ 3.6 400 44 kHz C1,2 sink current ratio RSINK_SP $1.(IC1 SINK/IC$	Output saturation voltage	V _O SAT_SP	I _O =0.5A, Source+Sink		1.8	2.4	V
CTL pin input current IVCTL_SP V _C = VREF = 1.65V -0.2 -0.2 -0.5 μA Control gain GVCO_SP 0.29 0.34 0.39 V/V Control dead zone width 1 VCDZ1_SP Forward 490 150 mV Control dead zone width 2 VCDZ2_SP Revers -150 -9.0 mV Current limiter voltage VLIM_SP VCOIN = 3V 0.36 0.4 0.44 V VCOIN input current IVCOIN_SP VCOIN = 3V 0.36 0.45 0.55 kHz VCO min frequency FVCOMIN_SP CX = 0.01 μ F, VCOIN = OPEN 0.36 0.45 0.55 kHz VCO max frequency FVCOMAX_SP CX = 0.01 μ F, VCOIN = 5V 36 40 44 kHz C1,C2 source current ratio RSOURCE_SP 1-(IC1 SOURCE/IC2 SOUCE) -10 10 % C1 source, sink current ratio RC1_SP IC2 SOURCE/IC2 SINK 40 60 % C2 source, sink current ratio RC2_SP FGO resistance 20kQ, 5V pull-up <td>CTL pin input voltage range</td> <td>VCTL_SP</td> <td></td> <td>0</td> <td></td> <td>5</td> <td>V</td>	CTL pin input voltage range	VCTL_SP		0		5	V
Control gain GVCO_SP 0.29 0.34 0.39 V/V Control dead zone width 1 VCDZ1_SP Forward +90 150 mV Control dead zone width 2 VCDZ2_SP Revers -150 -90 mV Current limiter voltage VLIM_SP Revers -150 -90 MV Current limiter voltage VLIM_SP Revers -150 -90 MV VCOIN input current IVCOIN_SP VCOIN = 3V 0.36 0.4 0.44 V VCOIN input current IVCOIN_SP CX = 0.01µF, VCOIN = OPEN 0.35 0.45 0.55 kHz VCO max frequency FVCOMAX_SP CX = 0.01µF, VCOIN = 5V 36 40 44 kHz C1,c2 source current ratio RSURCE_SP 1-(IC1 SUNCE/IC2 SUNCE) -10 10 % C1,c2 sink current ratio RSINK_SP 1-(IC1 SUNCE/IC2 SINK 40 60 % C2 source, sink current ratio RC1_SP IC1 SOURCE/IC2 SINK 40 64 %	CTL pin input current	IVCTL_SP	V _C = VREF = 1.65V		-0.2	-0.5	μΑ
Control dead zone width 1 VCDZ1_SP Forward +90 150 mV Control dead zone width 2 VCDZ2_SP Revers 150 90 mV Current limiter voltage VLIM_SP Revers 150 0.36 0.44 0.44 V VCOIN input current IVCOIN_SP VCOIN = 3V 0.35 0.45 0.55 kHz VCO min frequency FVCOMIN_SP CX = 0.01µF, VCOIN = OPEN 0.35 0.45 0.55 kHz VCO max frequency FVCOMAX_SP CX = 0.01µF, VCOIN = 5V 36 400 44 kHz C1,C2 source current ratio RSOURCE_SP 1-(IC1 SOURCE/C2 SOUCE) -10 10 % C1 source, sink current ratio RC1_SP IC1 SOURCE/IC2 SINK 400 60 % C2 source, sink current ratio RC2_SP IC2 SOURCE/IC2 SINK 400 60 % FGO pin L voltage FGOL_SP FGO resistance 20kΩ, 5V pull-up 4.8 V V FR pin input voltage range VFR SO	Control gain	GVCO_SP		0.29	0.34	0.39	V/V
Control dead zone width 2 VCDZ2_SP Revers -150 -90 mV Current limiter voltage VLIM_SP 0.36 0.4 0.44 V VCOIN input current IVCOIN_SP VCOIN = 3V 0.35 0.45 0.55 kHz VCO min frequency FVCOMIN_SP CX = 0.01 μ F, VCOIN = OPEN 0.35 0.45 0.44 kHz C1.C2 source current ratio RSOURCE_SP 1-(IC1 SOURCE/IC2 SOUCE) -10 10 % C1.22 sink current ratio RSINK_SP 1-(IC1 SOURCE/IC2 SINK) -100 100 % C1 source, sink current ratio RC1_SP IC1 SOURCE/IC2 SINK 400 600 % C2 source, sink current ratio RC2_SP IC2 SOURCE/IC2 SINK 400 600 % FGO pin H voltage FGOL_SP FGO resistance 20kQ, 5V pull-up 4.8 V V FR pin input voltage range VFR FGO resistance 20kQ, 5V pull-up 0.15 0.4 V FR pin input voltage range VFR IFR = 3V 0 1.5	Control dead zone width 1	VCDZ1_SP	Forward		+90	150	mV
Current limiter voltage VLIM_SP VCOIN = 3V 0.36 0.4 0.44 V VCOIN input current IVCOIN_SP VCOIN = 3V 0.35 0.45 0.55 kHz VCO min frequency FVCOMIN_SP CX = 0.01 μ F, VCOIN = OPEN 0.35 0.45 0.55 kHz VCO max frequency FVCOMAX_SP CX = 0.01 μ F, VCOIN = 5V 36 40 44 kHz C1,C2 source current ratio RSOURCE_SP 1-(IC1 SOURCE/IC2 SOUCE) -10 10 % C1,c2 sink current ratio RC1_SP IC1 SOURCE/IC1 SINK 40 60 % C2 source, sink current ratio RC1_SP IC1 SOURCE/IC2 SINK 40 60 % C2 source, sink current ratio RC1_SP IC1 SOURCE/IC2 SINK 40 0 60 % FGO pin H voltage FGOH_SP FGO resistance 20kΩ, 5V pull-up 4.8 V V FR pin input voltage range VFR VFR = 3V 0 5 V FR pin input current IFR VFR = 3V 1	Control dead zone width 2	VCDZ2_SP	Revers	-150	-90		mV
VCOIN input current IVCOIN_SP VCOIN = 3V Image: first state sta	Current limiter voltage	VLIM_SP		0.36	0.4	0.44	V
VCO min frequency FVCOMIN_SP CX = 0.01 μ F, VCOIN = OPEN 0.35 0.45 0.55 kHz VCO max frequency FVCOMAX_SP CX = 0.01 μ F, VCOIN = 5V 36 40 444 kHz C1,C2 source current ratio RSOURCE_SP 1-(IC1 SOURCE/IC2 SOUCE) -10 10 % C1,C2 sink current ratio RSINK_SP 1-(IC1 SINK/IC2 SINK) -10 10 % C1 source, sink current ratio RC1_SP IC1 SOURCE/IC1 SINK 40 60 % C2 source, sink current ratio RC2_SP IC2 SOURCE/IC2 SINK 40 60 % FGO pin H voltage FGOH_SP FGO resistance 20kQ, 5V pull-up 4.8 V V FGO pin L voltage range VFR FGO resistance 20kQ, 5V pull-up 4.8 V V FR pin input voltage range VFR VFR = 3V 0 5 V Gutput saturation voltage V_OSAT_3 I_O = 0.3A, Source+Sink 1.5 1.8 V Input voltage range V _{IN} 3 V _{IN} = VREF = 1.65V -0.5	VCOIN input current	IVCOIN_SP	VCOIN = 3V			1	μA
VCO max frequency FVCOMAX_SP CX = 0.01μ F, VCOIN = 5V 36 40 44 kHz C1,C2 source current ratio RSOURCE_SP 1-(IC1 SOURCE/IC2 SOUCE) -10 10 % C1,C2 sink current ratio RSINK_SP 1-(IC1 SINK/IC2 SINK) -10 10 % C1 source, sink current ratio RC1_SP IC1 SOURCE/IC1 SINK 40 60 % C2 source, sink current ratio RC2_SP IC2 SOURCE/IC2 SINK 40 60 % G0 pin H voltage FGOH_SP FGO resistance 20kQ, 5V pull-up 4.8 V V FGO pin L voltage FGOL_SP FGO resistance 20kQ, 5V pull-up 4.8 V V FR pin input voltage range VFR FGO resistance 20kQ, 5V pull-up 0.15 0.4 V FR pin input current IFR VFR SV 54 100 μ A Input voltage range VIN_S IQ = 0.3A, Source+Sink 1.5 1.5 V CTL pin input current IFR VIN_S VIN = VREF = 1.65V -0.5	VCO min frequency	FVCOMIN_SP	$CX = 0.01 \mu F$, $VCOIN = OPEN$	0.35	0.45	0.55	kHz
C1,C2 source current ratio RSOURCE_SP 1-(IC1 SOURCE/IC2 SOUCE) -10 10 % C1,C2 sink current ratio RSINK_SP 1-(IC1 SINK/IC2 SINK) -10 10 % C1 source, sink current ratio RC1_SP IC1 SOURCE/IC1 SINK 40 60 % C2 source, sink current ratio RC2_SP IC2 SOURCE/IC2 SINK 40 60 % FGO pin H voltage FGOH_SP FGO resistance 20kQ, 5V pull-up 4.8 V V FGO pin L voltage range FGOL_SP FGO resistance 20kQ, 5V pull-up 0.15 0.4 V FR pin input voltage range VFR VFR = 3V 0 55 V Thread driver (AMP3) U 0 1.5 1.8 V Output saturation voltage V _O SAT_3 I _O = 0.3A, Source+Sink 0 1.5 1.8 V Input voltage range V _{IN} 3 I _O = 0.3A, Source+Sink 1.5 1.8 V CTL pin input current I _{IN} 3 V _{IN} = VREF = 1.65V -0.5 -0.1 μ A <	VCO max frequency	FVCOMAX_SP	$CX = 0.01 \mu F$, $VCOIN = 5V$	36	40	44	kHz
C1,C2 sink current ratio RSINK_SP 1-(IC1 SINK/IC2 SINK) -10 10 % C1 source, sink current ratio RC1_SP IC1 SOURCE/IC1 SINK 40 60 % C2 source, sink current ratio RC2_SP IC2 SOURCE/IC2 SINK 40 60 % FGO pin H voltage FGOH_SP FGO resistance $20k\Omega$, $5V$ pull-up 4.8 V V FGO pin L voltage FGOL_SP FGO resistance $20k\Omega$, $5V$ pull-up 0.15 0.4 V FR pin input voltage range VFR FGO resistance $20k\Omega$, $5V$ pull-up 0 55 V FR pin input voltage range VFR VFR = $3V$ 0 54 100 μ A Output saturation voltage V_OSAT_3 I_O = 0.3A, Source+Sink 1.5 1.8 V Input voltage range V _{IN-3} I_O = 0.3A, Source+Sink 0 55 V CTL pin input current I_I_N_3 V_IN = VREF = 1.65V -0.5 -0.1 μ A Current gain GVCO_3 I_OPF_3 Note) -50 0	C1,C2 source current ratio	RSOURCE_SP	1-(IC1 SOURCE/IC2 SOUCE)	-10		10	%
C1 source, sink current ratio RC1_SP IC1 SOURCE/IC1 SINK 40 60 % C2 source, sink current ratio RC2_SP IC2 SOURCE/IC2 SINK 40 60 % FGO pin H voltage FGOH_SP FGO resistance $20k\Omega$, $5V$ pull-up 4.8 0.15 0.4 V FGO pin L voltage FGOL_SP FGO resistance $20k\Omega$, $5V$ pull-up 0.15 0.4 V FR pin input voltage range VFR IC1 SOURCE/IC2 SINK 0 5 V FR pin input current IFGO L_SP FGO resistance $20k\Omega$, $5V$ pull-up 0.15 0.4 V Thread driver (AMP3) VFR VFR = 3V 0 54 100 μ A Output saturation voltage V_OSAT_3 I_O = 0.3A, Source+Sink 1.5 1.8 V Input voltage range V_IN_3 I_O = 0.3A, Source+Sink 0 5 V CTL pin input current I_IN_3 V_IN = VREF = 1.65V -0.5 -0.1 μ A Current gain GVCO_3 I_IO IAS 18.7 19.6 </td <td>C1,C2 sink current ratio</td> <td>RSINK_SP</td> <td>1-(IC1 SINK/IC2 SINK)</td> <td>-10</td> <td></td> <td>10</td> <td>%</td>	C1,C2 sink current ratio	RSINK_SP	1-(IC1 SINK/IC2 SINK)	-10		10	%
C2 source, sink current ratio RC2_SP IC2 SOURCE/IC2 SINK 40 60 % FGO pin H voltage FGOH_SP FGO resistance $20k\Omega$, $5V$ pull-up 4.8 // V FGO pin L voltage FGOL_SP FGO resistance $20k\Omega$, $5V$ pull-up 0.15 0.4 V FR pin input voltage range VFR FGO resistance $20k\Omega$, $5V$ pull-up 0 .5 V FR pin input voltage range VFR VFR 0 .54 100 μ A Thread driver (AMP3) IFR VFR = 3V .54 100 μ A Output saturation voltage V_OSAT_3 I_O = 0.3A, Source+Sink 1.5 1.8 V Input voltage range VIN_3 I_O = 0.3A, Source+Sink 0 .5 V CTL pin input current I_IN_3 V_IN = VREF = 1.65V .0.5 .0.1 μ A Current gain GVCO_3 I_OPF_3 Note) .50 0 .50 mV	C1 source, sink current ratio	RC1_SP	IC1 SOURCE/IC1 SINK	40		60	%
FGO pin H voltage FGOH_SP FGO resistance 20kΩ, 5V pull-up 4.8 ··· V FGO pin L voltage FGOL_SP FGO resistance 20kΩ, 5V pull-up 0.15 0.4 V FR pin input voltage range VFR ··· 0 ··· 55 V FR pin input current IFR VFR VFR = 3V ··· 54 100 µA Thread driver (AMP3) U VFR = 3V ··· 54 100 µA Output saturation voltage V _O SAT_3 I _O = 0.3A, Source+Sink ··· 1.5 1.8 V Input voltage range V _{IN-3} I _O = 0.3A, Source+Sink ··· 1.5 1.8 V CTL pin input current I _{IN-3} I _O = 0.3A, Source+Sink ··· 1.5 1.8 V GUtput voltage range V _{IN-3} I _O = 0.3A, Source+Sink ··· 1.5 1.8 V CTL pin input current I _{IN-3} V _{IN} = VREF = 1.65V ··· ··· µA Current gain GVCO_3 <td< td=""><td>C2 source, sink current ratio</td><td>RC2_SP</td><td>IC2 SOURCE/IC2 SINK</td><td>40</td><td></td><td>60</td><td>%</td></td<>	C2 source, sink current ratio	RC2_SP	IC2 SOURCE/IC2 SINK	40		60	%
FGO pin L voltage FGOL_SP FGO resistance 20kΩ, 5V pull-up 0.15 0.4 V FR pin input voltage range VFR VFR = 3V 0 54 100 μ A FR pin input current IFR VFR = 3V 0 54 100 μ A Thread driver (AMP3) U 0.55 1.5 1.8 V Output saturation voltage V ₀ SAT_3 I ₀ = 0.3A, Source+Sink 0 1.5 1.8 V Input voltage range V _{1N-3} I ₀ = 0.3A, Source+Sink 0 0 55 V CTL pin input current I _{1N-3} V _{1N} = VREF = 1.65V -0.5 -0.1 μ A Current gain GVCO_3 V _{1N} = VREF = 1.65V -0.5 -0.1 μ A Output offset voltage V ₀ OFF_3 Note) -50 0 50 mV	FGO pin H voltage	FGOH_SP	FGO resistance 20kΩ, 5V pull-up	4.8			V
FR pin input voltage range VFR Image: Constraint of the system of the	FGO pin L voltage	FGOL_SP	FGO resistance 20kΩ, 5V pull-up		0.15	0.4	V
FR pin input current IFR VFR = 3V 54 100 μ A Thread driver (AMP3) Output saturation voltage V ₀ SAT_3 I ₀ = 0.3A, Source+Sink 1.5 1.8 V Input voltage range V _{IN-3} I ₀ = 0.3A, Source+Sink 0 55 V CTL pin input current I _{IN-3} V _{IN} = VREF = 1.65V -0.5 -0.1 μ A Current gain GVCO_3 VoOFF_3 Note) -50 0 50 mV	FR pin input voltage range	VFR		0		5	V
Thread driver (AMP3) Output saturation voltage V_0SAT_3 $I_0 = 0.3A$, Source+Sink 1.5 1.8 V Input voltage range V_{IN-3} 0 5 V CTL pin input current I_{IN-3} $V_{IN} = VREF = 1.65V$ -0.5 -0.1 μA Current gain GVCO_3 17.8 18.7 19.6 dB Output offset voltage V_0OFF_3 Note) -50 0 50 mV	FR pin input current	IFR	VFR = 3V		54	100	μA
	Thread driver (AMP3)						
Input voltage range V _{IN} _3 0 5 V CTL pin input current I _{IN} _3 V _{IN} = VREF = 1.65V -0.5 -0.1 μA Current gain GVCO_3 17.8 18.7 19.6 dB Output offset voltage V _O OFF_3 Note) -50 0 50 mV	Output saturation voltage	V _O SAT_3	I _O = 0.3A, Source+Sink		1.5	1.8	V
CTL pin input current I _{IN_3} V _{IN} = VREF = 1.65V -0.5 -0.1 μA Current gain GVCO_3 17.8 18.7 19.6 dB Output offset voltage V _O OFF_3 Note) -50 0 50 mV	Input voltage range	V _{IN-} 3		0		5	V
Current gain GVCO_3 17.8 18.7 19.6 dB Output offset voltage V _O OFF_3 Note) -50 0 50 mV	CTL pin input current	I _{IN} _3	V _{IN} = VREF = 1.65V	-0.5	-0.1		μΑ
Output offset voltage V _O OFF_3 Note) -50 0 50 mV	Current gain	GVCO_3		17.8	18.7	19.6	dB
	Output offset voltage	V _O OFF_3	Note)	-50	0	50	mV

Continued from preceding page.						
Peremeter	Symbol	O an differen		Ratings		
Parameter	Symbol	Conditions	min	typ	max	Unit
Focusing and tracking drivers (AM	IP1, 2)					
Output saturation voltage	V _O SAT_1	I _O = 0.6A, Source+Sink		1.8	2.2	V
Input voltage range	V _{IN} _1		0		5	V
CTL pin input current	I _{IN} _1	V _{IN} = VREF = 1.65V	-0.5	-0.1		μA
Control gain	GVCO_1		11.6	12.7	13.8	dB
Output offset voltage	V _O OFF_1	Note)	-50	0	50	mV
Loading driver (AMP4)						
Output saturation voltage	V _O SAT_4	I _O = 0.2A, Source+Sink		1.3	1.6	V
Input voltage range	V _{IN} _4		0		5	V
CTL pin input current	I _{IN} _4	V _{IN} = VREF = 1.65V	-0.5	-0.2		μA
Control gain	GVCO_4		17.8	18.7	19.6	dB
Output offset voltage	V _O OFF_4	Note)	-50	0	50	mV
OP-AMP						
Output L voltage	V _O L_5	I _O = 1mA, Sink		0.2	0.4	V
Input voltage range	V _{IN} _5		0		5	V
Input offset voltage	V _I OFF_5		-5	0	5	mV

Note) The pre-OPAMP in the previous stage is used as buffer.

MUTE function	Mode	
MUTE1 : H	SPINDLE : ON	
MUTE2 : H	FOCUS, TRACKING, SLED : ON	
MUTE3 : H	LOADENG : ON	

Package Dimensions

unit : mm (typ) 3278



Pin Assignment



Top view

LA6502



Block Diagram (In certain applications, snubber may be added to the spindle motor coil output.)

Sample Application Circuit (Spindle Block)



Note) The external constant is for reference only and the optimum constant may differ from one motor to another.

Pin Fu	Inction			
Pin No.	Pin name	Function	Pin voltage	Equivalent circuit
22	V _{CC} 1	Power pin to provide the voltage of all other than BTL-AMP1 and 2 output transistors.	4.5 to 13.8	
4	V _{CC} 2	Power pin of the BTL-AMP1 and 2 outputs.	4.5 to 13.8	
28	SGND	GND for all other than output.		
12 13	MGND	Output GND other than spindle		
46	MUTE3	MUTE function control pin. MUTE : $H \Rightarrow$ Motor drive MUTE : $L \Rightarrow$ drive OFF	0V to 4V	
47	MUTE2	"H" is for 2.8V or more. "L" is for 0.5V or less.		
48	MUTE1	MUTE1 : SP MUTE2 : BTL1, 2, 3 MUTE3 : BTL4		
1	AMP2IN+	OP-AMP non-inverted input pin.	0V to 5V	
2	AMP2IN ⁻	OP-AMP inverted input pin.		
3	AMP2OUT	OP-AMP output pin.		
8	OUT2F	BTL-AMP Forward output pin		
7	OUT2R	BTAL-AMP Reverse output pin		
44	AMP1IN+	OP-AMP non-inverted input pin.	0V to 5V	
43	AMP1IN ⁻	OP-AMP inverted input pin.		

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Pin No.	Pin name	Function	Pin voltage	Equivalent circuit
42 10 9	AMP1OUT OUT1F OUT1R	OP-AMP output pin. BTL-AMP Forward output pin. BTL-AMP Reverse output pin.		5V VCC1 VCC2 VCC1 VCC2 VCC2 VCC2 VCC2 VCC2 VCC2 (0) (0) (0) (0) (0) (0) (0) (0)
31	AMP3IN+	OP-AMP non-inverted input pin.	0V to 5V	
32	AMP3IN ⁻	OP-AMP inverted input pin.		
33	AMP3OUT	OP-AMP output pin of previous stage.		
14	OUT3F	BTL-AMP Forward output pin.		
11	OUT3R	BTL-AMP Reverse output pin.		
30	AMP4IN+	non-inverted input pin.	0.3V to 5V	29 300Ω 300
29	AMP4IN⁻	BTL-4ch reference voltage pin	1V to 4V	
16	OUT4F	BTL-AMP Forward output pin.		5V G G G G G G G G
15	OUT4R	BTL-AMP Reverse output pin.		40kg 40kg 40kg 10kg

Continued for	rom preceding pag	ge.	1	
Pin No.	Pin name	Function	Pin voltage	Equivalent circuit
36	AMPIN ⁺	OP-AMP non-inverted input pin. OP-AMP inverted input pin.	0V to 5V	300Ω 36 35 300Ω 35
34	AMPOUT	OP-AMP output pin.		
19	SPUOUT	Spindle motor driver output pin.		Vcc1
18	SPVOUT			
17	SPWOUT			21
21	SPRF	Spindle motor driver output transistor power pin Detects this voltage for constant current control /The current limiter also detects this potential and is activated.		
24	мсом	Spindle motor coil mid-point input pin Detects the coil voltage waveform with reference to this voltage.		V _{CC1} (7)(18)(19) (3) (3) (3) (3) (4) (4) (4) (4) (4) (4) (4) (4) (4) (4
39	SPC1	Spindle triangular wave generating capacitor connection pin With this triangular wave, the coil output waveform is soft switched.		5V 33) VCC1 40) 40) 40)
40	SPC2			

Din No.	om preceding pag	ge.	Pin voltago	Equivalant arouit
38	SPCX	With the value of a capacitor connected between this pin and GND in the spindle VCO circuit, the operation frequency range and minimum operation frequency are determined.	1 in volage	SV SV SV SV SV SV SV SV SV SV
27	SPFC	Frequency characteristics compensation pin. With a capacitor inserted between this pin and GND, oscillation of the current control system closed loop can be stopped.		
25	SPCTL	Spindle speed control pin Control is the constant current control by applying current return from DRS.	0V to 5V	5V 300Ω (25) 7/7
26	VREF	Spindle speed control reference pin BTLAMP internal VREF buffer input pin.	1V to 3.3V	5V 300Ω 300Ω 300Ω 300Ω 300Ω 300Ω 300Ω 300Ω 300Ω 300Ω
41	SPFGO	Spindle motor counter electromotive voltage detection FG output pin (synthesis of three phases)		^{5V} Vcc1 (41) 1 1 1 1 1 1 1 1
37	SPVCOIN	Drum block VCO circuit voltage input pin PCOUT pin voltage is filtered with CR for input.		

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Pin No.	Pin name	Function	Pin voltage	Equivalent circuit
23	FR	Spindle block V-type control switching pin. FR : $H \Rightarrow VREF < SPCTL drive$ FR : $L \Rightarrow VREF < SPCTL drive$ "H" is for 2.8V or more. "L" is for 0.5V or less.	0V to V _{CC} 1	

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