Ordering number : ENN7818

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA6574H — Five-Channel Driver (four BTL channels plus one H bridge channel) for MD and CD Player

Overview

The LA6574H is a motor driver IC for MD and CD players with four BTL channels and one H bridge channel. The LA6574H features a separate power supply for the H bridge block, an output adjustment pin, and a 3.3 V regulator to support a wide range of applications.

Functions and Features

- Four power amplifier channels plus one H bridge channel
- I_O max: 700 mA (each channel)
- Built-in level shifting circuits for the BLT amplifiers
- Thermal protection circuit (Thermal shutdown circuit)
- Separate loading block power supply
- Built-in 3.3 V regulator
- Provides a dedicated pin for adjusting the loading block output.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Allowable power dissipation	Pdmax	Independent IC	0.82	W
		∗ Mounted on a board.	2.0	W
Maximum output current	I_O max	Each channel for CH1 to CH5	0.7	A
Maximum input voltage	VINB		13	V
MUTE pin voltage	VMUTE		13	V
Operating temperature	Topr		–30 to +85	°C
Storage temperature	Tstg		–55 to +150	°C

Note ∗: Mounted on a board (76.1 × 114.3 × 1.6 mm) Material: glass epoxy

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5.6 to 13	V

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N2206 / 81004TN (OT) No.7818-1/7

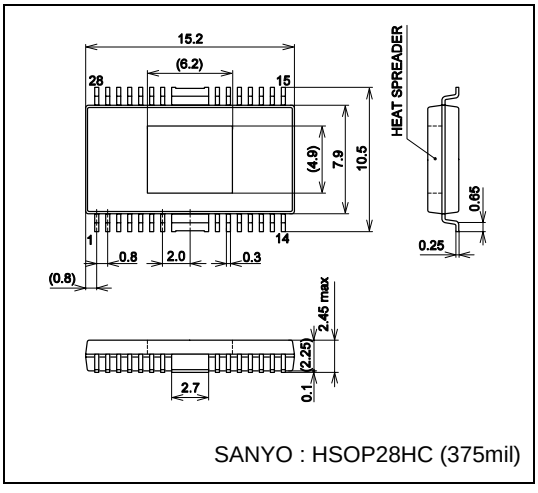
Electrical Characteristics at Ta = 25°C, $V_{CC}1 = V_{CC}2 = 8$ V, VREF = 1.65 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Overall Characteristics]						
No load current drain - ICC on	I_{CC}-ON	All outputs on, FWD = REV = 0 V ∗1		30	50	mA
VREF input voltage range	VREF-IN		1		V_{CC}–1.5	V
[BTL Amplifier Block]						
Output offset voltage	VOFF	BTL amplifiers, the voltage difference across each channel's output	–50		+50	mV
Input voltage range	V_{IN}	Input resistance: 11 kΩ	0		V_{CC}	V
Output voltage	V_O	The voltage between each of the V_O+/V_O– pairs when R_L is 8 Ω. ∗2	4	5		V
Closed loop voltage gain	VG	Gain from input to output		4		Multi-plier
Slew rate	SR	With the amplifier operating independently, twice the value measured between outputs ∗4		0.5		V/µs
[H Bridge Block]						
Output voltage	V_O-LOAD	The voltage between each of the V_O+/V_O– pairs when R_L is 8 Ω. ∗2		6		V
Low-level input voltage	V_{IN}-L				1	V
High-level input voltage	V_{IN}-H		2			V
Output control voltage	VCONT	VCONT = 3 V ∗2		3.5		V
[Regulator Block]						
Output voltage	Vreg	I_L = 100 mA	3.05	3.3	3.55	V
Load regulation	ΔVRL	I_L = 0 to 200 mA	–50	0	+10	mV
Line regulation	ΔVVCC	V_{CC} = 6 to 12 V, I_L = 100 mA	–15	+21	+60	mV

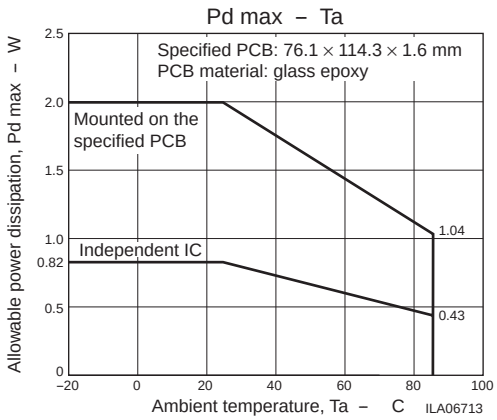
Note ∗1: The total current drain for $V_{CC}1$ and $V_{CC}2$ with no load.
∗2: Voltage difference across the load (8 Ω). With the outputs in the saturated state.
∗3: When the MUTE pin is high, the outputs will be on, and when low, the outputs will be off (high-impedance state).
∗4: Design guarantee value

Package Dimensions

unit: mm
3234B



SANYO : HSOP28HC (375mil)

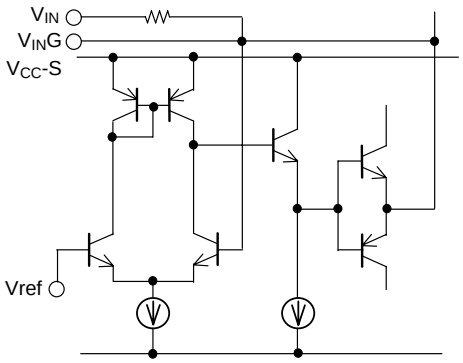
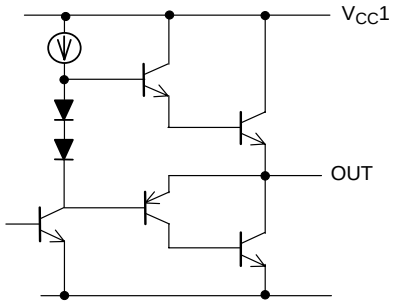
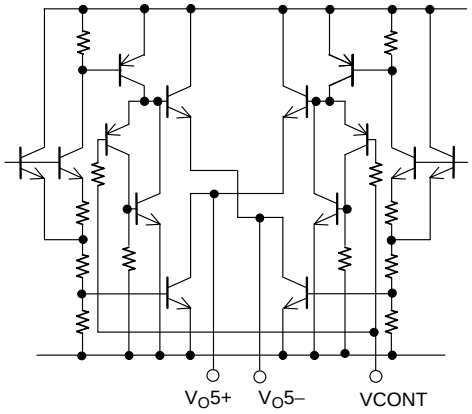
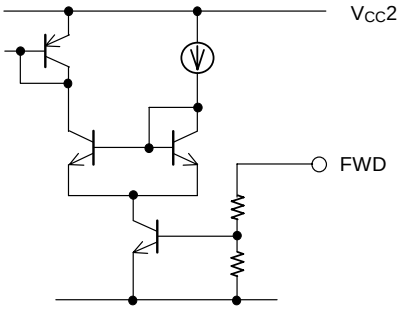


Pin Functions

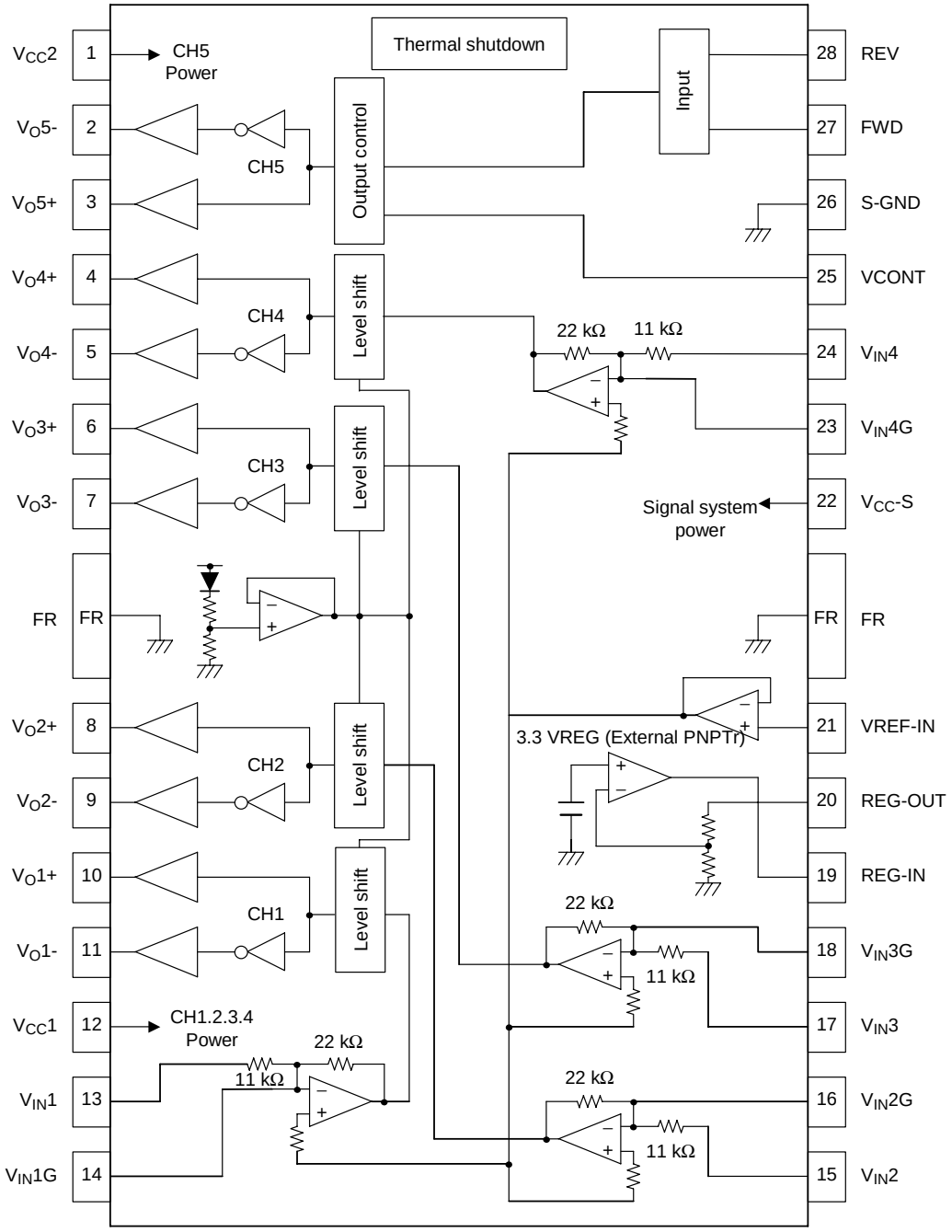
Pin No.	Symbol	Pin descriptions
1	$V_{CC}2$	Channels 3, 4, and 5 power supply (This pin must be shorted to $V_{CC}1$ and V_{CC}–S.)
2	V_O5–	Loading output (–)
3	V_O5+	Loading output (+)
4	V_O4+	Channel 4 output (+)
5	V_O4–	Channel 4 output (–)
6	V_O3+	Channel 3 output (+)
7	V_O3–	Channel 3 output (–)
8	V_O2+	Channel 2 output (+)
9	V_O2–	Channel 2 output (–)
10	V_O1+	Channel 1 output (+)
11	V_O1–	Channel 1 output (–)
12	$V_{CC}1$	Channels 1 and 2 (BTL) power supply (This pin must be shorted to V_{CC}-S and $V_{CC}2$.)
13	$V_{IN}1$	Channel 1 input
14	$V_{IN}1G$	Channel 1 input (gain adjustment input)
15	$V_{IN}2$	Channel 2 input
16	$V_{IN}2G$	Channel 2 input (gain adjustment input)
17	$V_{IN}3$	Channel 3 input
18	$V_{IN}3G$	Channel 3 input (gain adjustment input)
19	REG-IN	Regulator input (external pnp transistor base)
20	REG-OUT	Regulator output (external pnp transistor collector)
21	VREF-IN	Reference voltage input
22	V_{CC}-S	Signal system power supply (This pin must be shorted to $V_{CC}1$ and $V_{CC}2$.)
23	$V_{IN}4G$	Channel 4 input (gain adjustment input)
24	$V_{IN}4$	Channel 4 input
25	VCONT	Channel 5 (VLO) output voltage control
26	S-GND	Signal system ground
27	FWD	Channel 5 (VLO) output switching (FWD); loading block logic input
28	REV	Channel 5 (VLO) output switching (REV); loading block logic input

Note: • The center frame (FR) is used as the power system ground. Along with the signal system ground (S-GND), this level must be the lowest potential in the system.
• The three power supply pins V_{CC}–S, $V_{CC}1$, and $V_{CC}2$ must be shorted together externally.

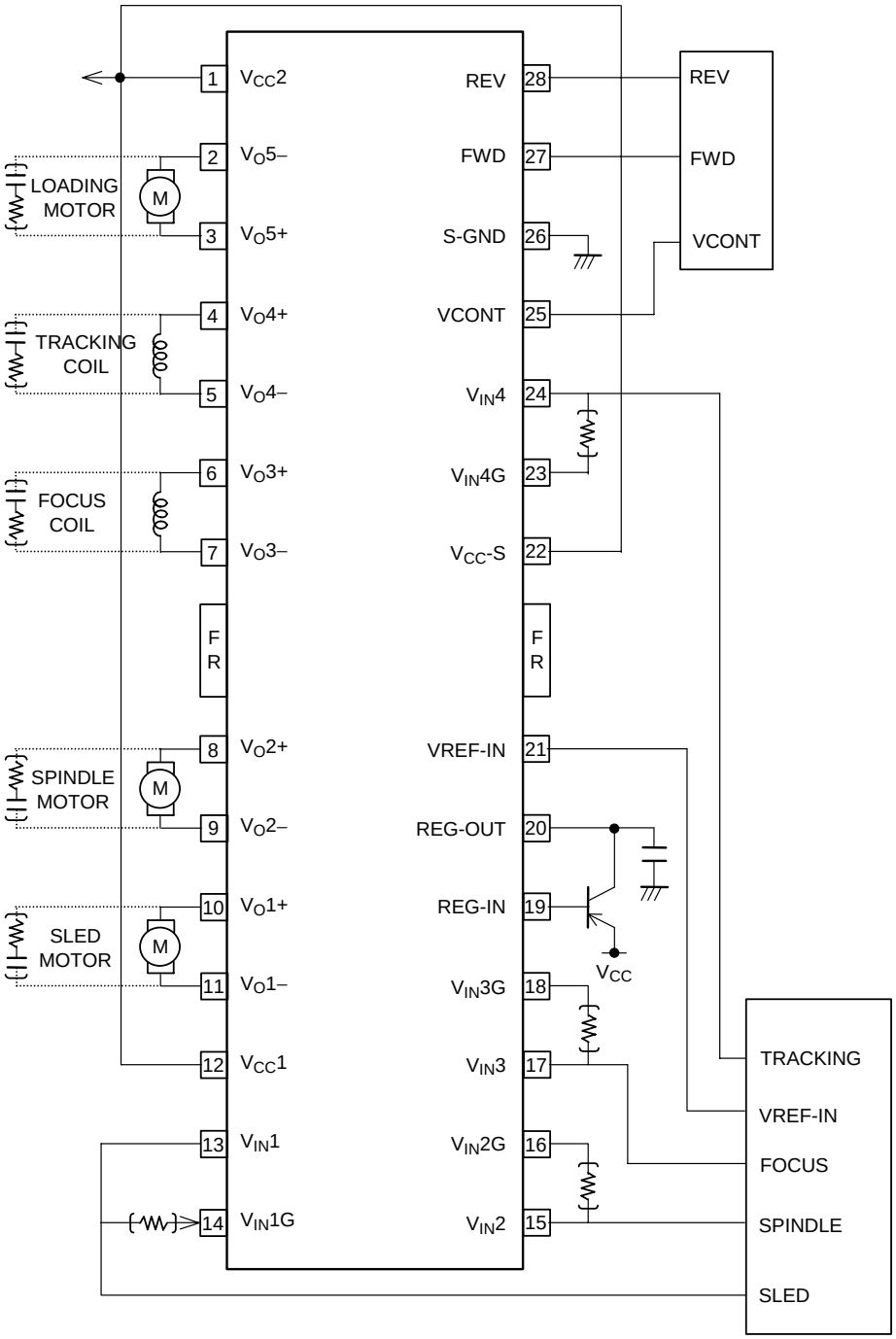
Pin Functions

Pin No.	Symbol	Pin name	Pin description	Equivalent circuit
13 14 15 16 17 18 23 24	V_{IN}	Inputs	Inputs	
4 5 6 7 8 9 10 11	V_O	Outputs	Outputs	
2 3 25	V_O5+ V_O5- VCONT	V_O5	H bridge outputs	
27 28	FWD REV	FWD REV	H bridge inputs	

Block Diagram



Sample Application Circuit



H Bridge Block

FWD	REV	V_O5+	V_O5-	Mode
L	L	OFF	OFF	Open ∗1
L	H	H	L	Forward
H	L	L	H	Reverse
H	H	L	L	Brake ∗2

Note ∗1: The output are in the high-impedance state in this mode

∗2: In brake mode, the sink side transistors are on (short-circuit braking). The VLO+ and VLO– levels go to a level essentially the same as the ground level.

∗3: VCONT (output voltage setting pin) and VLO have the following relationship: VLO = VCONT – 1 V (typical)

Relationship between the MUTE pin and the power supplies (V_{CC}*)