



SANYO Semiconductors

# DATA SHEET

## LA6546H — Monolithic Linear IC For Compact Disk Four-Channel Bridge (BTL) Driver

### Overview

The LA6546H is a 4-channel bridge (BTL) driver for CD players.

### Functions

- Bridge-connection (BTL) power amplifier 4-channel.
- $I_O$  max 700mA
- Operation-amplifier built-in
- MUTE circuit built-in (operable for all channels)
- 5V power supply built-in (with external PNP output)
- Reset circuit built-in (reset output delay time set with the external capacitor)

### Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$ max		14	V
Allowable power dissipation	$P_d$ max	Measure with a designated substrate*	2.34	W
Maximum input voltage	$V_{INB}$		13	V
MUTE pin voltage	$V_{MUTE}$		13	V
Operating temperature	$T_{opr}$		-30 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

\* Specified board size :  $76.1 \times 114.3 \times 1.6\text{mm}^3$ , glass epoxy.

Recommended Operating Conditions at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Operating voltage	$V_{CC}$		5.6 to 13	V
Reset output source current	$I_{ORH}$		0 to 200	$\mu\text{A}$
Reset output sync current	$I_{ORL}$		0 to 2	mA

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# LA6546H

**Electrical Characteristics** at  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 8\text{V}$ ,  $V_{REF} = 2.5\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>Overall</b>						
No-load current drain 1	$I_{CC1}$	All amp outputs ON (MUTE HI) *1		20	40	mA
No-load current drain 2	$I_{CC2}$	All amp outputs OFF (MUTE LOW) *1		15	35	mA
Output offset voltage 1	$V_{OF1}$	CH1 ( $V_{O1+}$ and $V_{O1-}$ ), CH2 ( $V_{O2+}$ and $V_{O2-}$ )	-50		50	mV
Output offset voltage 2	$V_{OF1}$	CH3 ( $V_{O3+}$ and $V_{O3-}$ ), CH4 ( $V_{O4+}$ and $V_{O4-}$ )	-50		50	mV
VREF input voltage range	$I_{BIN}$		1.5		$V_{CC}-1.5$	V
Output voltage	$V_O$	$R_L = 8.0\Omega$ *1	4.0	4.7		V
Closed-circuit voltage gain	VG			9		dB
Slew rate	SR			0.15		V/ $\mu\text{s}$
MUTE ON voltage	VMUTE			1.2		V
<b>5V power block</b> (PNP Tr 2SB632K used externally)						
Output voltage	$V_{OUT1}$	$I_O = 200\text{mA}$	4.75	5.0	5.25	V
Line regulation	$\Delta V_{OLN1}$	$5.6\text{V} \leq V_{IN1} \leq 12\text{V}$		20	100	mV
Load regulation	$\Delta V_{OLD1}$	$5\text{mA} \leq I_O \leq 200\text{mA}$		50	150	mV
<b>Reset block</b>						
H reset output voltage	$V_{ORH}$	$I_{ORH} = 200\mu\text{A}$ , CD Pin open	4.73	4.98	5.23	V
L reset output voltage	$V_{ORL}$	$I_{ORL} = 2\text{mA}$ , CD-GND short-circuited		100	200	mV
Reset threshold voltage	$V_{RT}$	*3		4.3		V
Reset hysteresis voltage	$V_{HYS}$	*4	40	100	200	mV
Reset output delay time	$t_d$	$C_d = 0.1\mu\text{F}$		10		ms
<b>Pre-amplifier block</b>						
Output offset voltage	$V_{OFF-OP}$		-7	0	7	mV
Input voltage range	$V_{IN-OP}$		1.5		$V_{CC}-1.5$	V
Output voltage SOURCE	VSOURCE-OP			1.2		V
Output voltage SYNC	VSINK-OP			0.5		V

Note \*1 : Voltage across both ends of  $8\Omega$  load inserted between outputs. Input = H or L.

The output is in the saturation condition.

\*2 : The output is ON with MUTE = H and OFF with MUTE = L. MUTE is operable for all channels.

With MUTE = L, the output is OFF and the impedance is HI.

\*3 : 5V supply voltage when the reset output is LOW.

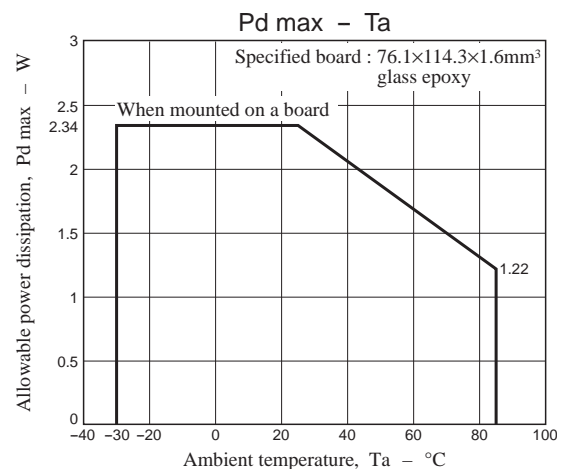
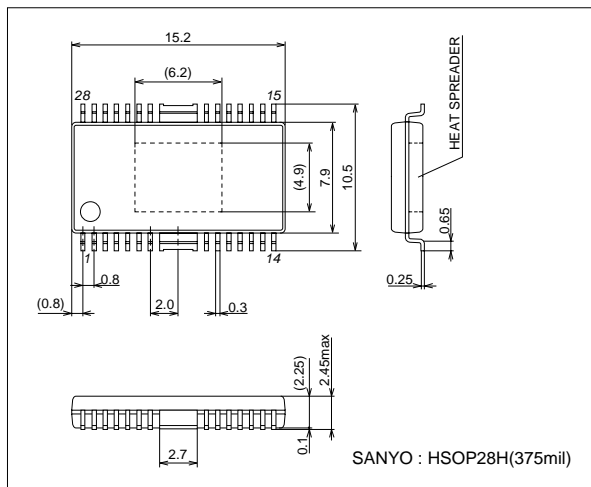
\*4 : Potential difference of 5V supply voltage between the reset output at LOW and at HI.

Hysteresis width.

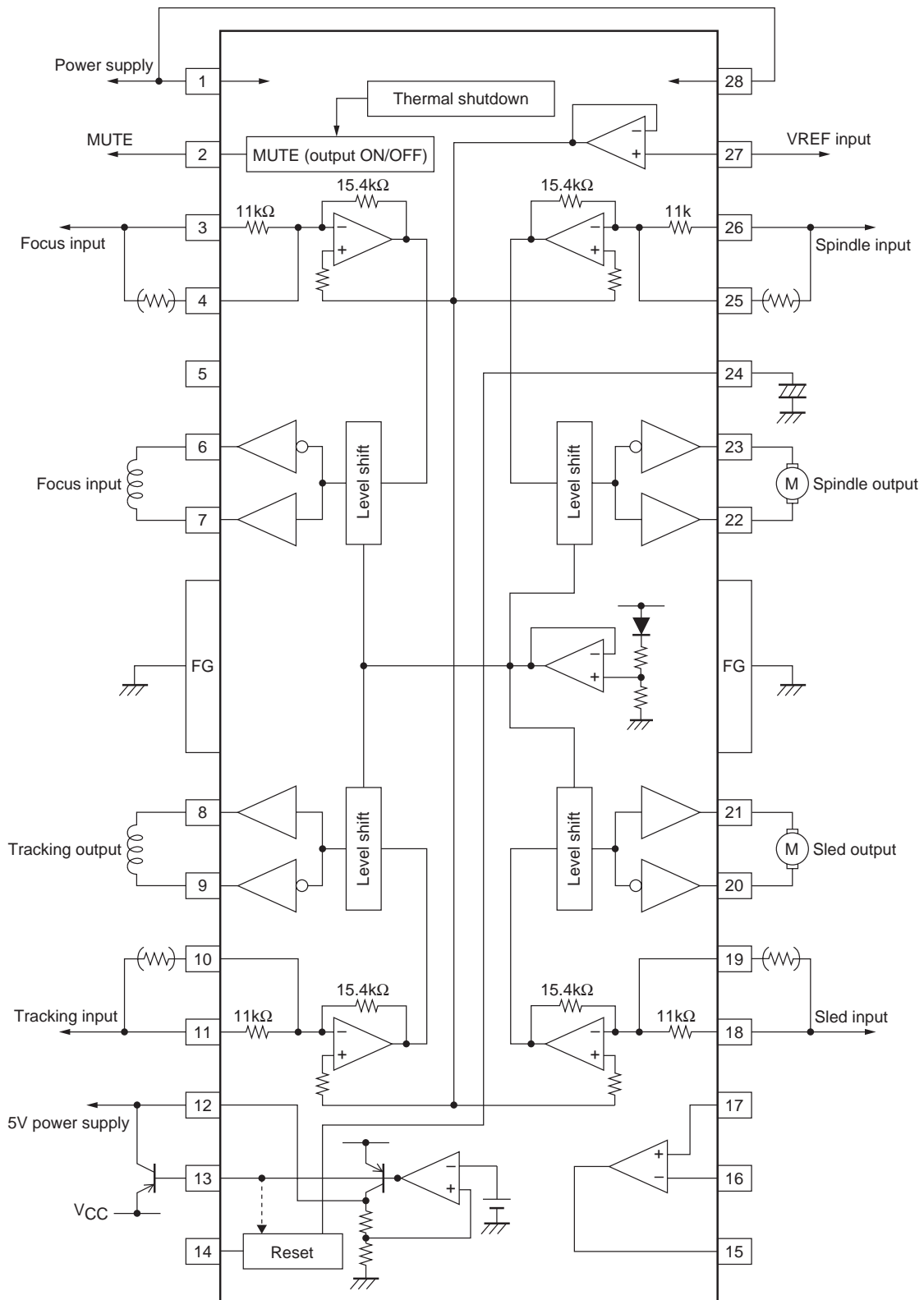
## Package Dimensions

unit : mm (typ)

3233B



Block Diagram and Sample Application Circuit



# LA6546H

## Pin Functions

Pin No.	Symbol	Pin descriptions
1	$V_{CC1}$	Substrate (Lowest potential)
2	MUTE	Output ON/OFF. Operable for all channels
3	$V_{IN1}$	CH1 input pin
4	VG1	CH1 input pin (for gain control)
5	(NC)	Do not use
6	$V_{O1+}$	CH1 output pin (+)
7	$V_{O1-}$	CH1 output pin (-)
8	$V_{O2-}$	CH2 output pin (-)
9	$V_{O2+}$	CH2 output pin (+)
10	VG2	CH2 input pin (for gain control)
11	$V_{IN2}$	CH2 input pin
12	REG-OUT	Connect collector of the external transistor (PNP), 5V power output
13	REG-IN	Connect base of the external transistor (PNP)
14	$\overline{RES}$	Reset output
15	$V_{OUT}$	OP-AMP output pin
16	$V_{IN-}$	OP-AMP input pin (-)
17	$V_{IN+}$	OP-AMP input pin (+)
18	$V_{IN3}$	CH3 input pin
19	VG3	CH3 input pin (for gain control)
20	$V_{O3+}$	CH3 output pin (+)
21	$V_{O3-}$	CH3 output pin (-)
22	$V_{O4-}$	CH4 output pin (-)
23	$V_{O4+}$	CH4 output pin (+)
24	CD	Reset output delay time setting (with external capacitor)
25	VG4	CH4 input pin (for gain control)
26	$V_{IN4}$	CH4 input pin
27	VREF	Application of the reference voltage
28	$V_{CC2}$	Power supply (short-circuit with pin 1)

Note : Set GND (minimum potential) the middle frame and connect both of them.

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## Pin Description

Pin No.	Symbol	Pin function	Description	Equivalent circuit
3 11 18 26 4 10 19 25	$V_{IN1}$ $V_{IN2}$ $V_{IN3}$ $V_{IN4}$ $VG1$ $VG2$ $VG3$ $VG4$	Input	Each input pin	
6, 7 8, 9 20, 21 22, 23	$V_{O1+}$ , $V_{O1-}$ $V_{O2+}$ , $V_{O2-}$ $V_{O3+}$ , $V_{O3-}$ $V_{O4+}$ , $V_{O4-}$	Output	Each output pin	
2	MUTE	MUTE	MUTE (output ON/OFF)	

## Truth Table

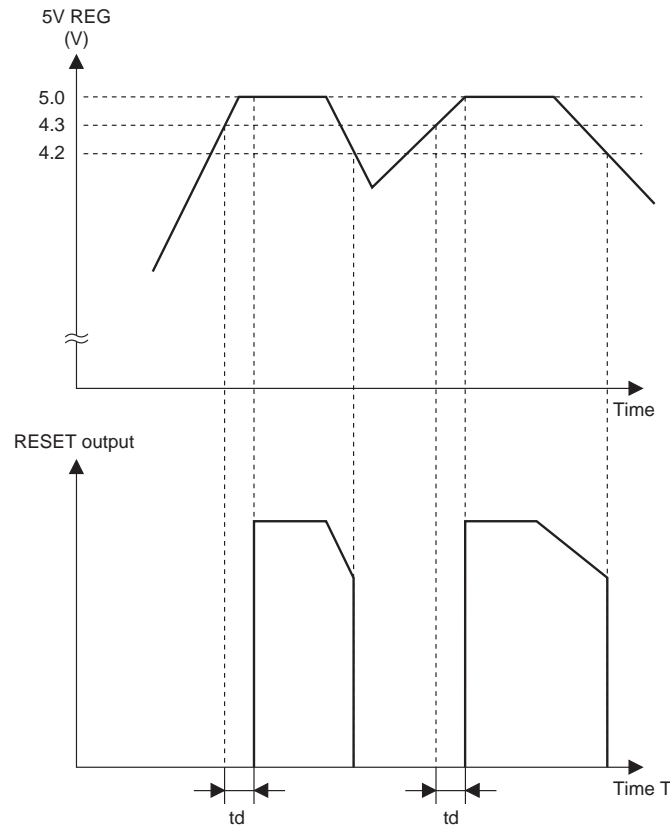
Input	MUTE	CH1		CH2		CH3		CH4	
		$V_{O1+}$	$V_{O1-}$	$V_{O2+}$	$V_{O2-}$	$V_{O3+}$	$V_{O3-}$	$V_{O4+}$	$V_{O4-}$
H	H	H	L	L	H	H	L	L	H
	L	-	-	-	-	-	-	-	-
L	H	L	H	H	L	L	H	H	L
	L	-	-	-	-	-	-	-	-

\* - : High-impedance

## Gain setting

For gain setting, refer to the block diagram. When setting the gain with the VG\* terminal, the total gain has more or less temperature characteristics due to difference in temperature characteristics between internal and external resistors. Use the  $V_{IN}^*$  terminal to set the gain.

## Reset operation



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