Ordering number : ENN6296

Monolithic Linear IC

LA6545M

Four-Channel Bridge (BTL) Driver for CD-ROM

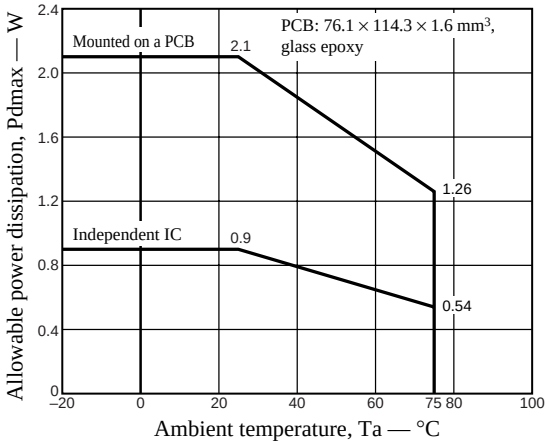
Overview

The LA6545M is a 4-channel bridge (BTL) driver developed for use in CD-ROM systems.

Functions

- Bridge connected (BTL) four-channel power amplifier
- V_{CE} (residual voltage) minimized (channels 1 and 2) by using two power supplies.
- $I_O$max: 1.0 A
- Muting circuit provided (output on/off control) (MUTE pin: low for output off, high for output on. MUTE1: controls channels 1, 2, and 3, MUTE2: controls channel 4.)
- Thermal protection (shutdown) circuit
- Separated output stage power supply (VS1: channels 1 and 2, VS2: channels 3 and 4)

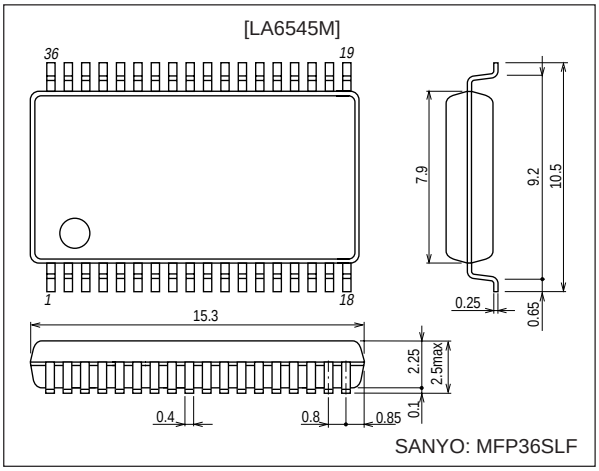
Pd max — Ta



Package Dimensions

unit: mm

3129-MFP36SLF



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_{CC} max	$V_{CC} \geq V_S1, 2$	14	V
Maximum supply voltage 2	V_S max	$V_S1, 2, V_{CC} \geq V_S1, 2$	14	V
Input voltage	V_{IN} max	Each of the input pins $V_{IN}1$ to $V_{IN}4$	13	V
MUTE pin voltage	V_{MUTE} max		13	V
Allowable power dissipation	Pd max	Independent IC	0.9	W
		Mounted on the specified PCB (76.1 × 114.3 × 1.6 mm³, glass epoxy)	2.1	W
Operating temperature	Topr		–20 to +75	℃
Storage temperature	Tstg		–55 to +150	℃

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage	V_{CC}	$V_{CC} \geq V_S1, 2$	4 to 13	V
	$V_S1, 2$	V_S1 and V_S2 are the output stage power supply. $V_{CC} \geq V_S1$ and V_S2	4 to 13	V

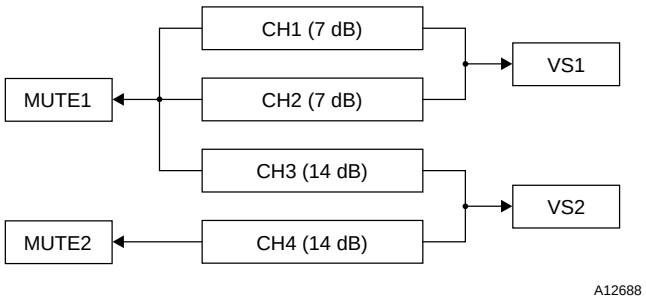
Electrical Characteristics at Ta = 25°C, V_{CC} = V_S2 = 12 V, V_S1 = 5 V, V_{REF} = 1.65 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{CC} no load current drain 1	I_{CC}-ON	Output on (MUTE1 and MUTE2: high), V_{CC}		10	25	mA
V_{CC} no load current drain 2	I_{CC}-OFF	Output off (MUTE1 and MUTE2: low), V_{CC}			4	mA
VS1 no load current drain 1	I_S1-ON	Output on (MUTE1 and MUTE2: high), V_S1		20	30	mA
VS1 no load current drain 2	I_S2-OFF	Output off (MUTE1 and MUTE2: low), V_S1			4	mA
VS2 no load current drain 1	I_S2-ON	Output on (MUTE1 and MUTE2: high), V_S2		20	30	mA
VS2 no load current drain 2	I_S2-OFF	Output off (MUTE1 and MUTE2: low), V_S2			4	mA
Output offset voltage	V_{OF}1 to 4	Potential difference between the + and – outputs for each channel	–50		+50	mV
Input voltage range 1	V_{IN}1	Input voltage range for each channel	0		V_S1	V
Output voltage 1	VO1	I_O = 700 mA, the difference between the outputs for channels 1 and 2	4	4.5		V
Output voltage 2	VO2	I_O = 700 mA, the difference between the outputs for channels 3 and 4	10.5	11		V
Closed circuit voltage gain	VG1	The BTL amplifier voltage gain for channels 1 and 2	5	7	9	dB
	VG2	The BTL amplifier voltage gain for channels 3 and 4	12	14	16	dB
Slew rate	SR	This value is doubled when measured across the outputs. *1		0.5		V/µs
Muting on voltage	V_{MUTE}	MUTE1 and MUTE2. The voltage at which the output turns on. *2		1.5	2	V

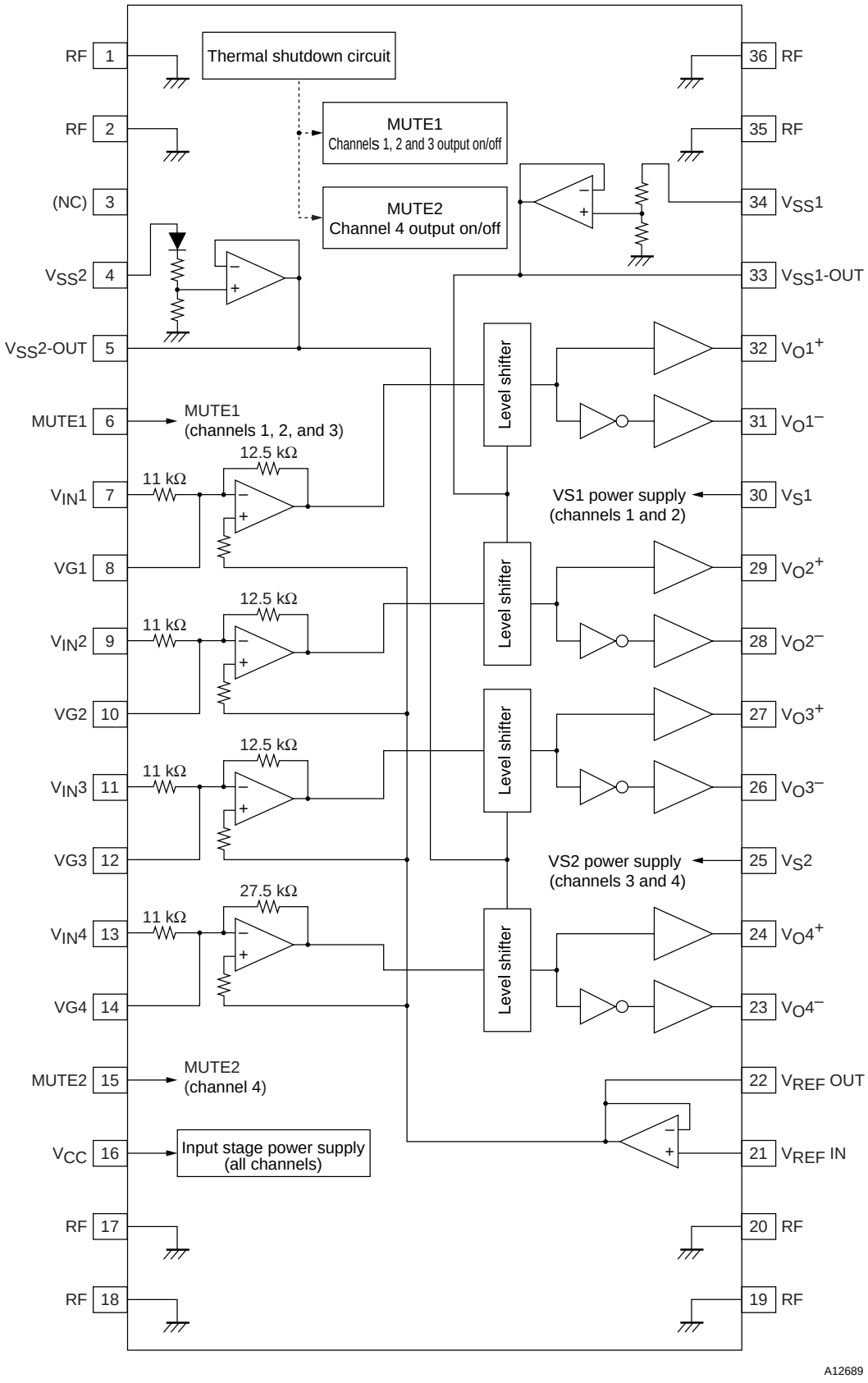
Notes 1. Design guarantee value.

2. The MUTE1, and MUTE2 pins turn the output on when high and off when low. When the output is off, the outputs will be in the high-impedance state.
   The figure below shows the relationship between the channels and the MUTE pins and between the channels and the power supplies.

System Figure



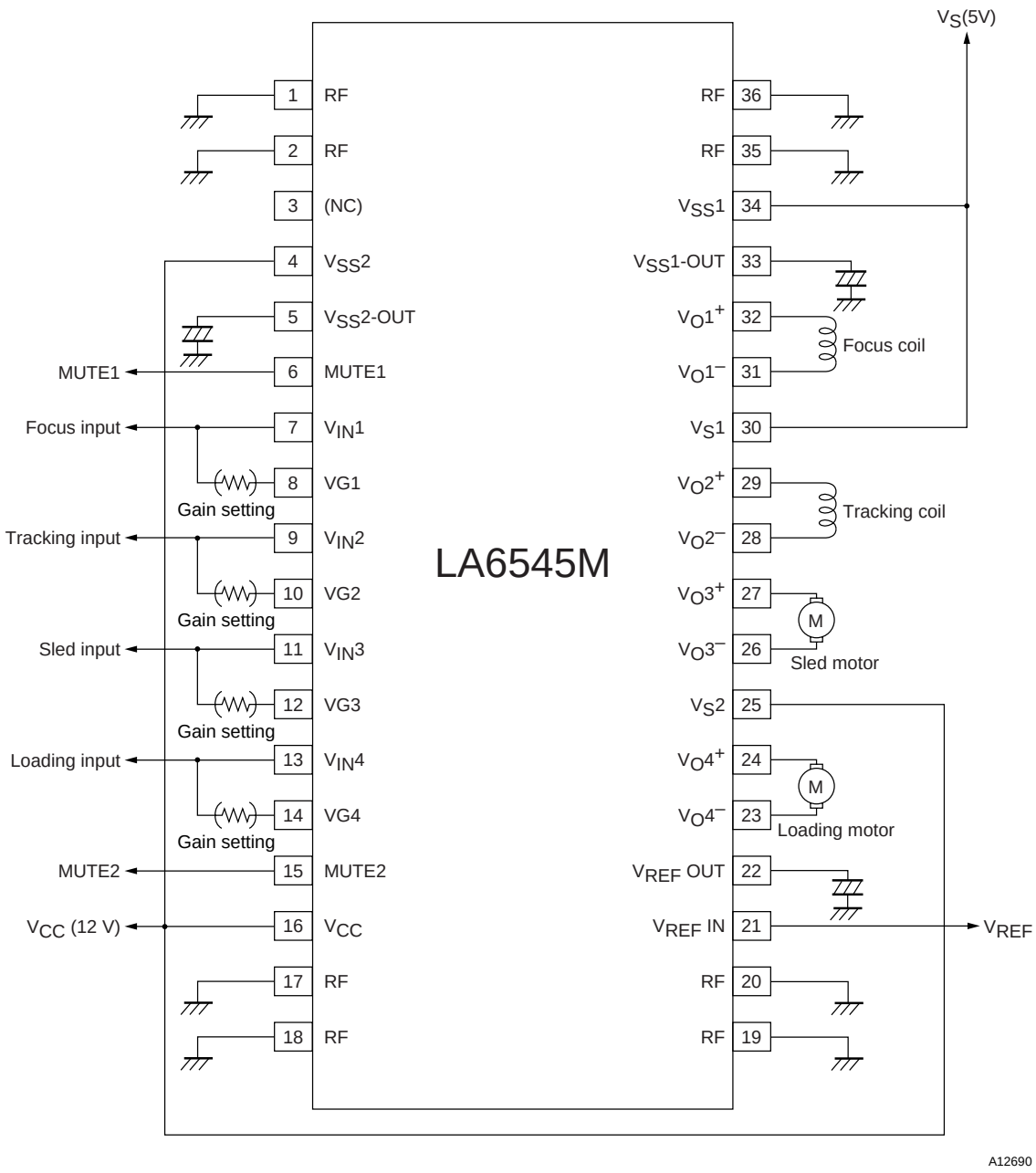
Block Diagram and Pin Assignment



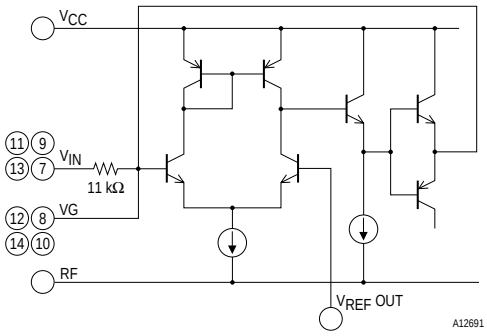
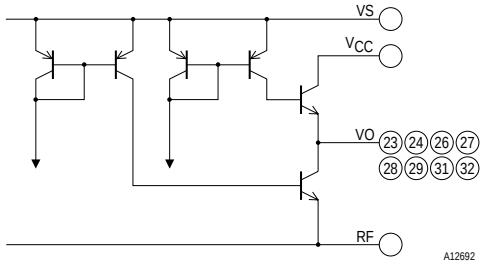
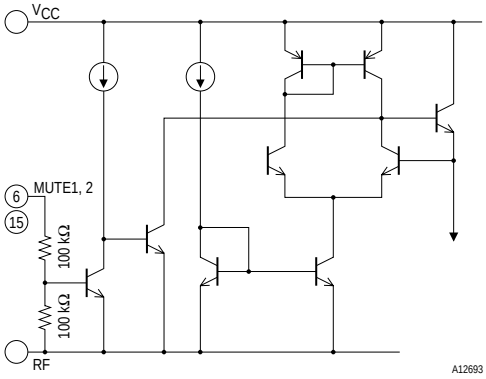
Pin Functions

Pin No.	Pin	Function
1	RF	Substrate (lowest potential)
2	RF	Substrate (lowest potential)
3	(NC)	Unused.
4	$V_{SS}2$	Connect to V_S2.
5	$V_{SS}2$-OUT	Output stage reference voltage output ((V_S2-VBE)/2, typical)
6	MUTE1	Channels 1, 2, and 3 output on/off control
7	$V_{IN}1$	Channel 1 input
8	VG1	Channel 1 input (gain adjustment)
9	$V_{IN}2$	Channel 2 input
10	VG2	Channel 2 input (gain adjustment)
11	$V_{IN}3$	Channel 3 input
12	VG3	Channel 3 input (gain adjustment)
13	$V_{IN}4$	Channel 4 input
14	VG4	Channel 4 input (adjustment)
15	MUTE2	Channel 4 on/off control
16	V_{CC}	Power supply
17	RF	Substrate (lowest potential)
18	RF	Substrate (lowest potential)
19	RF	Substrate (lowest potential)
20	RF	Substrate (lowest potential)
21	V_{REF} IN	Reference voltage input ($V_{REF}1$ buffer amplifier input)
22	V_{REF} OUT	Reference voltage output ($V_{REF}1$ buffer amplifier output)
23	V_O4^-	Channel 4 inverted output
24	V_O4^+	Channel 4 noninverted output
25	V_S2	Channes 3 and 4 output stage power supply
26	V_O3^-	Channel 3 inverted output
27	V_O3^+	Channel 3 noninverted output
28	V_O2^-	Channel 2 inverted output
29	V_O2^+	Channel 2 noninverted output
30	V_S1	Channels 1 and 2 output stage power supply
31	V_O1^-	Channel 1 inverted output
32	V_O1^+	Channel 1 noninverted output
33	$V_{SS}1$-OUT	Output stage reference voltage (Outputs V_{SS}/2: typical) ($V_{REF}2$ buffer amplifier output)
34	$V_{SS}1$	Connect to V_S1. ($V_{SS}1$ - OUT is generated by a resistor divider.)
35	RF	Substrate (lowest potential)
36	RF	Substrate (lowest potential)

Sample Application Circuit



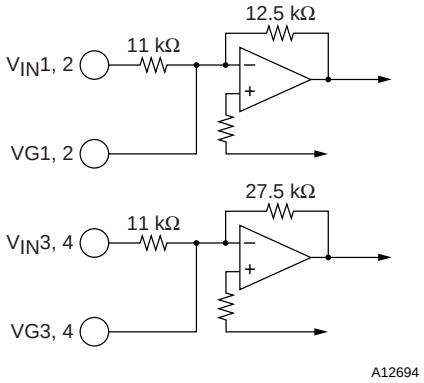
Pin Description

Pin No.	Pin	Symbol	Function	Equivalent circuit
7 8 9 10 11 12 13 14	V_{IN}* VG* (Input)	$V_{IN}1$ VG1 $V_{IN}2$ VG2 $V_{IN}3$ VG3 $V_{IN}4$ VG4	Inputs for each channel	
32 31 29 28 27 26 24 23	V_O* (Output)	V_O1^+ V_O1^- V_O2^+ V_O2^- V_O3^+ V_O3^- V_O4^+ V_O4^-	Outputs for each channel	
6 15	MUTE	MUTE1 MUTE2	Output on/off control	

Gain Setting (Functions of the Input and Gain Adjustment Pins)

The figures present overviews of the V_{IN} and VG pin circuits. (These are the same as the block diagrams.)

1. Consider resistors (11 kΩ, typical) to be inserted between the V_{IN} and VG pins. This should be seen as being the same as the operational amplifier noninverting input (V_{IN}^+).
2. If the VG pins are not used, and only the V_{IN} pins are used, the BTL gain (across the V_O^+ and V_O^- outputs) will be 7 dB for channels 1 and 2 (amplifier units: 1 dB + BTL: 6 dB) and 14 dB for channels 3 and 4 (amplifier units: 8 dB + BTL: 6 dB).
   If the V_{IN} pins are not used and 11 kΩ external resistors are attached to the VG pins, input to the opposite ends of those resistors will result in equivalent circuit operation. However, the V_{IN} pins should be used and the gain set to minimize the I/O gain temperature characteristics.



Offset Voltage

This IC includes built-in level shifting circuits. For input to which V_{REF} is applied as a reference, the output is referenced to the voltage $V_{SS}1/2$ (V) for channels 1 and 2, and the output is referenced to the voltage ($V_{SS}2 - V_{BE}(0.7)$)/2 (V) for channels 3 and 4.