

SANYO**LA6543****4-Channel Bridge (BTL) Driver for CD-ROM****Overview**

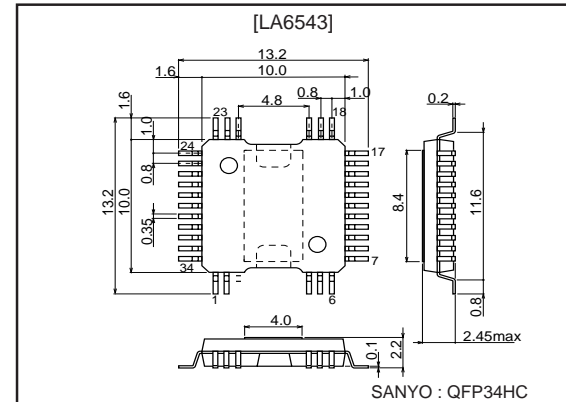
The LA6543 is a 4-channel bridge (BTL) driver developed for CD-ROM applications.

Features and Functions

- Integrated 4-channel power amplifier with bridge circuit (BTL) (two output stage power supply lines)
- I_{Omax} : 1A
- Integrated level shift circuit
- Integrated muting circuit
MUTE: Output OFF at Low, output ON at High.
MUTE1 is for channels 1 and 2, and MUTE2 for channels 3 and 4.
- Integrated thermal shutdown circuit
- Divided output stage power supply (V_{S1} : CH1, CH2, CH3; V_{S2} : CH4)

Package Dimensions

unit: mm

3219-QFP34HC**Specifications****Maximum Ratings at $T_a = 25^\circ\text{C}$**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_{CCmax}		14	V
Maximum supply voltage 2	V_{Smax}	$V_{S1}, 2$	14	V
Maximum input voltage	V_{INmax}	Input pins V_{IN1} to 4	13	V
Mute pin voltage	$V_{MUTEmax}$		13	V
Allowable power dissipation	$P_d max$	IC only	0.77	W
Operating temperature	T_{opr}		-20 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operation voltage 1	V_{CC}		4 to 13	V
Recommended operation voltage 2-1	V_{S1}	V_{S1} : CH1 to CH3	4 to 13	V
Recommended operation voltage 2-2	V_{S2}	V_{S2} : CH4 output reference power supply	4 to 13	V

* $V_{CC} \geq V_{S1}, 2$

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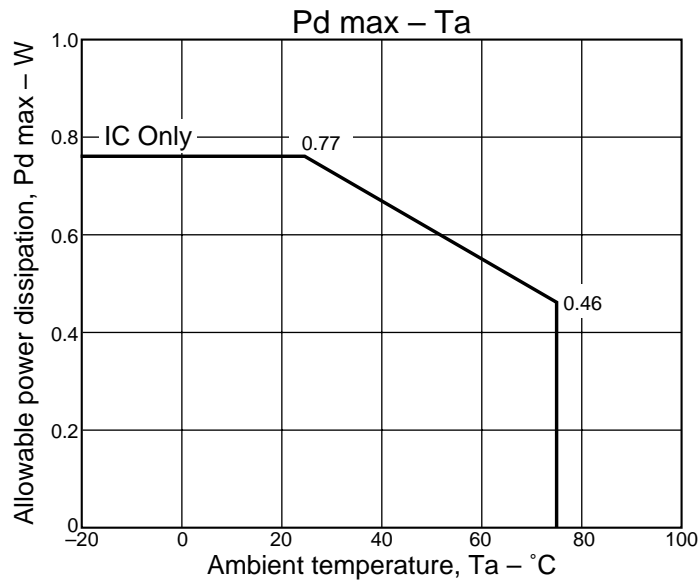
N1798RM(KI) No. 5973-1/7

Electrical Characteristics at $V_{CC} = 12V$, $V_{S1} = 5V$, $V_{S2} = 12V$, $T_a = 25^\circ C$

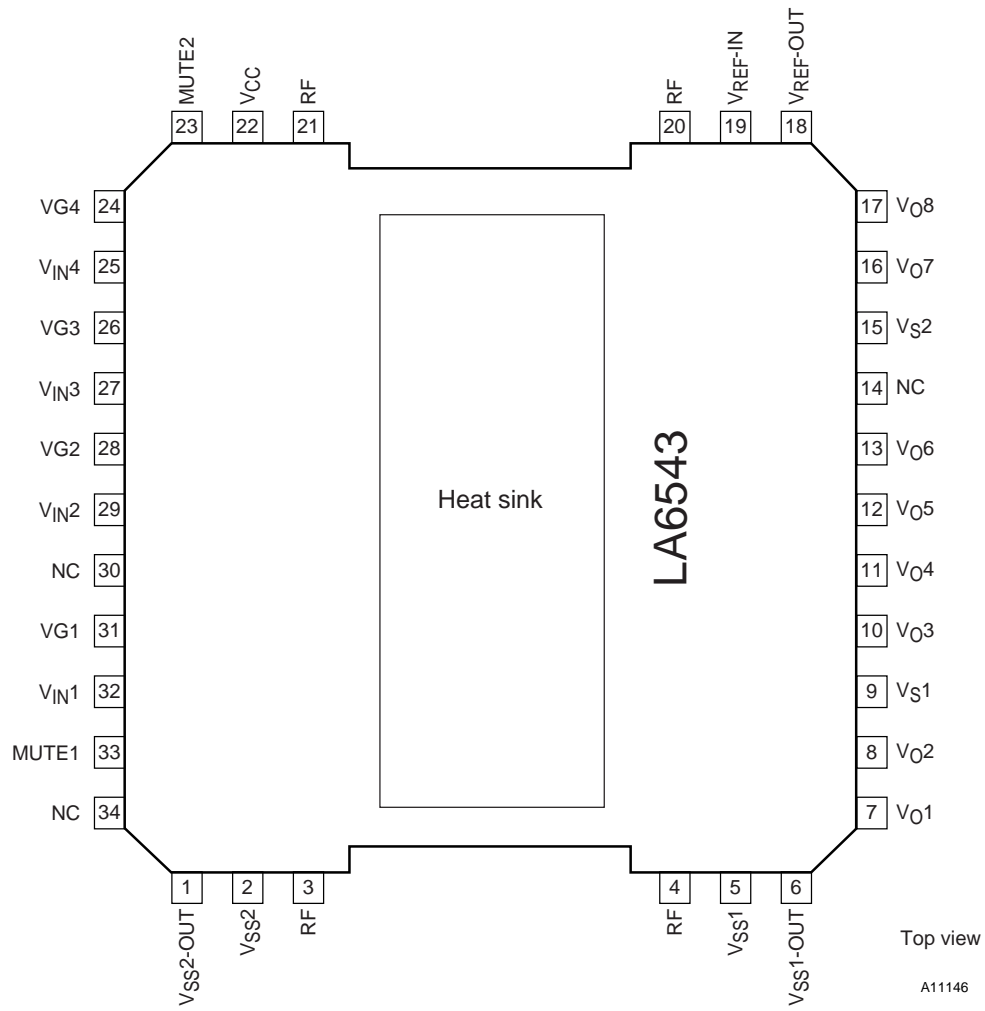
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{CC} no-load current drain	I_{CC1}	All outputs ON (MUTE1, MUTE2: High)	5	10	20	mA
	I_{CC2}	All outputs OFF (MUTE1, MUTE2: Low)		5	10	mA
V_{S1} no-load current drain	I_{S1-1}	CH1 ON (MUTE1, MUTE2: High)		20	40	mA
	I_{S1-2}	CH1 OFF (MUTE1, MUTE2: Low)			4	mA
V_{S2} no-load current drain	I_{S2-1}	CH2 to CH4 ON (MUTE1, MUTE2: High)		5	10	mA
	I_{S2-2}	CH2 to CH4 OFF (MUTE1, MUTE2: Low)			4	mA
Output offset voltage	$V_{OFF1 \text{ to } 4}$	Potential difference between plus and minus outputs for CH1 to CH4	-50		50	mV
Input voltage range	V_{IN}	Input voltage range for V_{IN1} to V_{IN4}	0.5		5	V
Output voltage (source) (sink)	$V_{Osource}$	Plus and minus outputs at high level	4.4	4.7		V
		$I_O = 700 \text{ mA}$				
	V_{Osink}	Plus and minus outputs at low level		0.3	0.6	V
		$I_O = 700 \text{ mA}$				
Closed circuit voltage gain1	VG1	Voltage gain between CH1 to CH3 BTL amplifiers		7		dB
Closed circuit voltage gain2	VG2	Voltage gain between CH4 BTL amplifiers		14		dB
Slew rate	SR	(Note 1)		0.5		V/ μs
Mute ON voltage	V_{MUTE}	MUTE1, MUTE2 voltage when output is ON (Note 2)		1.5	2	V
Mute ON current	I_{MUTE}	MUTE1, MUTE2 voltage when output is ON (Note 2)		6	10	μA

Note 1: Guaranteed design value

Note 2: MUTE turns amplifier output ON at High and OFF at Low. (At Low, output impedance becomes high.) MUTE1 and MUTE2 operate independently on the respective channels.



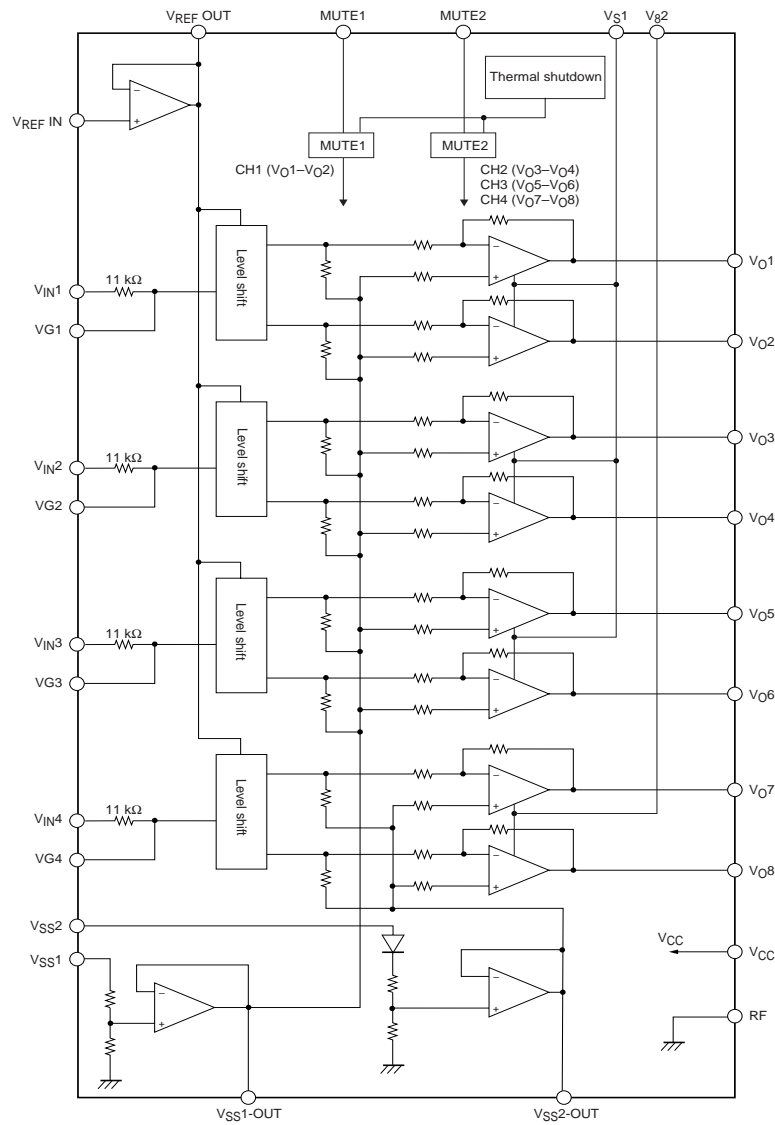
Pin Assignment



Pin Function

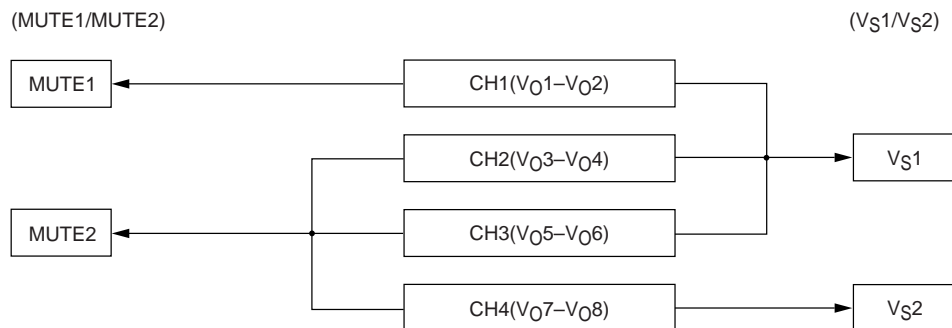
Pin number	Pin name	Equivalent circuit	Pin function
1	V _{SS2} -OUT		Output stage reference voltage (V _{SS2} -V _{BE})/2: typ)
2	V _{SS2}		Connect to V _{S2}
3,4 20,21	R _F		Substrate (minimum potential)
7	V _{O1}		CH1 non-inverted output (CH1+)
8	V _{O2}		CH1 inverted output (CH1-)
10	V _{O3}		CH2 non-inverted output (CH2+)
11	V _{O4}		CH2 inverted output (CH2-)
12	V _{O5}		CH3 non-inverted output (CH3+)
13	V _{O6}		CH3 inverted output (CH3-)
16	V _{O7}		CH4 non-inverted output (CH4+)
17	V _{O8}		CH4 inverted output (CH4-)
9	V _{S1}	A11144	Power supply for output stage (CH1 to CH3) (CH4)
15	V _{S2}		
5	V _{SS1}		Connect to V _{S1}
6	V _{SS1} -OUT		Output reference voltage (V _{SS1} /2: typ)
14,30 34	NC		May not be used.
18	V _{REF} -OUT		Output reference voltage (V _{REF} buffer amplifier output)
24	VG4		Input pin for CH4 (gain adjustment)
26	VG3		Input pin for CH3 (gain adjustment)
28	VG2		Input pin for CH2 (gain adjustment)
31	VG1		Input pin for CH1 (gain adjustment)
25	V _{IN4}		Input pin for CH4 (fixed gain)
27	V _{IN3}		Input pin for CH3 (fixed gain)
29	V _{IN2}		Input pin for CH2 (fixed gain)
32	V _{IN1}		Input pin for CH1 (fixed gain)
19	V _{REF} -IN		Reference voltage input (V _{REF} buffer amplifier input)
22	V _{CC}		Power supply
23	MUTE2		CH2-CH4 amplifier output ON/OFF
33	MUTE1		CH1 amplifier output ON/OFF

Block Diagram



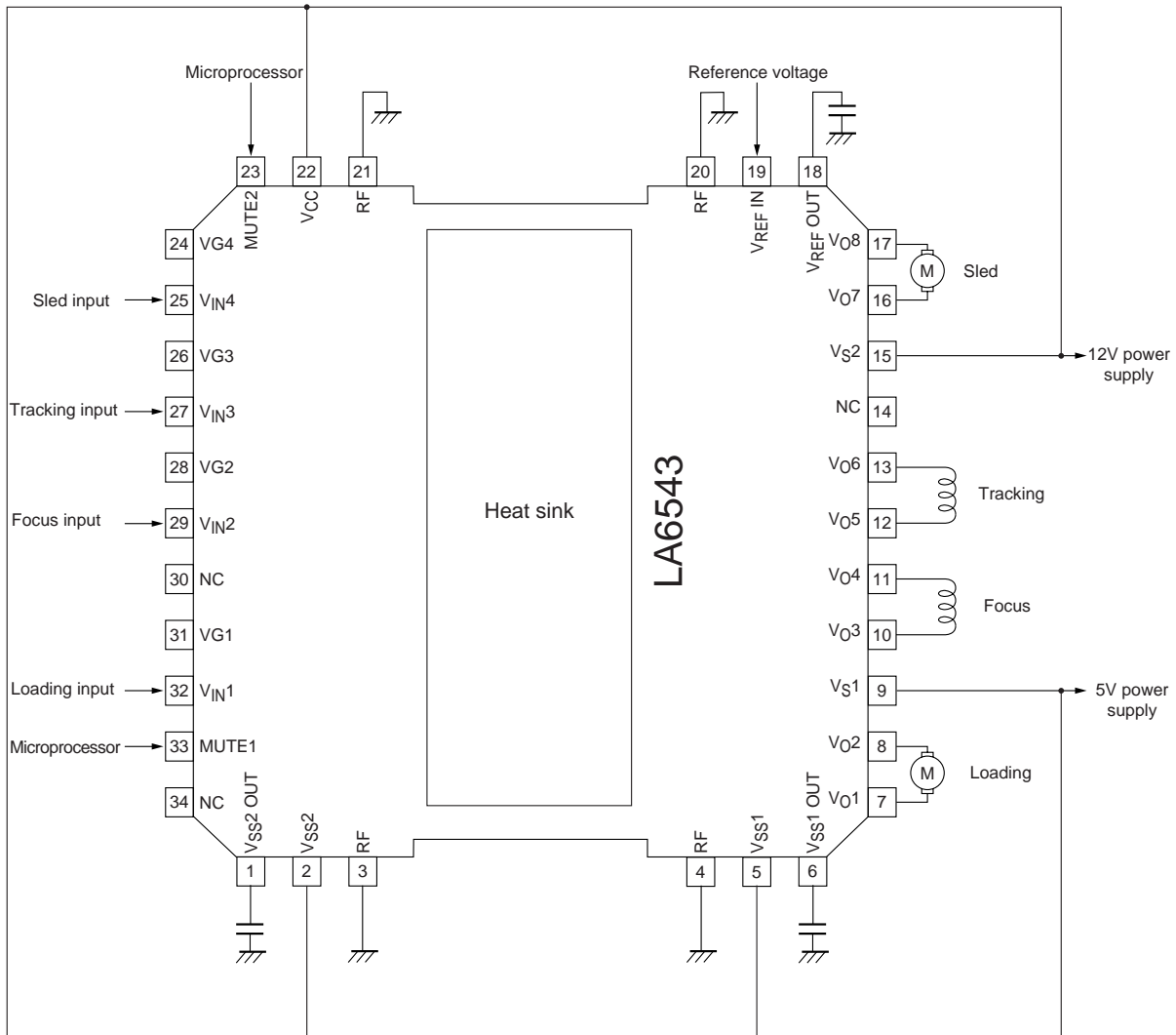
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System Diagram (relationship between power supply and MUTE)



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Sample Application Circuit



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Gain Setting (input pins and adjustment pins)

A simplified diagram of V_{IN} and VG is shown below.

- 1) Consider an 11 k Ω (typ.) resistor inserted between V_{IN} and VG.
- 2) When not the pin VG but the pin V_{IN} is used alone, the BTL gain (between V_{O+} and V_{O-}) is set to 7 dB for CH1 to CH3 (1 dB for AMP only). For CH4, it is 14 dB (8 dB for AMP only). This also applies for the case when V_{IN} is not used and an 11 k Ω external resistor is connected to VG for input.
- 3) Gain is set by the input impedance as seen from point A.

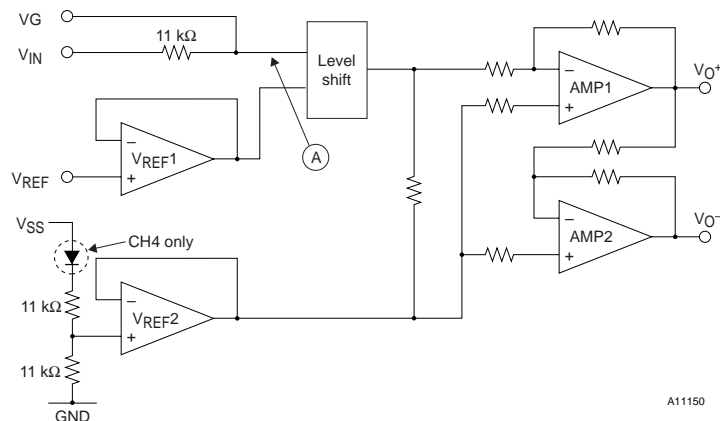
When VG only is used and the external resistor is R, the BTL gain (between V_{O+} and V_{O-}) is

$$20 \log (11 \text{ k}\Omega / R) + 14 \text{ dB}.$$

When an 11 k Ω resistor is inserted between V_{IN} and VG, and input is via V_{IN} , the combined resistance R_z as seen from point A is $R_z = 5.5 \text{ k}\Omega$. Gain is

$$\text{CH1 to CH3} : 20 \log (11 \text{ k}\Omega / 5.5 \text{ k}\Omega) + 7 \text{ dB} = 13 \text{ dB}$$

$$\text{CH4} : 20 \log (11 \text{ k}\Omega / 5.5 \text{ k}\Omega) + 14 \text{ dB} = 20 \text{ dB}.$$



Offset Voltage

This IC incorporates a level shifter circuit. The input references the voltage V_{REF} to be applied and references the voltage $(V_{SS1})/2V$ for channels 1 to 3 or the voltage $(V_{SS2}-V_{BE} (0.7))/2V$ for channel 4 to be output.

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