



SANYO Semiconductors

# DATA SHEET

## LA6548D — Monolithic Linear IC For Compact Disk Four-Channel Bridge (BTL) Driver

### Overview

The LA6548D is a 4-channel bridge (BTL) driver that integrates a 3.3 V regulator and a reset circuit on the same chip. It is optimal for use in CD players

### Functions

- Bridge-connection (BTL) power amplifier 4-channel.
- $I_O$  max 700mA
- MUTE circuit built-in (operable for all channels, Output ON for Mute : H)
- 3.3V regulator built-in (PNP transistor externally connected)
- Reset circuit built-in (reset output delay time set with the external capacitor)

### Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$ max		14	V
Allowable power dissipation	$P_d$ max	Independent IC	1.5	W
		Measure with a designated substrate*	2.5	W
Maximum input voltage	$V_{INB}$		13	V
MUTE pin voltage	$V_{MUTE}$		13	V
Operating temperature	$T_{opr}$		-20 to +75	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

\* Specified board size :  $76.1 \times 114.3 \times 1.6 \text{mm}^3$ , glass epoxy.

Recommended Operating Conditions at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Operating voltage	$V_{CC}$		4 to 13	V
Reset output source current	$I_{ORH}$		0 to 200	$\mu\text{A}$
Reset output sync current	$I_{ORL}$		0 to 2	mA

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# LA6548D

Electrical Characteristics at  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 6\text{V}$ ,  $V_{REF} = 1.65\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>Overall</b>						
No-load current drain 1	$I_{CC-ON}$	All channel outputs ON, Mute : Hi		20	40	mA
No-load current drain 2	$I_{CC-OFF}$	All channel outputs OFF, Mute : Low		15	35	mA
Output offset voltage	$V_{OFF}$	Each channel	-50		50	mV
Buffer input voltage range	$I_{BIN}$	VREG buffer amp input range	1.5		$V_{CC}-1.5$	V
Output voltage	$V_O$	$R_L = 8\Omega$ *1	2.6	3		V
Closed-circuit voltage gain	VG	Input/output gain		9		dB
Slew rate	SR			0.15		V/ $\mu\text{s}$
MUTE ON voltage	VMUTE	*2		1.2		V
<b>Power block (2SB632K used)</b>						
Output voltage	$V_{OUT1}$	$I_O = 200\text{mA}$	3.13	3.3	3.47	V
Line regulation	$\Delta V_{OLN1}$	$4\text{V} \leq V_{CC} \leq 12\text{V}$		40	100	mV
Load regulation	$\Delta V_{OLD1}$	$5\text{mA} \leq I_O \leq 200\text{mA}$		50	150	mV
<b>Reset block</b>						
H reset output voltage	$V_{ORH}$	$I_{ORH} = 200\mu\text{A}$ , Cd Pin open	3.08	3.25	3.42	V
L reset output voltage	$V_{ORL}$	$I_{ORL} = 2\text{mA}$ , Cd-GND short-circuited		100	200	mV
Reset threshold voltage	$V_{RT}$	*3	2.58	2.75	2.92	V
Reset hysteresis voltage	$V_{HYS}$	*4	40	80	160	mV
Reset output delay time	$t_d$	Cd = $0.1\mu\text{F}$		10		ms

Note \*1 : Voltage difference across each channel when the  $8\Omega$  load is added between outputs.

\*2 : MUTE voltage when the output is ON/OFF : all outputs are ON when MUTE = H and all channels are OFF when MUTE = L.

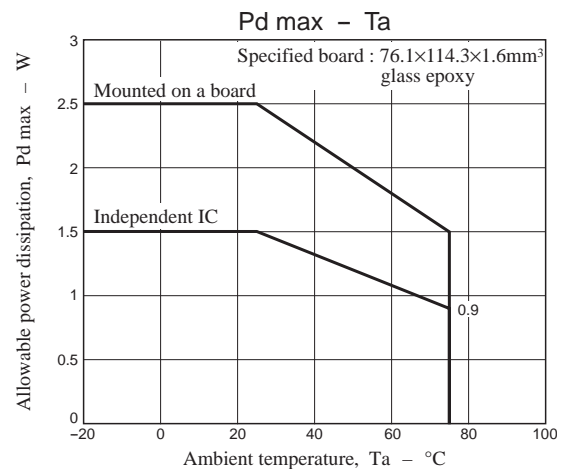
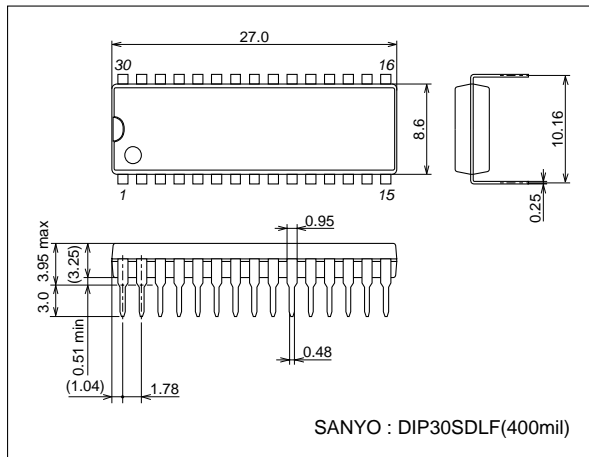
\*3 : 3.3VREG voltage when the reset is LOW.

\*4 : Voltage difference of 3.3VREG between resets at LOW and at HI.

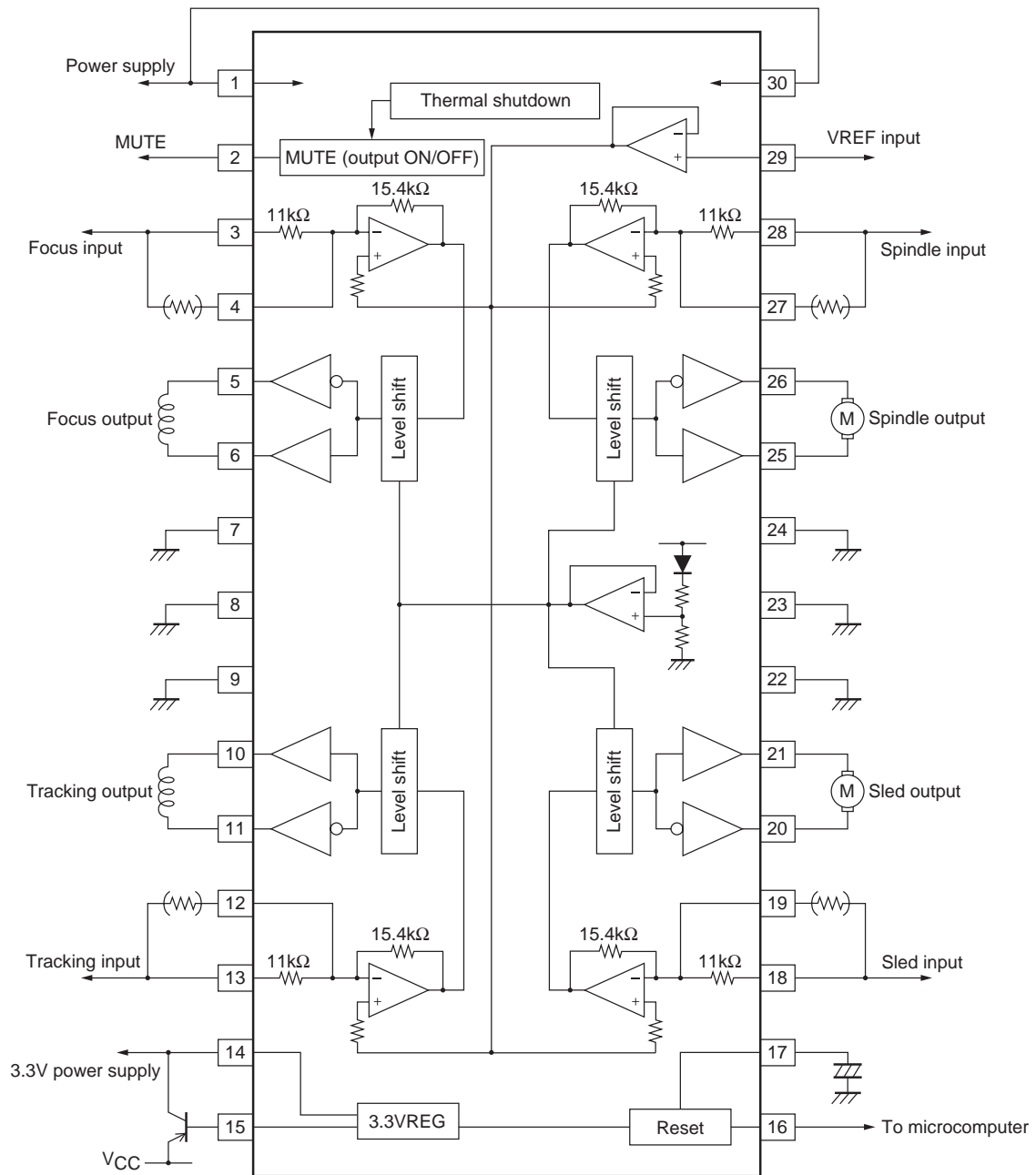
## Package Dimensions

unit : mm (typ)

3307



Block Diagram and Sample Application Circuit



# LA6548D

## Pin Functions

Pin No.	Symbol	Pin descriptions
1	V <sub>CC</sub>	Power (short-circuit with pin 30.)
2	MUTE	All channels output ON/OFF
3	V <sub>IN1</sub>	CH1 input pin
4	VG1	CH1 input pin (for gain control)
5	V <sub>O1+</sub>	CH1 output pin (counter-inversion)
6	V <sub>O1-</sub>	CH1 output pin (inversion)
7	GND	GND pin
8	GND	GND pin
9	GND	GND pin
10	V <sub>O2-</sub>	CH2 output pin (inversion)
11	V <sub>O2+</sub>	CH2 output pin (counter-inversion)
12	VG2	CH2 input pin (for gain control)
13	V <sub>IN2</sub>	CH2 input pin
14	REG-OUT	Connect collector of the external transistor (PNP), 3.3VREG power output
15	REG-IN	Connect base of the external PNP transistor
16	RESET	Reset output
17	CD	Reset output delay time setting (with external capacitor)
18	V <sub>IN3</sub>	CH3 input pin
19	VG3	CH3 input pin (for gain control)
20	V <sub>O3+</sub>	CH3 output pin (counter-inversion)
21	V <sub>O3-</sub>	CH3 output pin (inversion)
22	GND	GND pin
23	GND	GND pin
24	GND	GND pin
25	V <sub>O4-</sub>	CH4 output pin (inversion)
26	V <sub>O4+</sub>	CH4 output pin (counter-inversion)
27	VG4	CH4 input pin (for gain control)
28	V <sub>IN4</sub>	CH4 input pin
29	VREF	Application of the reference voltage
30	V <sub>CC</sub>	Power supply (short-circuit with pin 1)

Note : GND should have the lowest potential) as connected with pins 7 to 9 and pins 22 to 24.

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## Pin Description

Pin No.	Symbol	Pin function	Description	Equivalent circuit
3 13 18 28 4 12 19 27	$V_{IN1}$ $V_{IN2}$ $V_{IN3}$ $V_{IN4}$ $VG1$ $VG2$ $VG3$ $VG4$	Input	Each input pin	
5 6 11 10 20 21 26 25	$V_{O1+}$ $V_{O1-}$ $V_{O2+}$ $V_{O2-}$ $V_{O3+}$ $V_{O3-}$ $V_{O4+}$ $V_{O4-}$	Output	Each output pin	
2	MUTE	MUTE	MUTE	

## Truth Table

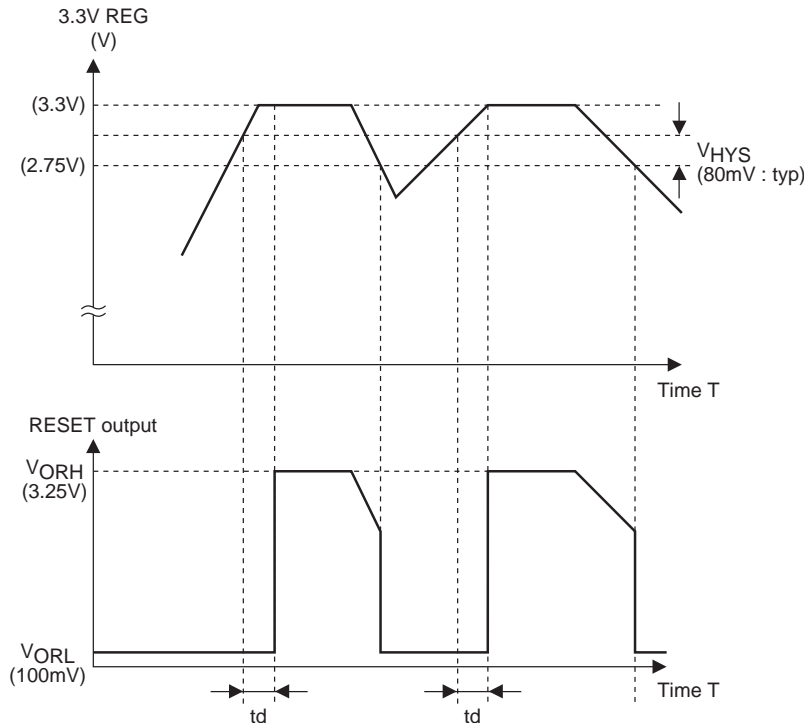
Input	MUTE	CH1		CH2		CH3		CH4	
		$V_{O1+}$	$V_{O1-}$	$V_{O2+}$	$V_{O2-}$	$V_{O3+}$	$V_{O3-}$	$V_{O4+}$	$V_{O4-}$
H	H	H	L	L	H	H	L	L	H
	L	-	-	-	-	-	-	-	-
L	H	L	H	H	L	L	H	H	L
	L	-	-	-	-	-	-	-	-

\* - : High-impedance

## Gain setting

For gain setting, refer to the block diagram. When setting the gain with the  $V_G^*$  terminal, the total gain has more or less temperature characteristics due to difference in temperature characteristics between internal and external resistors. Use the  $V_{IN}^*$  terminal to set the gain.

## Reset operation



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