



SANYO Semiconductors

DATA SHEET

LA6541NH — Monolithic Linear IC For CD Players and Recorders Four-Channel Driver IC

Overview

The LA6541NH is a four-channel driver IC for CD players and recorders (four BTL amplifier channels).

Functions

- Four BTL connection power amplifier channels
- I_O max 0.7A
- Built-in level shifters
- Muting circuit (on/off control of all outputs)
(This circuit applies to the BTL amplifier circuits. It does not control operation of the regulator.)
- Built-in regulator (provides a 5V output using an external pnp transistor)
- Thermal protection circuit (thermal shutdown circuit)

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Maximum input voltage	V_{IN}		13	V
Maximum output current	I_O max	For each of the channel 1 to 4 outputs	0.7	A
Muting pin application voltage	V_{MUTE}		13	V
Allowable power dissipation	P_d max	Independent IC	0.8	W
		Specified circuit board	1.8	W
Operating temperature	T_{opr}		-30 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

* Specified substrate : 76.1mm×114.3mm×1.6mm, glass epoxy board.

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Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC1}		5.6 to 13	V
Supply voltage 2	V_{CC2}	Only used by the BTL amplifiers (Not used by the 5V regulator circuit)	3.9 to 13	V

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 8\text{V}$, $V_{REF} = 2.5\text{V}$, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Overall Characteristics						
No-load current drain, on state	I_{CCON}	All outputs on, MUTE : high		20	40	mA
No-load current drain, off state	I_{CCOFF}	All outputs off, MUTE : low		15	35	mA
Thermal shutdown circuit operating temperature	TSD	(Design guarantee value *1)	150	175	200	$^\circ\text{C}$
Output Amplifier Block						
Output offset voltage	V_{OFF}	The voltage difference between each of the + or - outputs.	-50		50	mV
V_{REF} input voltage range	$V_{IN}V_{REF}$		1.5		$V_{CC}-1.5$	V
Output voltage	V_O	The voltage across the outputs when $R_L = 8\Omega$	4	4.7		V
Voltage gain, input to output	VG	The voltage gain from an input to the corresponding +/- outputs.*2		9		dB
Slew rate	SR	(Design guarantee value *1)		0.15		V/ μs
Muting on voltage	V_{MUTE}	The voltage at which the output on/off state changes		1.2		V
Power Supply Block (Using a 2SB632K)						
5V power supply voltage		$I_O = 200\text{mA}$	4.75	5.00	5.25	V
Line regulation	ΔV_{OLIN}	$5.6\text{V} \leq V_{CC} \leq 12\text{V}$		20	100	mV
Load regulation	ΔV_{OLOAD}	$5\text{mA} \leq I_O \leq 200\text{mA}$		50	150	mV
Reset Block						
RESET pin high-level voltage	V_{ORH}		4.73	4.98	5.23	V
RESET pin low-level voltage	V_{ORL}	$I_{SRL} = 2\text{mA}$, Cd-GND		100	200	mV
RESET pin threshold voltage	V_{RT}	*4		4.2		V
RESET pin hysteresis	V_{HYS}	*5	40	100	200	mV
RESET pin output delay time	t_d	$C_d = 0.1\mu\text{F}$		10		ms

*1 : These parameters are not tested.

2 : The gain from input to output when only the V_{IN}^ pins are used.

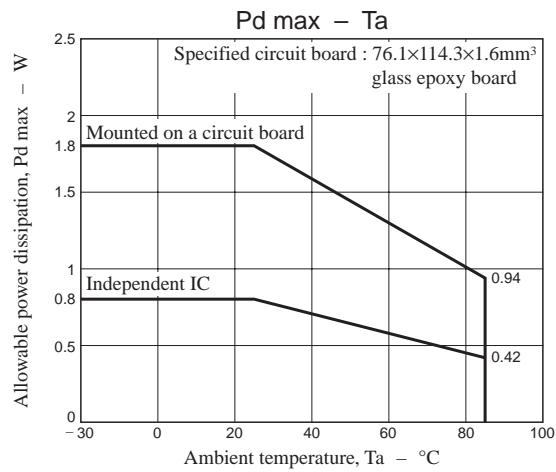
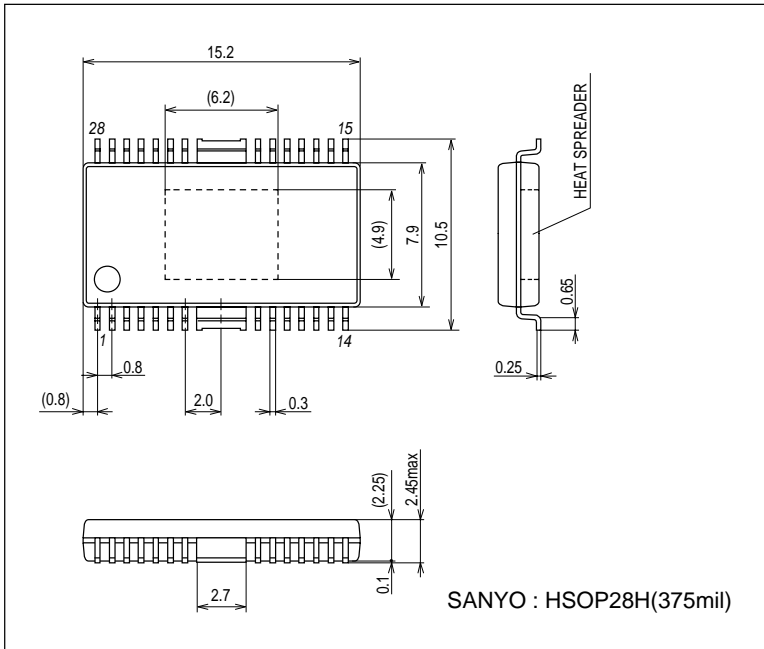
*3 : The MUTE pin voltage when the output changes between the on and off states. When the MUTE pin is high, all the BTL amplifiers will be on, and the when MUTE is low, all the BTL amplifiers will be off.

*4 : The 5V regulator voltage when the RESET pin goes from high to low.

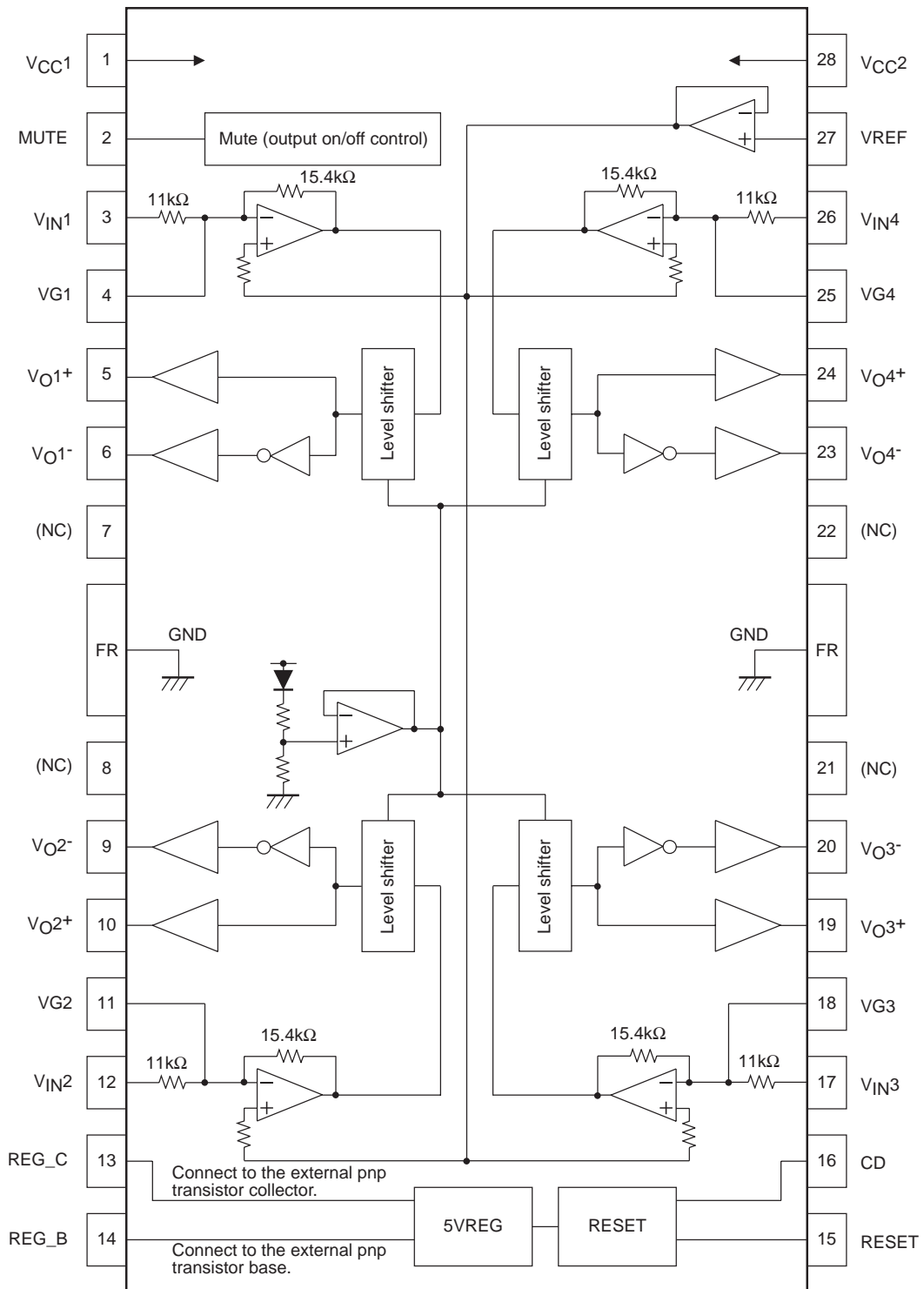
*5 : The 5V regulator voltage difference between the RESET pin going from high to low the RESET pin going from low to high. That is, the hysteresis.

Package Dimensions

unit : mm (typ)
3233B



Block Diagram



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Pin Functions

Pin No.	Pin	Description
1	V _{CC} 1	Power supply (This pin is shorted to V _{CC} 2 (pin 28))
2	MUTE	Output on/off control
3	V _{IN} 1	Channel 1 input
4	VG1	Channel 1 input (Gain setting)
5	V _O 1 ⁺	Channel 1 output (+)
6	V _O 1 ⁻	Channel 1 output (-)
7	(NC)	(This pin must not be used.)
8	(NC)	(This pin must not be used.)
9	V _O 2 ⁻	Channel 2 output (-)
10	V _O 2 ⁺	Channel 2 output (+)
11	VG2	Channel 2 input (Gain setting)
12	V _{IN} 2	Channel 2 input
13	REG_C	Connect this pin to the external pnp transistor collector. (This is the 5 V regulator output)
14	REG_B	Connect this pin to the external pnp transistor base.
15	RESET	Reset output
16	CD	Connection for the reset delay time setting capacitor
17	V _{IN} 3	Channel 3 input (Gain setting)
18	VG3	Channel 3 input (Gain setting)
19	V _O 3 ⁺	Channel 3 output (+)
20	V _O 3 ⁻	Channel 3 output (-)
21	(NC)	(This pin must not be used.)
22	(NC)	(This pin must not be used.)
23	V _O 4 ⁻	Channel 4 output (-)
24	V _O 4 ⁺	Channel 4 output (+)
25	VG4	Channel 4 input (Gain setting)
26	V _{IN} 4	Channel 4 input (Gain setting)
27	VREF	Reference voltage input
28	V _{CC} 2	Power supply (This pin is shorted to V _{CC} 1 (pin 1))

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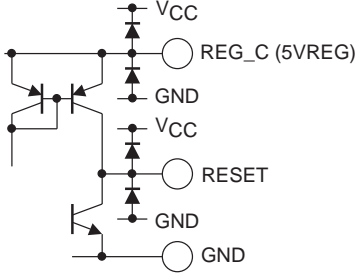
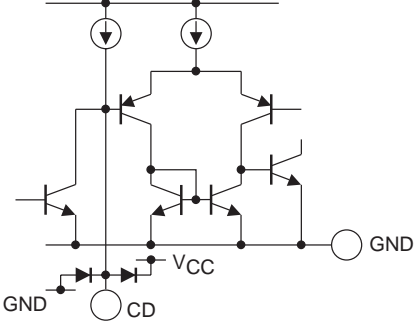
Equivalent Circuits

Pin No.	Pin	Description	Equivalent circuit
3 4 12 11 17 18 26 25	V_{IN1} VG1 V_{IN2} VG2 V_{IN3} VG3 V_{IN4} VG4	Input pins.	<p>The diagram shows four differential input stages. Each stage consists of a pair of transistors with diodes connected to their bases. The diodes are connected to V_{CC} and GND. A 11kΩ resistor is connected between the two V_{CC} nodes. The inputs are labeled V_{ING^*} and V_{IN^*}.</p>
5 6 10 9 19 20 24 23	V_{O1^+} V_{O1^-} V_{O2^+} V_{O2^-} V_{O3^+} V_{O3^-} V_{O4^+} V_{O4^-}	Output pins.	<p>The diagram shows a push-pull output stage with two transistors. A 33kΩ resistor is connected between the V_{CC} supply and the output node. The output is labeled $V_{O^{+/-}}$.</p>
2	MUTE	Muting control input. The outputs will be on when the MUTE pin is at the high level. The outputs will be off when the MUTE pin is at the low level ; in particular, the outputs go to the high-impedance state at this time.	<p>The diagram shows a transistor whose base is connected to the MUTE pin. The base is also connected to V_{CC} through a 40kΩ resistor and to GND through a 30kΩ resistor. The emitter is connected to GND, and the collector is connected to the output stage.</p>
27	VREF	Reference voltage input.	<p>The diagram shows a differential input stage similar to the first row, but with a resistor network connected to the output nodes. The inputs are labeled V_{REF} and V_{CC}.</p>

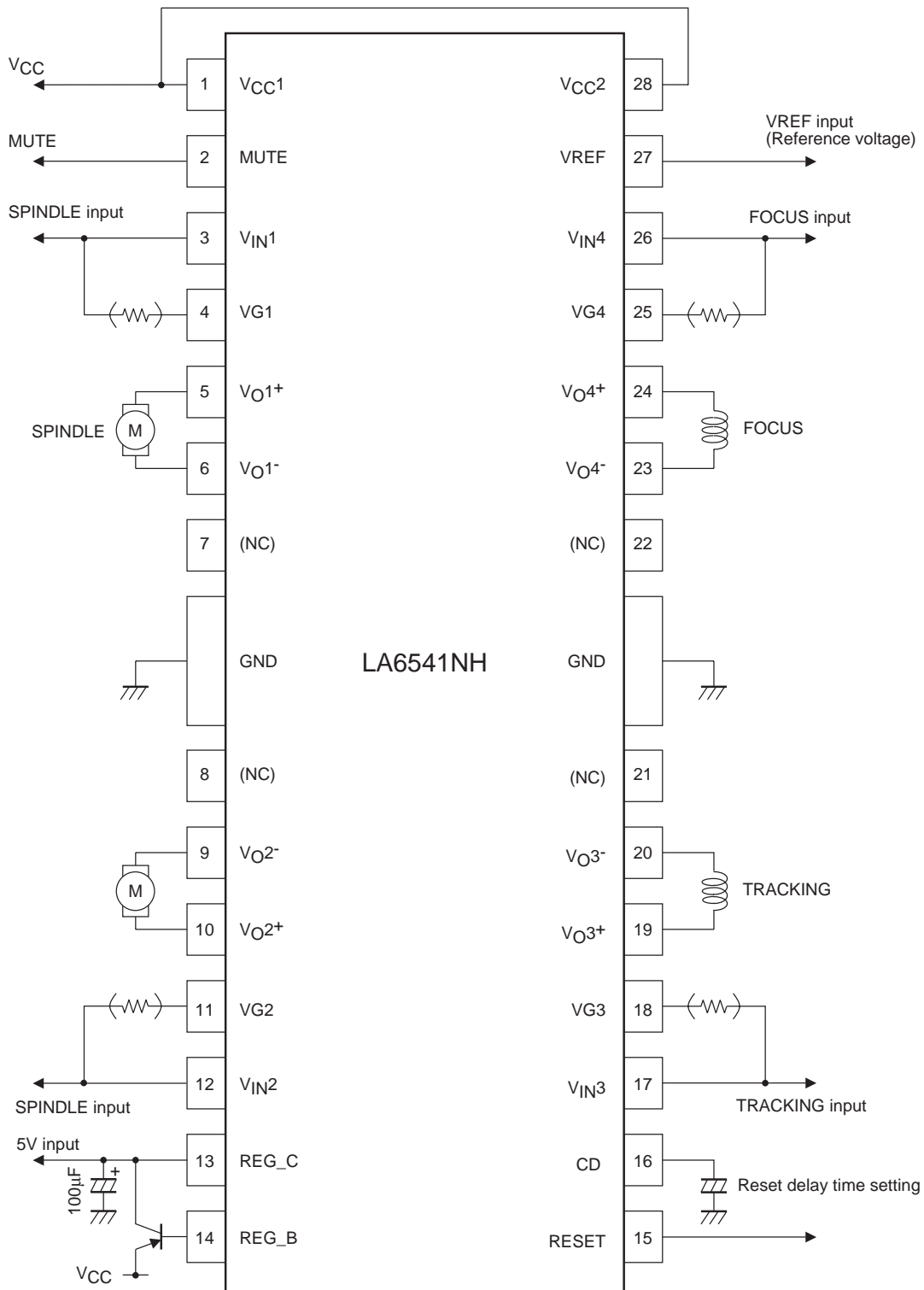
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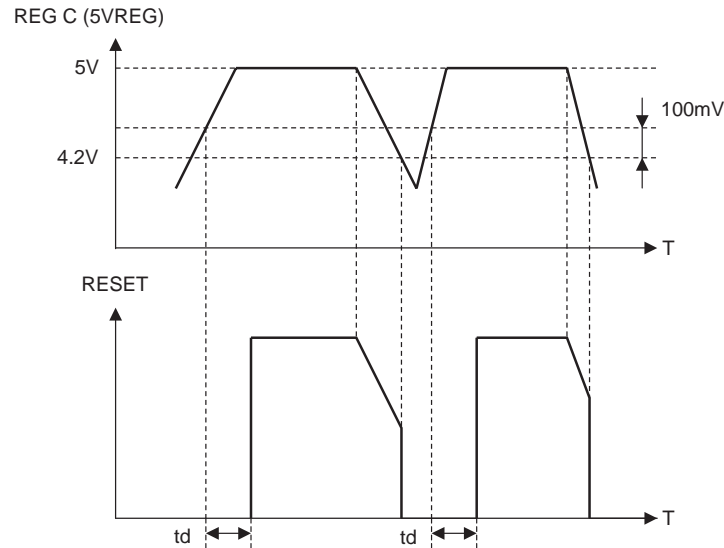
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Pin No.	Pin	Description	Equivalent circuit
15	RESET	<p>Reset output.</p> <p>When REG C (5VREG) is high, RESET will be high.</p> <p>When REG C (5VREG) is low, RESET will be low.</p> <p>See section 11, Reset Operation, for details on the reset operation.</p>	
16	CD	<p>Reset output delay time setting.</p> <p>The delay time until the point the reset output switches from low to high is set by the capacitor connected between this pin and ground.</p> <p>See section 11, Reset Operation, for details on the reset operation.</p>	

Application Circuit Example



Reset Operation



*1 : t_d is the delay time. It is set by an external capacitor connected between the CD pin and ground).

*2 : The voltage at which RESET changes state is a typical value (voltage).

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