

40 V, 2 A PNP low  $V_{\mbox{CEsat}}$  (BISS) transistor with N-channel Trench MOSFET

Rev. 1 — 25 August 2010

**Preliminary data sheet** 

# 1. Product profile

## 1.1 General description

Combination of PNP low V<sub>CEsat</sub> Breakthrough In Small Signal (BISS) transistor and N-channel Trench MOSFET. The device is housed in a small and ultra thin SOT1118 Surface-Mounted Device (SMD) plastic package.

## 1.2 Features and benefits

- Very low collector-emitter saturation voltage V<sub>CEsat</sub>
- High collector current capability I<sub>C</sub> and I<sub>CM</sub>
- High collector current gain (h<sub>FE</sub>) at high I<sub>C</sub>
- High energy efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

## 1.3 Applications

- Loadswitch
- Power management

- Battery-driven devices
- Charging circuits
- Power switches (e.g. motors, fans)

## 1.4 Quick reference data

Table 1.	Quick	reference	data
	QUICK	relefence	uata

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
PNP low \	/ <sub>CEsat</sub> (BISS) transistor						
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	-40	V	
I <sub>C</sub>	collector current		<u>[1]</u> _	-	-2	А	
I <sub>CM</sub>	peak collector current	single pulse; $t_p \leq 1 \text{ ms}$	<u>[1]</u> _	-	-3	А	
R <sub>CEsat</sub>	collector-emitter saturation resistance	I <sub>C</sub> = -500 mA; I <sub>B</sub> = -50 mA	[2] _	240	340	mΩ	
N-channel Trench MOSFET							
V <sub>DS</sub>	drain-source voltage	T <sub>amb</sub> = 25 °C	-	-	30	V	
V <sub>GS</sub>	gate-source voltage	T <sub>amb</sub> = 25 °C	-	-	±8	V	



## **NXP Semiconductors**

# PBSM5240PF

### 40 V, 2 A PNP BISS/Trench MOSFET module

Table 1.	Quick reference data	continued				
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I <sub>D</sub>	drain current	T <sub>amb</sub> = 25 °C; V <sub>GS</sub> = 10 V	<u>[3]</u> _	-	0.66	A
R <sub>DSon</sub>	drain-source on-state resistance	$T_j = 25 \text{ °C};$ $V_{GS} = 4.5 \text{ V};$ $I_D = 0.2 \text{ A}$	<u>[4]</u>	390	460	mΩ

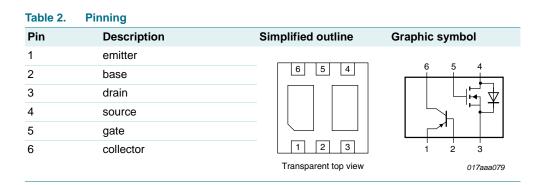
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.

[2] Pulse test:  $t_p \leq 300 \ \mu s$ ;  $\delta \leq 0.02$ .

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

[4] Pulse test:  $t_p \le 300 \ \mu s$ ;  $\delta \le 0.01$ .

#### **Pinning information** 2.



#### **Ordering information** 3.

#### Table 3. **Ordering information**

Type number	Package	Package					
	Name	Description	Version				
PBSM5240PF	HUSON6	Plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body $2 \times 2 \times 0.65$ mm	SOT1118				

#### Marking 4.

Type number	Marking code <sup>[1]</sup>	
PBSM5240PF	<tbd></tbd>	

\* = -: made in Hong Kong

\* = p: made in Hong Kong

\* = t: made in Malaysia

\* = W: made in China

PBSM5240PF Preliminary data sheet

## **NXP Semiconductors**

# PBSM5240PF

#### 40 V, 2 A PNP BISS/Trench MOSFET module

# 5. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
PNP low V	CEsat (BISS) transistor				
V <sub>CBO</sub>	collector-base voltage	open emitter	-	-40	V
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-40	V
V <sub>EBO</sub>	emitter-base voltage	open collector	-	-5	V
I <sub>C</sub>	collector current		<u>[1]</u> _	-2	А
I <sub>CM</sub>	peak collector current	single pulse; $t_p \leq 1 ms$	<u>[1]</u> -	-3	А
I <sub>B</sub>	base current		<u>[1]</u> _	-300	mA
I <sub>BM</sub>	peak base current		<u>[1]</u> -	-1	А
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25 \ ^{\circ}C$	<u>[1]</u> _	1.3	W
N-channel	Trench MOSFET				
V <sub>DS</sub>	drain-source voltage	T <sub>amb</sub> = 25 °C	-	30	V
$V_{DG}$	drain-gate voltage	$T_{amb}$ = 25 °C; $R_{GS}$ = 20 k $\Omega$	-	30	V
V <sub>GS</sub>	gate-source voltage	T <sub>amb</sub> = 25 °C	-	±8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V	[2]		
		T <sub>amb</sub> = 25 °C	-	0.66	А
		T <sub>amb</sub> = 100 °C	-	0.42	А
I <sub>DM</sub>	peak drain current	$T_{amb} = 25 \ ^{\circ}C;$ single pulse; $t_p \le 10 \ \mu s$	-	3.56	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2] _	200	mW
Source-dra	in diode				
I <sub>S</sub>	source current	$T_{amb} = 25 \ ^{\circ}C$	-	0.66	А
Per device	•				
Тj	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-55	+150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

#### 40 V, 2 A PNP BISS/Trench MOSFET module

## 6. Thermal characteristics

Table 6.	Thermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
<b>PNP</b> low	V <sub>CEsat</sub> (BISS) transistor					
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	<u>[1]</u> -	-	95	K/W
N-channel Trench MOSFET						
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[2] _	-	625	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

## 7. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
I <sub>CBO</sub>	collector-base cut-off	$V_{CB}$ = -40 V; I <sub>E</sub> = 0 A		-	-	-100	nA
	current	$\label{eq:VCB} \begin{array}{l} V_{CB} = -40 \ V; \ I_{E} = 0 \ A; \\ T_{j} = 150 \ ^{\circ}C \end{array}$		-	-	-50	μA
I <sub>CEO</sub>	collector-emitter cut-off current	$V_{CE} = -30 \text{ V}; I_B = 0 \text{ A}$		-	-	-100	nA
I <sub>EBO</sub>	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; \text{ I}_{C} = 0 \text{ A}$		-	-	-100	nA
h <sub>FE</sub>	DC current gain	$V_{CE} = -5 V$					
		$I_C = -1 \text{ mA}$		300	-	-	
		I <sub>C</sub> = -100 mA		300	-	800	
		I <sub>C</sub> = -500 mA	[1]	250	-	-	
		I <sub>C</sub> = -1 A	<u>[1]</u>	160	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_C = -100 \text{ mA}; I_B = -1 \text{ mA}$		-	-80	-140	mV
		$I_{C} = -500 \text{ mA};$ $I_{B} = -50 \text{ mA}$	<u>[1]</u>	-	-120	-170	mV
		$I_{C} = -1 \text{ A}; I_{B} = -100 \text{ mA}$	[1]	-	-200	-310	mV
R <sub>CEsat</sub>	collector-emitter saturation resistance	$I_{C} = -500 \text{ mA};$ $I_{B} = -50 \text{ mA}$	<u>[1]</u>	-	240	340	mΩ
V <sub>BEsat</sub>	base-emitter saturation voltage	$I_{C} = -1$ A; $I_{B} = -50$ mA	<u>[1]</u>	-	-	-1.1	V
V <sub>BEon</sub>	base-emitter turn-on voltage	$V_{CE} = -5 \text{ V}; \text{ I}_{C} = -1 \text{ A}$	[1]	-	-	-1	V
f <sub>T</sub>	transition frequency	$V_{CE} = -10 V;$ $I_{C} = -50 mA;$ f = 100 MHz		150	-	-	MHz
C <sub>c</sub>	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz		-	-	12	pF

 Table 7.
 Characteristics for PNP low V<sub>CEsat</sub> transistor

[1] Pulse test:  $t_p \le 300 \ \mu s; \ \delta \le 0.02.$ 

Preliminary data sheet

### 40 V, 2 A PNP BISS/Trench MOSFET module

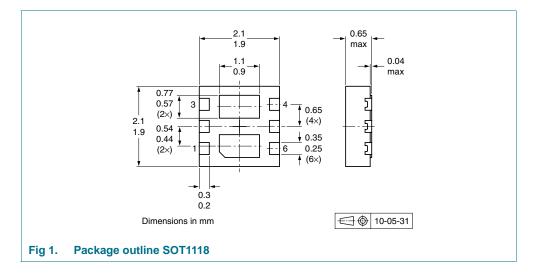
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
V <sub>(BR)DSS</sub>	drain-source breakdown	$I_D = 10 \ \mu A; \ V_{GS} = 0 \ V$				
	voltage	T <sub>j</sub> = 25 °C	30	-	-	V
		T <sub>j</sub> = −55 °C	27	-	-	V
V <sub>GS(th)</sub>	gate-source threshold	$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$				
	voltage	T <sub>j</sub> = 25 °C	0.45	0.7	0.95	V
		T <sub>j</sub> = 150 °C	0.25	-	-	V
		T <sub>j</sub> = −55 °C	-	-	1.15	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}$				
		T <sub>j</sub> = 25 °C	-	-	1	μA
		T <sub>j</sub> = 150 °C	-	-	100	μA
I <sub>GSS</sub>	gate leakage current	$V_{GS}$ = ±8 V; $V_{DS}$ = 0 V	-	10	±100	nA
R <sub>DSon</sub>	drain-source on-state	$V_{GS}$ = 4.5 V; I <sub>D</sub> = 0.2 A	[2]			
	resistance	T <sub>j</sub> = 25 °C	-	390	460	mΩ
		T <sub>j</sub> = 150 °C	-	663	782	mΩ
		$V_{GS}$ = 2.5 V; $I_D$ = 0.1 A	-	460	560	mΩ
		$V_{GS}$ = 1.8 V; I <sub>D</sub> = 75 mA	-	550	730	mΩ
Dynamic o	characteristics					
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 1 A; V <sub>DS</sub> = 15 V;	-	0.89	-	nC
Q <sub>GS</sub>	gate-source charge	V <sub>GS</sub> = 4.5 V	-	0.1	-	nC
Q <sub>GD</sub>	gate-drain charge		-	0.2	-	nC
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 V; V_{DS} = 25 V;$	-	43	-	pF
C <sub>oss</sub>	output capacitance	f = 1 MHz	-	7.7	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	4.8	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 15 V;	-	4	-	ns
t <sub>r</sub>	rise time	$R_{L} = 15 \Omega;$	-	7.5	-	ns
t <sub>d(off)</sub>	turn-off delay time	– V <sub>GS</sub> = 10 V; R <sub>G</sub> = 6 Ω	-	18	-	ns
t <sub>f</sub>	fall time	- <b>-</b>	-	4.5	-	ns
Source-dr	ain diode					
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 0.3 A; V <sub>GS</sub> = 0 V	-	0.76	1.2	V

# Table 8.Characteristics for N-channel Trench MOSFET $T_i = 25$ °C unless otherwise specified.

 $\label{eq:point} \begin{tabular}{ll} \end{tabular} \end{tabular} \begin{tabular}{ll} \end{tabular} 1 \end{tabular} \end{tabular} \end{tabular} \end{tabular} \begin{tabular}{ll} \end{tabular} \end{tabular} \end{tabular} \end{tabular} \begin{tabular}{ll} \end{tabular} \end{tabular}$ 

40 V, 2 A PNP BISS/Trench MOSFET module

# 8. Package outline



# 9. Packing information

### Table 9. Packing methods

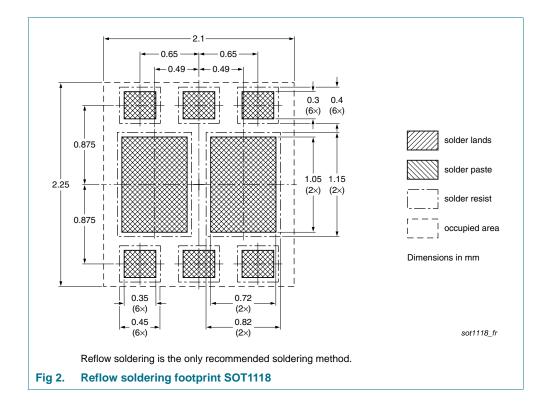
The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity
			3000
PBSM5240PF	SOT1118	4 mm pitch, 8 mm tape and reel	-115

[1] For further information and the availability of packing methods, see <u>Section 13</u>.

### 40 V, 2 A PNP BISS/Trench MOSFET module

# 10. Soldering



PBSM5240PF

40 V, 2 A PNP BISS/Trench MOSFET module

# 11. Revision history

Table 10. Revision hist	ory			
Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSM5240PF v.1	20100825	Preliminary data sheet	-	-

#### 40 V, 2 A PNP BISS/Trench MOSFET module

## 12. Legal information

### 12.1 Data sheet status

Document status[1][2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

### 12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <a href="http://www.nxp.com/profile/terms">http://www.nxp.com/profile/terms</a>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

PBSM5240PF

Preliminary data sheet

All information provided in this document is subject to legal disclaimers. Rev. 1 — 25 August 2010 © NXP B.V. 2010. All rights reserved. 9 of 11

#### 40 V, 2 A PNP BISS/Trench MOSFET module

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

## 12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

# **13. Contact information**

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

PBSM5240PF

**Preliminary data sheet** 

#### 40 V, 2 A PNP BISS/Trench MOSFET module

## 14. Contents

1	Product profile 1
1.1	General description 1
1.2	Features and benefits 1
1.3	Applications 1
1.4	Quick reference data 1
2	Pinning information 2
3	Ordering information 2
4	Marking 2
5	Limiting values 3
6	Thermal characteristics 4
7	Characteristics 4
8	Package outline 6
9	Packing information 6
10	Soldering 7
11	Revision history 8
12	Legal information 9
12.1	Data sheet status 9
12.2	Definitions
12.3	Disclaimers
12.4	Trademarks 10
13	Contact information 10
14	Contents 11

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

#### © NXP B.V. 2010.

All rights reserved.

For more information, please visit: http://www.nxp.com For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 25 August 2010 Document identifier: PBSM5240PF