

**Product Summary**

Device	$V_{(BR)DSS}$	$R_{DS(ON)}$ max	$I_D$ max $T_A = 25^\circ C$
Q1	20V	0.99Ω @ $V_{GS} = 4.5V$	450mA
		1.2Ω @ $V_{GS} = 2.5V$	400mA
		1.8Ω @ $V_{GS} = 1.8V$	330mA
		2.4Ω @ $V_{GS} = 1.5V$	300mA
Q2	-20V	1.9Ω @ $V_{GS} = -4.5V$	-310mA
		2.4Ω @ $V_{GS} = -2.5V$	-280mA
		3.4Ω @ $V_{GS} = -1.8V$	-240mA
		5Ω @ $V_{GS} = -1.5V$	-180mA

**Features and Benefits**

- Low On-Resistance
- Very low Gate Threshold Voltage, 1.0V max
- Low Input Capacitance
- Fast Switching Speed
- Ultra-Small Surface Mount Package 1mm x 1mm
- Low Package Profile, 0.45mm Maximum Package height
- ESD Protected Gate
- **Lead Free By Design/RoHS Compliant (Note 1)**
- **"Green" Device, Halogen and Antimony Free (Note 2)**
- **Qualified to AEC-Q101 standards for High Reliability**

**Mechanical Data**

- Case: SOT963
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.027 grams (approximate)

**Description and Applications**

This MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

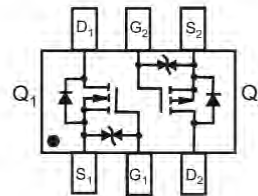
- General Purpose Interfacing Switch
- Power Management Functions
- Analog Switch



SOT963



Top View



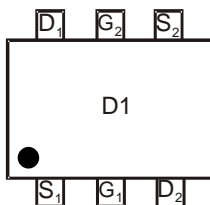
Top View  
Schematic and Transistor Diagram

**Ordering Information** (Note 3)

Part Number	Case	Packaging
DMC2990UDJ-7	SOT963	10K/Tape & Reel

- Notes:
1. No purposefully added lead.
  2. Diodes Inc.'s "Green" policy can be found on our website at <http://www.diodes.com>.
  3. For packaging details, go to our website at <http://www.diodes.com>.

**Marking Information**



D1 = Product Type Marking Code

**Thermal Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 4)	$P_D$	350	mW
Thermal Resistance, Junction to Ambient (Note 4)	Steady State $R_{\theta JA}$	360	$^\circ\text{C/W}$
		t<5s	270
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

**Maximum Ratings Q1 N-CHANNEL** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic	Symbol	Value	Units	
Drain-Source Voltage	$V_{DSS}$	20	V	
Gate-Source Voltage	$V_{GSS}$	$\pm 8$	V	
Continuous Drain Current (Note 4) $V_{GS} = 4.5\text{V}$	Steady State $I_D$	$T_A = 25^\circ\text{C}$	450	mA
		$T_A = 70^\circ\text{C}$	350	
Continuous Drain Current (Note 4) $V_{GS} = 1.8\text{V}$	Steady State $I_D$	$T_A = 25^\circ\text{C}$	330	mA
		$T_A = 70^\circ\text{C}$	260	
Continuous Drain Current (Note 4) $V_{GS} = 4.5\text{V}$	t<5s $I_D$	$T_A = 25^\circ\text{C}$	520	mA
		$T_A = 70^\circ\text{C}$	410	
Continuous Drain Current (Note 4) $V_{GS} = 1.8\text{V}$	t<5s $I_D$	$T_A = 25^\circ\text{C}$	390	mA
		$T_A = 70^\circ\text{C}$	310	
Maximum Continuous Body Diode Forward Current (Note 4)	$I_S$	440	mA	
Pulsed Drain Current (Note 5)	$I_{DM}$	800	mA	

**Maximum Ratings Q2 P-CHANNEL** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic	Symbol	Value	Units	
Drain-Source Voltage	$V_{DSS}$	-20	V	
Gate-Source Voltage	$V_{GSS}$	$\pm 8$	V	
Continuous Drain Current (Note 4) $V_{GS} = -4.5\text{V}$	Steady State $I_D$	$T_A = 25^\circ\text{C}$	-310	mA
		$T_A = 70^\circ\text{C}$	-240	
Continuous Drain Current (Note 4) $V_{GS} = -1.8\text{V}$	Steady State $I_D$	$T_A = 25^\circ\text{C}$	-240	mA
		$T_A = 70^\circ\text{C}$	-190	
Continuous Drain Current (Note 4) $V_{GS} = -4.5\text{V}$	t<5s $I_D$	$T_A = 25^\circ\text{C}$	-360	mA
		$T_A = 70^\circ\text{C}$	-280	
Continuous Drain Current (Note 4) $V_{GS} = -1.8\text{V}$	t<5s $I_D$	$T_A = 25^\circ\text{C}$	-280	mA
		$T_A = 70^\circ\text{C}$	-220	
Maximum Continuous Body Diode Forward Current (Note 4)	$I_S$	-440	mA	
Pulsed Drain Current (Note 5)	$I_{DM}$	-800	mA	

- Notes: 4. Device mounted on FR-4 PCB, with minimum recommended pad layout.  
5. Device mounted on minimum recommended pad layout test board, 10 $\mu\text{s}$  pulse duty cycle = 1%.

**Electrical Characteristics Q1 N-CHANNEL** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition	
<b>OFF CHARACTERISTICS (Note 6)</b>							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	@T <sub>c</sub> = 25°C	-	-	100	nA	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
			-	-	50		V <sub>DS</sub> = 5V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±5V, V <sub>DS</sub> = 0V	
<b>ON CHARACTERISTICS (Note 6)</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	0.4	-	1.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	0.60	0.99	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 100mA	
		-	0.75	1.2		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 50mA	
		-	0.90	1.8		V <sub>GS</sub> = 1.8V, I <sub>D</sub> = 20mA	
		-	1.2	2.4		V <sub>GS</sub> = 1.5V, I <sub>D</sub> = 10mA	
		-	2.0	-		V <sub>GS</sub> = 1.2V, I <sub>D</sub> = 1mA	
Forward Transfer Admittance	Y <sub>fs</sub>	180	850	-	mS	V <sub>DS</sub> = 5V, I <sub>D</sub> = 125mA	
Diode Forward Voltage (Note 6)	V <sub>SD</sub>	-	0.6	1.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 10mA	
<b>DYNAMIC CHARACTERISTICS (Note 7)</b>							
Input Capacitance	C <sub>iss</sub>	-	27.6	-	pF	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1.0MHz	
Output Capacitance	C <sub>oss</sub>	-	4.0	-	pF		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	2.8	-	pF		
Gate Resistance	R <sub>G</sub>	-	0.11	-	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz	
Total Gate Charge	Q <sub>g</sub>	-	0.5	-	nC	V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 10V, I <sub>D</sub> = 250mA	
Gate-Source Charge	Q <sub>gs</sub>	-	0.07	-	nC		
Gate-Drain Charge	Q <sub>gd</sub>	-	0.07	-	nC		
Turn-On Delay Time	t <sub>D(on)</sub>	-	4.0	-	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V, R <sub>L</sub> = 47Ω, R <sub>G</sub> = 2Ω, I <sub>D</sub> = 200mA	
Turn-On Rise Time	t <sub>r</sub>	-	3.3	-	ns		
Turn-Off Delay Time	t <sub>D(off)</sub>	-	19.0	-	ns		
Turn-Off Fall Time	t <sub>f</sub>	-	6.4	-	ns		

**Electrical Characteristics Q2 P-CHANNEL** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition	
<b>OFF CHARACTERISTICS (Note 6)</b>							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	@T <sub>c</sub> = 25°C	-	-	100	nA	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V
			-	-	50		V <sub>DS</sub> = -5V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±5V, V <sub>DS</sub> = 0V	
<b>ON CHARACTERISTICS (Note 6)</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	-0.4	-	-1.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	1.2	1.9	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -100mA	
		-	1.5	2.4		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -50mA	
		-	2.1	3.4		V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -20mA	
		-	2.5	5		V <sub>GS</sub> = -1.5V, I <sub>D</sub> = -10mA	
		-	4.0	-		V <sub>GS</sub> = -1.2V, I <sub>D</sub> = -1mA	
Forward Transfer Admittance	Y <sub>fs</sub>	100	450	-	mS	V <sub>DS</sub> = -5V, I <sub>D</sub> = -125mA	
Diode Forward Voltage (Note 6)	V <sub>SD</sub>	-	-0.6	-1.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -10mA	
<b>DYNAMIC CHARACTERISTICS (Note 7)</b>							
Input Capacitance	C <sub>iss</sub>	-	28.7	-	pF	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1.0MHz	
Output Capacitance	C <sub>oss</sub>	-	4.2	-	pF		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	2.9	-	pF		
Gate Resistance	R <sub>G</sub>	-	0.4	-	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz	
Total Gate Charge	Q <sub>g</sub>	-	0.4	-	nC	V <sub>GS</sub> = -4.5V, V <sub>DS</sub> = -10V, I <sub>D</sub> = -250mA	
Gate-Source Charge	Q <sub>gs</sub>	-	0.08	-	nC		
Gate-Drain Charge	Q <sub>gd</sub>	-	0.06	-	nC		
Turn-On Delay Time	t <sub>D(on)</sub>	-	5.8	-	ns	V <sub>DD</sub> = -15V, V <sub>GS</sub> = -4.5V, R <sub>G</sub> = 2Ω, I <sub>D</sub> = -200mA	
Turn-On Rise Time	t <sub>r</sub>	-	5.7	-	ns		
Turn-Off Delay Time	t <sub>D(off)</sub>	-	31.1	-	ns		
Turn-Off Fall Time	t <sub>f</sub>	-	16.4	-	ns		

Notes: 6. Short duration pulse test used to minimize self-heating effect.  
7. Guaranteed by design. Not subject to product testing.

**Q1 N-CHANNEL**

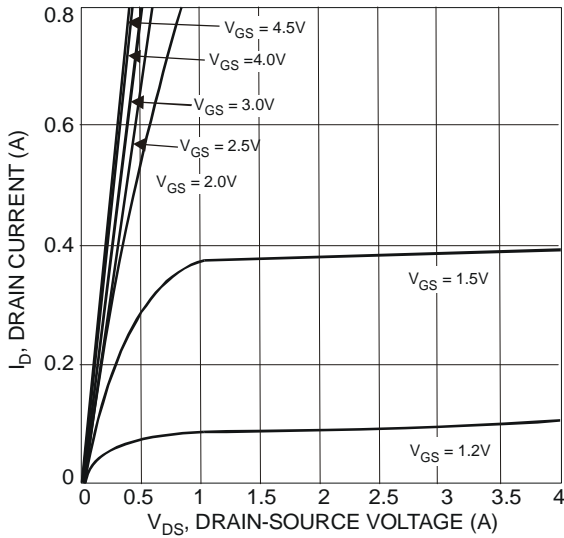


Fig. 1 Typical Output Characteristics

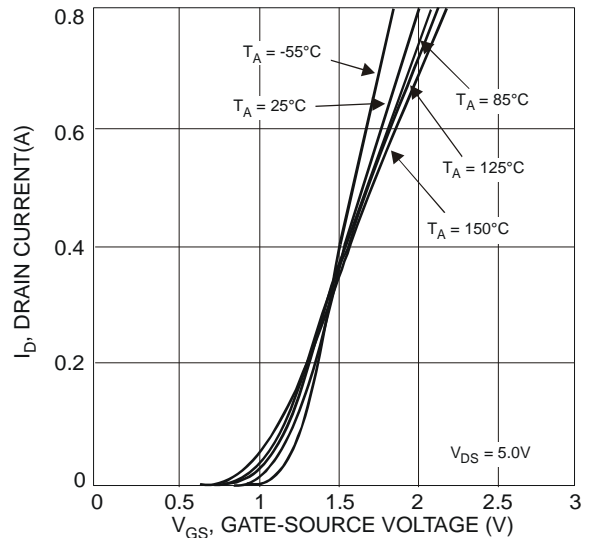


Fig. 2 Typical Transfer Characteristics

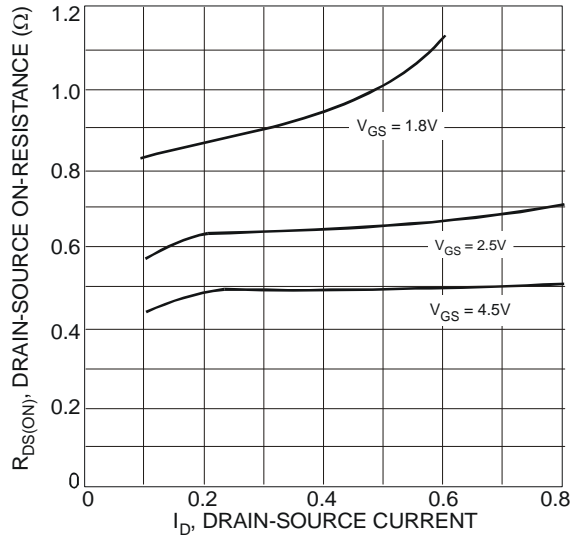


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

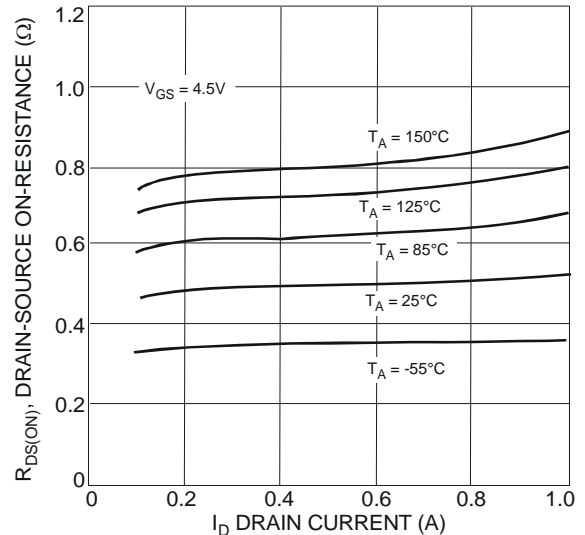


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

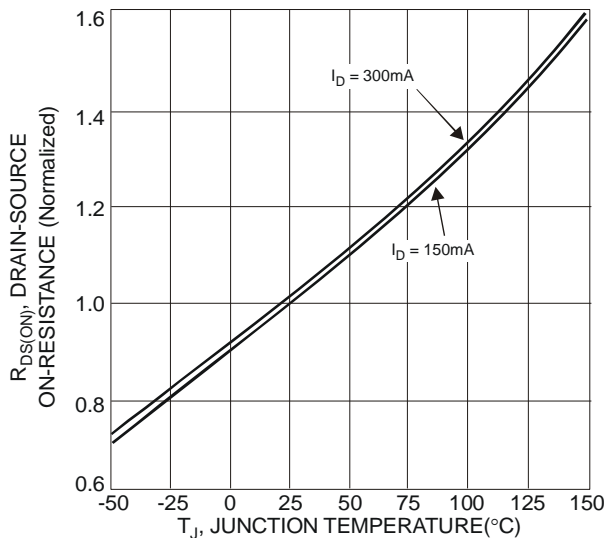


Fig. 5 On-Resistance Variation with Temperature

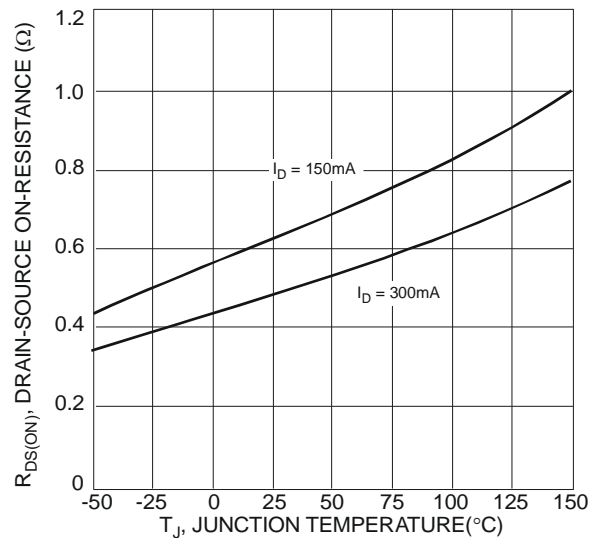


Fig. 6 On-Resistance Variation with Temperature

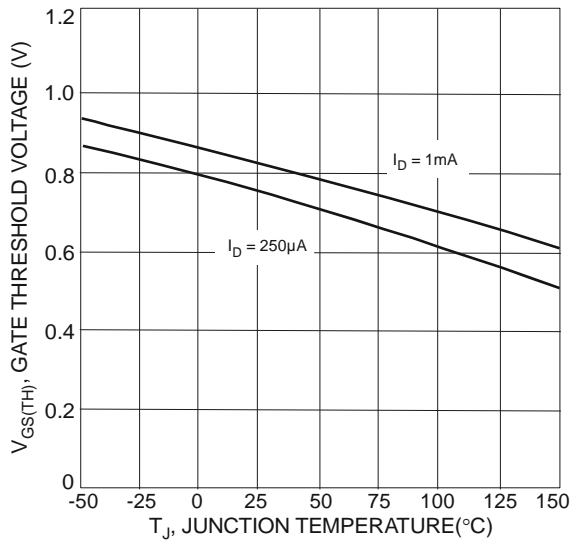


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

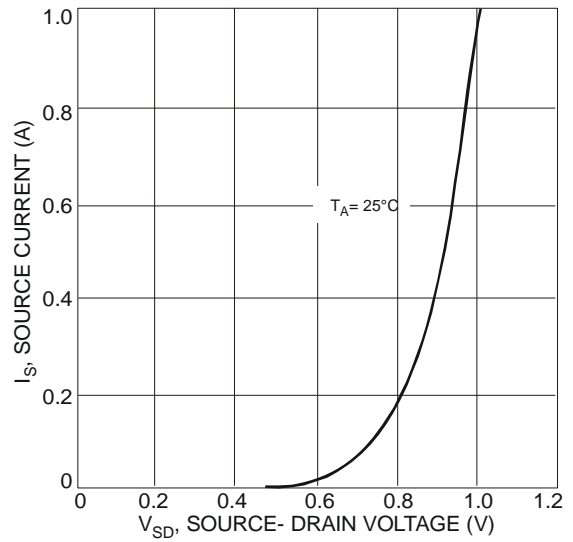


Fig. 8 Diodes Forward Voltage vs. Current

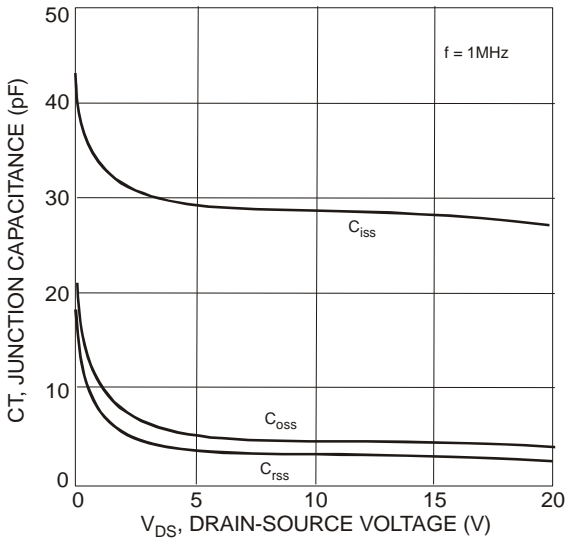


Fig. 9 Typical Junction Capacitance

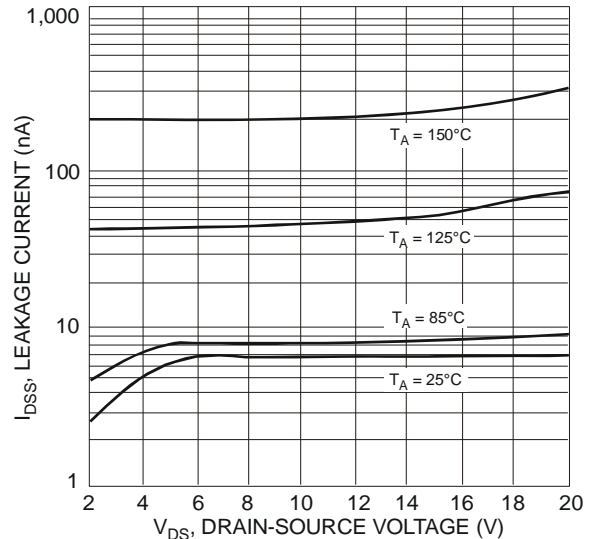


Fig. 10 Typical Drain-Source Leakage Current vs. Voltage

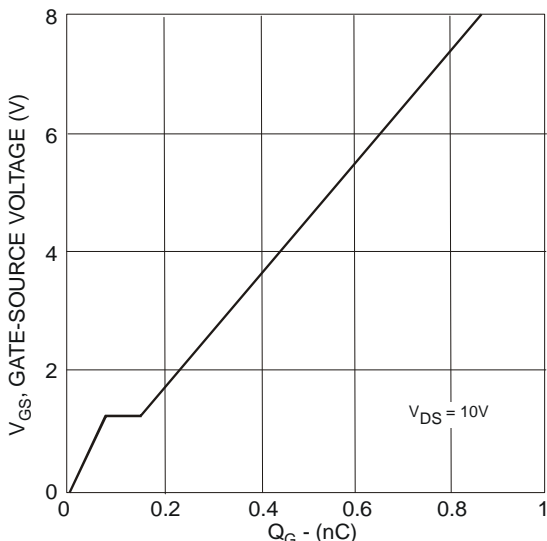


Fig. 11 Gate Charge Characteristics

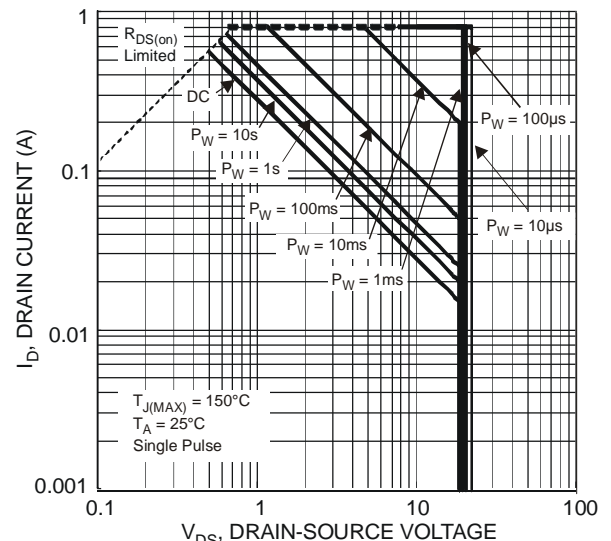


Fig. 12 SOA, Safe Operation Area

**Q2 P-CHANNEL**

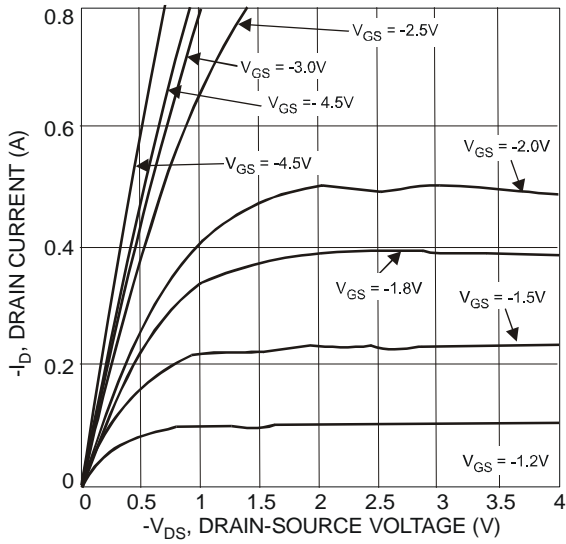


Fig. 13 Typical Output Characteristics

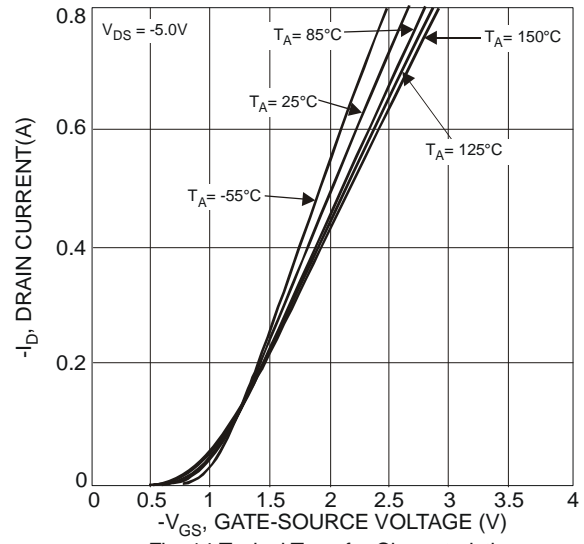


Fig. 14 Typical Transfer Characteristics

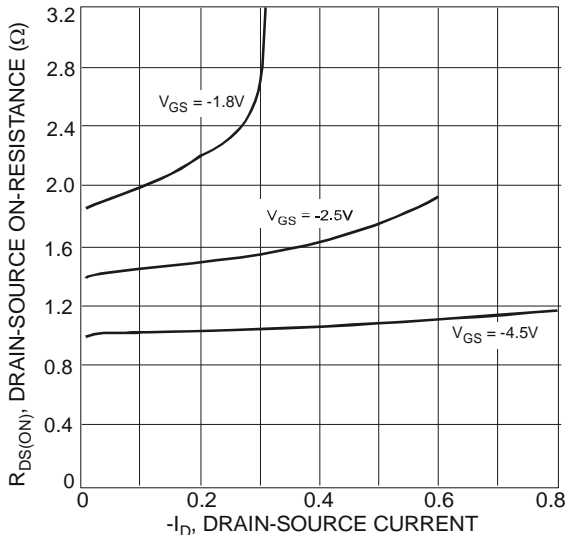


Fig. 15 Typical On-Resistance vs. Drain Current and Gate Voltage

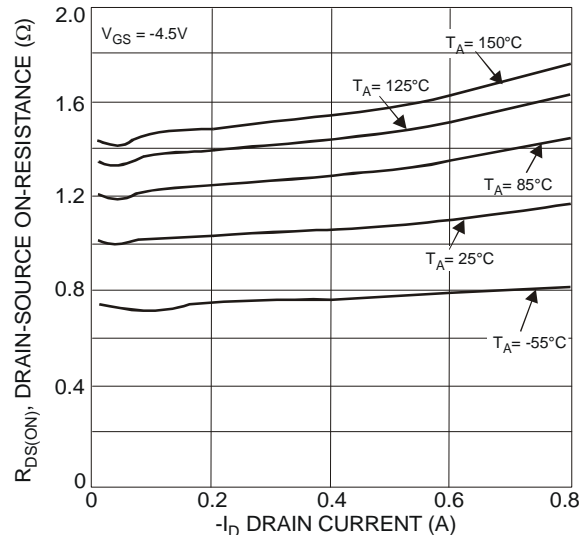


Fig. 16 Typical On-Resistance vs. Drain Current and Temperature

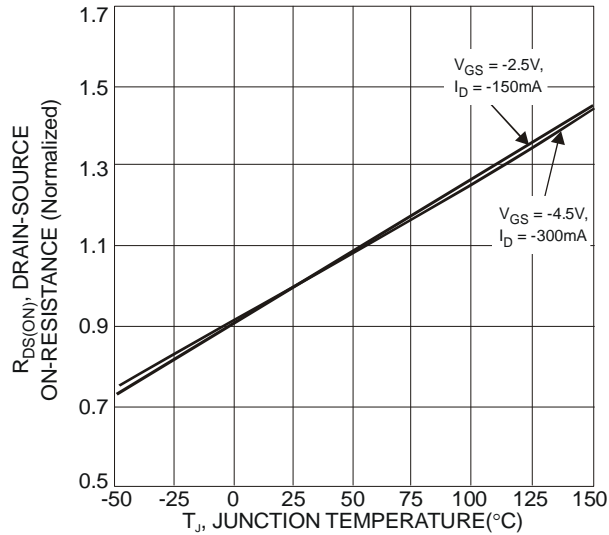


Fig. 17 On-Resistance Variation with Temperature

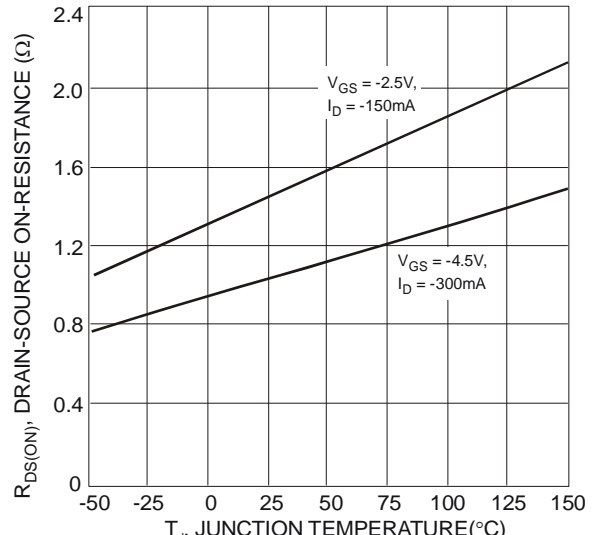


Fig. 18 On-Resistance Variation with Temperature

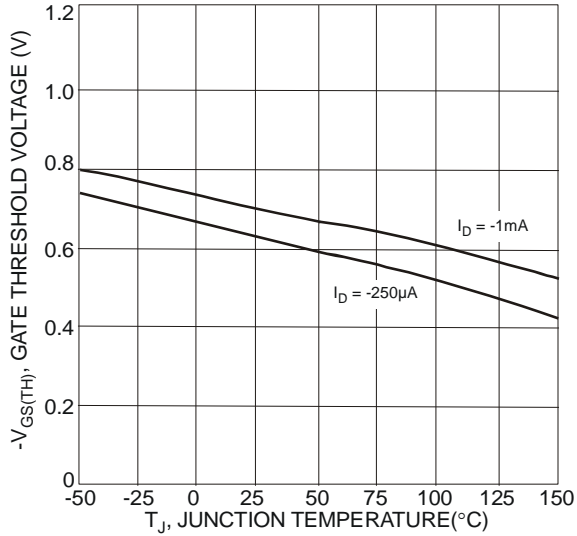


Fig. 19 Gate Threshold Variation vs. Ambient Temperature

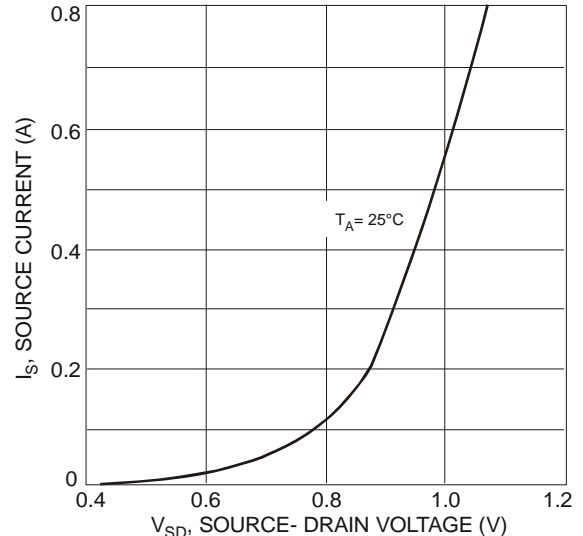


Fig. 20 Diodes Forward Voltage vs. Current

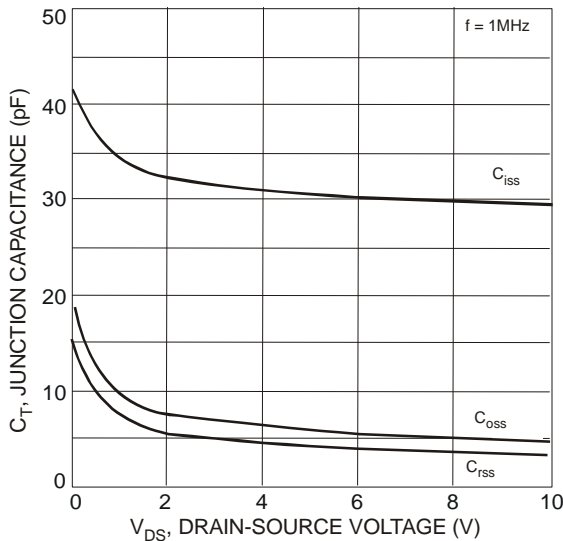


Fig. 21 Typical Junction Capacitance

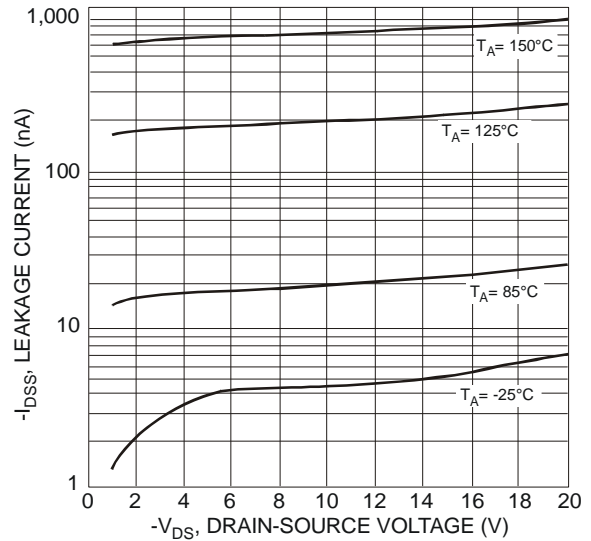


Fig. 22 Typical Leakage Current vs. Drain-Source Voltage

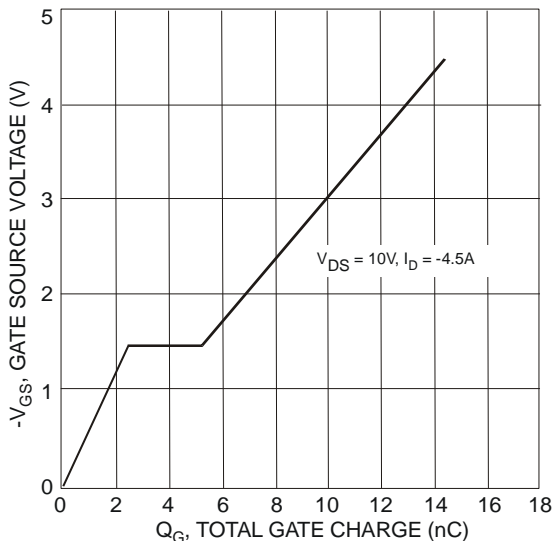


Fig. 23 Gate Charge Characteristics

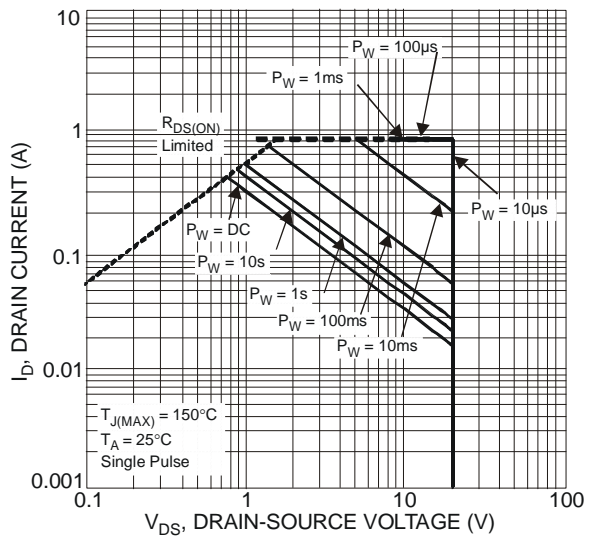


Fig. 24 SOA, Safe Operation Area

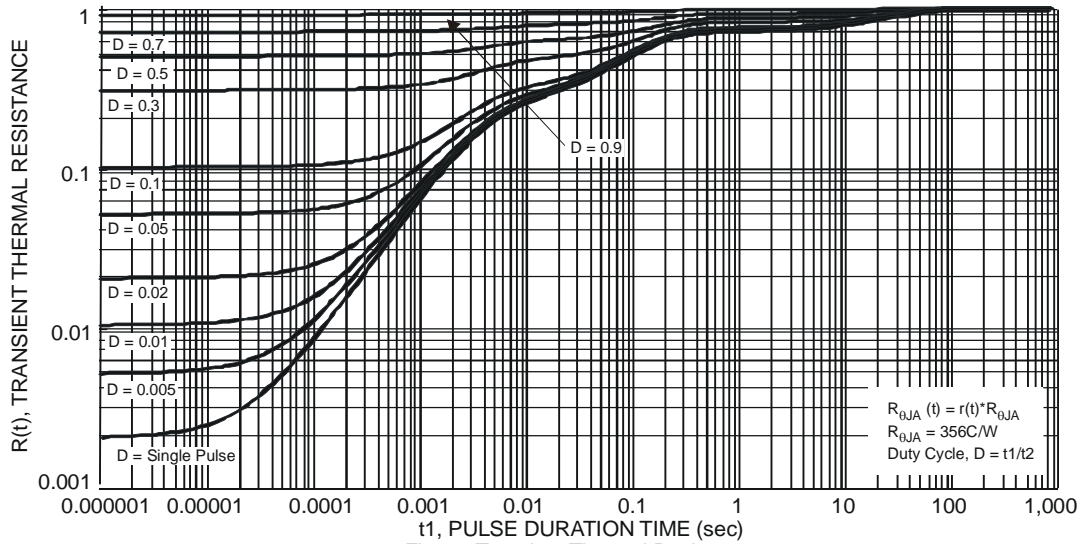
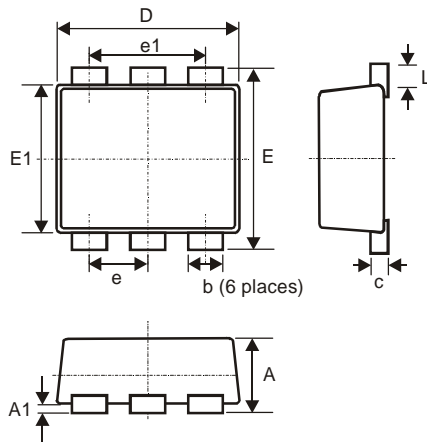


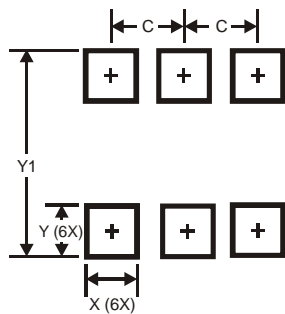
Fig. 25 Transient Thermal Resistance

**Package Outline Dimensions**



SOT963			
Dim	Min	Max	Typ
A	0.40	0.50	0.45
A1	0	0.05	-
c	0.120	0.180	0.150
D	0.95	1.05	1.00
E	0.95	1.05	1.00
E1	0.75	0.85	0.80
L	0.05	0.15	0.10
b	0.10	0.20	0.15
e	0.35 Typ		
e1	0.70 Typ		
All Dimensions in mm			

**Suggested Pad Layout**



Dimensions	Value (in mm)
C	0.350
X	0.200
Y	0.200
Y1	1.100



**IMPORTANT NOTICE**

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

**LIFE SUPPORT**

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

Copyright © 2011, Diodes Incorporated

**[www.diodes.com](http://www.diodes.com)**