HOLT INTEGRATED CIRCUITS INC.

August, 2011

HI-6130 / HI-6131
MIL-STD-1553 / MIL-STD-1760
3.3V BC / MT / RT Multi-Terminal Device

GENERAL DESCPIPTION

The 3.3V CMOS HI-613x device provides a complete single- or multi-function interface between a host processor and MIL-STD-1553B bus. Each IC contains a Bus Controller (BC), a Bus Monitor Terminal (MT) and two independent Remote Terminals (RTs). Any combination of the contained 1553 functions can be enabled for concurrent operation. The enabled terminals communicate with the MIL-STD-1553 buses through a shared on-chip dual bus transceiver and external transformer. The user allocates 64K bytes of on-chip static RAM between devices to suit application requirements.

Two options are offered for host access to internal registers and static RAM: The HI-6130 uses a 16-bit parallel bus; the HI-6131 communicates with the host via a 4-wire serial peripheral interface (SPI). Package options vary, based on host interface I/O pin count:

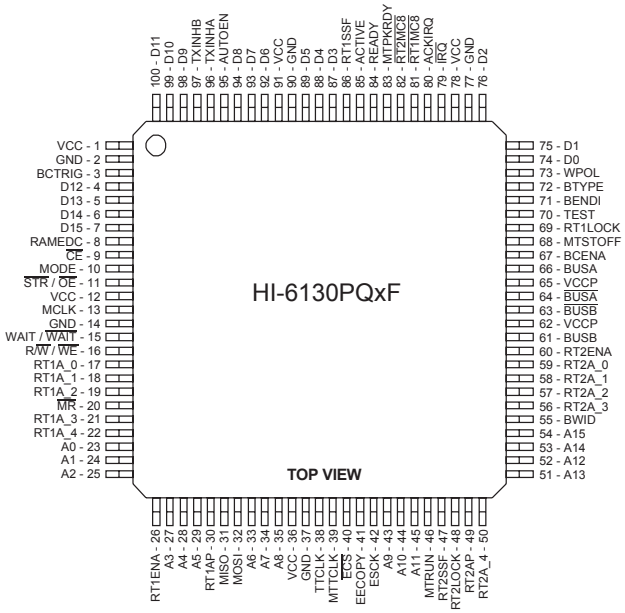
Device	*Host Interface*	*Packages*
HI-6130	16-bit parallel	100-pin PQFP
HI-6131	4-wire SPI	64-pin QFN 64-pin PQFP

Programmable interrupts provide terminal status to the host processor. Circular data stacks in RAM have rollover and programmable “level attained” interrupts. The HI-613x can be configured for automatic self-initialization after reset. A dedicated SPI port reads data from an external serial EEPROM to fully configure registers and RAM for any subset of one to four terminal devices.

FEATURES

- Concurrent multi-terminal operation for one to four MIL-STD-1553B functions: BC, MT and two independent RTs.
- Two host interface options: 16-bit parallel bus for speed, or 4-wire SPI for smaller footprint and interconnect wiring reduction.
- 64K bytes internal static RAM.
- Autonomous terminal operation requires minimal host intervention.
- Shared 1553 bus interface reduces circuit complexity and circuit board area.
- Fully programmable Bus Controller with 28 op code instruction set.
- Bus Monitor can operate in dual-stack mode, recording commands and data separately, with 16-bit or 48-bit time tagging.
- Bus Monitor can record commands and data in single-stack mode, using IRIG-106 Chapter 10 “packet body” format.
- Single-stack Bus Monitor and can optionally generate complete IRIG-106 data packets, including full packet headers and trailers.
- Independent 16-bit time tag counters and clock sources for all terminals. The Bus Controller and Monitor also have 32- and 48-bit time count options, respectively.
- 64-Word Interrupt Log Buffer queues the most recent 32 interrupts. Hardware-assisted interrupt decoding quickly identifies interrupt sources.
- RAM Error Detection/Correction option
- Built-in self-test for protocol logic, digital signal paths and internal RAM.
- Optional self-initialization at reset uses external serial EEPROM
- ±8kV ESD Protection (HBM, all pins).
- Two temperature ranges: -40°C to +85°C, or -55°C to +125°C with optional burn-in.
- RoHS compliant lead-free option.

PIN CONFIGURATION (TOP)



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1. BLOCK DIAGRAM

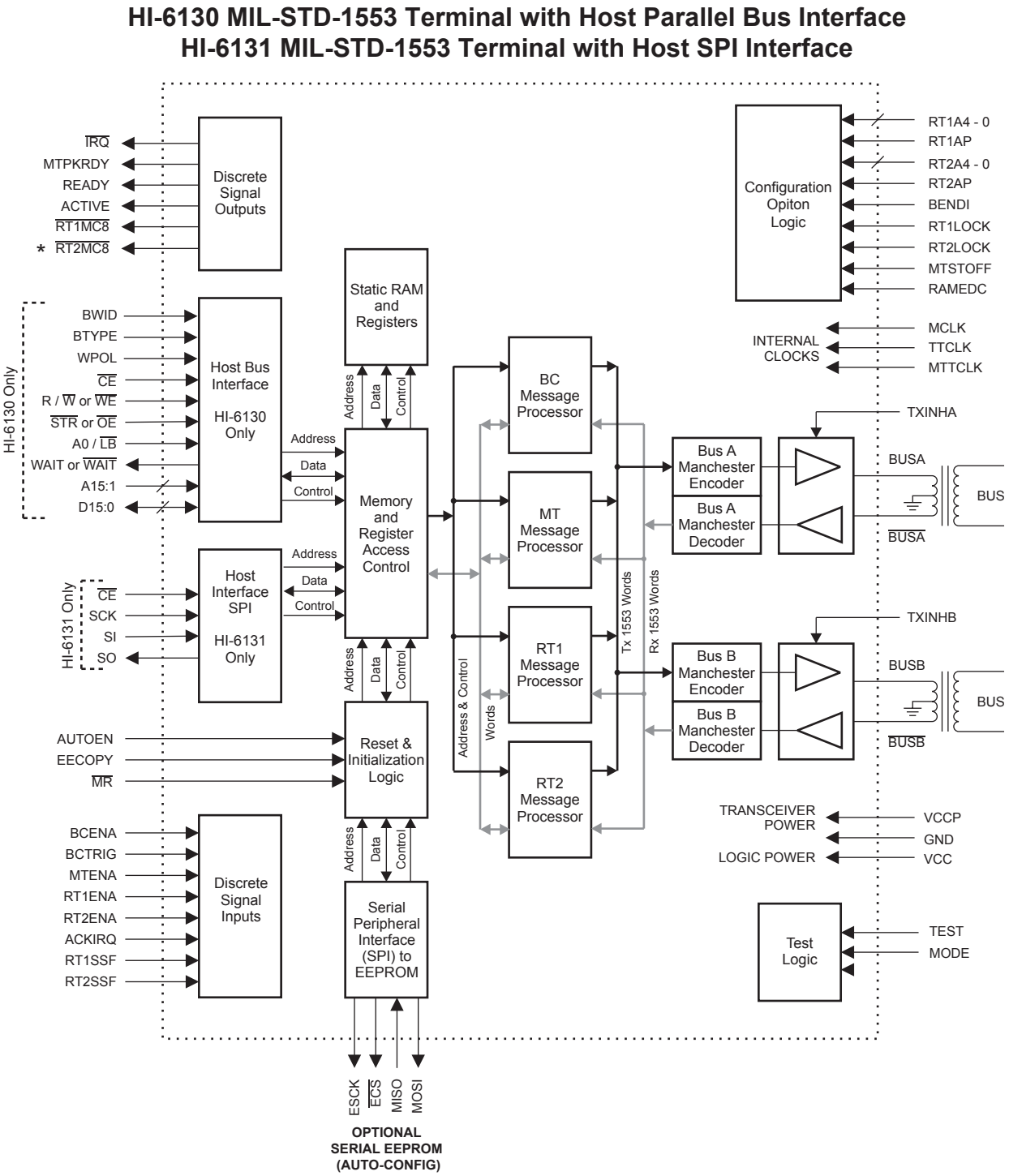

Figure 1. HI-6130 / HI-6131 Block Diagram

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2. FEATURE OVERVIEW

2.1. Bus Controller Operation

The HI-613x is configurable to operate as a Bus Controller (BC). The BC is a programmable message-sequencing device for control in MIL-STD-1553B applications. Programmed using a set of 28 instruction op codes, the BC greatly reduces the host's processing workload. The BC can optionally use a 16- or a 32-bit time base, clocked from a choice of six internally generated clocks, or an external time base clock. Special BC op codes manage all 32-bit time base functions. One internally generated BC time base option clocks the 32-bit BC time counter coincident with the upper 32-bits of the 48-bit MIL-STD-1760 aircraft system time.

The programmable HI-613x Bus Controller autonomously supports multi-frame message scheduling, message retry schemes, storage of message data, asynchronous message insertion and status /error reporting to the host processor.

2.2. Remote Terminal Operation

The HI-613x is configurable to operate one as or two Remote Terminals. The RTs are modeled after the popular Holt HI-6120/21 Remote Terminal. The two Remote Terminals operate with independent characteristics, each RT having fully separate RAM structures (e.g., descriptor and illegal command tables) and independent configuration and status registers. RAM buffer options include single, double and 2 circular buffer choices. The two RTs can be reset and reinitialized independently. The full benefit of two autonomous RTs is achieved while using the same complexity and circuit board area as a single Remote Terminal.

2.3. Monitor Terminal Operation

The Bus Monitor Terminal (MT) passively records MIL-STD-1553 bus activity. Message commands, terminal responses and message data are stored in internal RAM, using either one or two data stacks. Single- and dual-stack MT modes are targeted for different applications. When operating in dual-stack mode, the MT maintains separate command and data stacks. The single-stack HI-613x MT offers expanded message status flags to minimize host processing. The MT can utilize 16- or 48-bit time tags with a range of clocking options.

Single-stack HI-613x Bus Monitor operation is designed to meet data recording requirements of Telemetry Standard RCC Document 106-07, Chapter 10. This "IRIG 106 Chapter 10" data recorder uses 48-bit relative time stamping, having 10MHz (100ns) resolution. Message time stamps occur at one of three selectable message progress points. Several error handling schemes are available. Bus Monitor interrupts notify the host when stack rollover occurs, or when a user-programmed stack level has been reached. The single-stack HI-613x MT stores message records in the assigned stack using IRIG 106 "packet body" format. The device can optionally generate complete IRIG 106 packets, including full packet headers and trailers meeting IRIG 106 Chapter 10 requirements.

2.4. Interrupts

Host interrupts can originate from device hardware or any of the enabled terminal devices (up to 4 devices). A circular 64-word Interrupt Log Buffer retains interrupt information from the last 32 interrupts, while the hardware maintains a count of occurring interrupts since the previous host buffer service.

Hardware-assisted interrupt decoding provides quick identification of the interrupt source by terminal device: BC, MT, RT1, RT2 or hardware. When a hardware interrupt occurs (e.g., Bus A Loopback Failure), a Pending Hardware Interrupt register bit explicitly identifies the interrupt source. For interrupts from BC, MT or RT, the three low-order bits in the same register identify the specific interrupt register (or registers) with pending interrupts: that is, the BC, MT or RT Pending Interrupt registers.

2.5. Reset and Initialization

After hardware Master Reset, there are two HI-613x initialization methods: host initialization or self-initialization from external serial EEPROM. For host initialization, the host processor uses its bus interface or 4-wire SPI to load HI-613x registers and initialize tables, data buffers, etc. in internal static RAM. For self-initialization, the device uses setup information contained within an external serial EEPROM. A dedicated 4-wire SPI port reads data from the serial EEPROM and writes it to registers and RAM. Error checking is performed, looking for data mismatch or an EEPROM checksum error.

Individual 1553 terminal devices (BC, MT, RT1 or RT2) can be re-initialized from the serial EEPROM by writing to the Reset Initialization Register.

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3. PIN DESCRIPTIONS

Table 1. Common pins (Apply to both HI-6130 and HI-6131)

Pin	Function	Description
MCLK	Input 50KΩ pull-down	Master clock input, 50.0MHz +/-100 ppm.
TTCLK MTTCLK	Inputs 50KΩ pull-down	Optional clock input for BC time base and RT time tag counters. Optional clock input for the MT time tag counter. Each function (BC, MT, RT1, RT2) has an independent time tag counter. The BC and RT counters share a common clock, selectable from internally generated frequencies, or an external clock input. The MT time tag counter has its own external or internal clock source.
$\overline{MR}$	Input 50KΩ pull-up	Master reset, active low. The host can also assert software reset by setting bits in the Master Status & Reset register.
TXINHA TXINHB	Inputs 50KΩ pull-down	Transmit inhibit inputs for Bus A and Bus B, active high. These two inputs are logically ORed with the pair of corresponding bits in the Master Configuration Register to enable or inhibit transmit on Bus A or Bus B, affecting behavior for all enabled 1553 devices.
MTSTOFF	Input 50KΩ pull-down	Memory test disable, active high. When this pin is low, the device performs a memory test on the entire RAM after rising edge on the $\overline{MR}$ reset pin. When this pin is high, RAM testing is skipped, resulting in a faster reset process. For further information, refer to the data sheet section entitled “Reset and Initialization.”
AUTOEN	Input 50KΩ pull-down	Auto-Initialize Enable, active high. If this pin is high at rising edge on $\overline{MR}$ reset pin, self-initialization proceeds, copying configuration data to registers and RAM from an external serial EEPROM via a dedicated EEPROM SPI port. Refer to the data sheet section entitled “Reset and Initialization.”
READY	Output	This pin is low when auto-initialization or built-in test is in process. The host cannot read or write device RAM or registers when pin state is low; reads to any address return the value in the Master Status & Reset register. When the AUTOEN pin is low at Master Reset, the host can configure device RAM and registers after READY goes high.
ACTIVE	Output	This pin is high while an enabled BC or RT in the device is processing a 1553 message. The IMTA bit 1 in Master Configuration Register 0x0000 logically-ORs bus monitor (MT) activity as well.
$\overline{ECS}$ ESCK MOSI MISO	Output Output Output Input 50KΩ pull-down	Dedicated 4-wire Serial Peripheral Interface (SPI) for connection to an optional external EEPROM used for automatic self-initialization when AUTOEN is high at Master Reset.
EECOPY	Input 50KΩ pull-down	EEPROM Copy, active high. Asserting this input initiates RAM and register copy into serial EEPROM used for auto-initialization. Refer to the data sheet section entitled “Reset and Initialization.”
BCENA	Input 50KΩ pull-down	Bus Controller Enable input, active high.

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Pin	Function	Description
BCTRIG	Input 50KΩ pull-down	BC Trigger input, active high. Used in conjunction with certain BC instructions.
MTRUN	Input 50KΩ pull-down	Monitor Run / $\overline{\text{Stop}}$ input, active high. This input starts/stops MT data recording. Upon going low, the MT stops when the current message is completed.
RT1ENA RT2ENA	Inputs 50KΩ pull-down	RT Enable input, active high. This input pin is logically ANDed with the STEX Start Execution bit in the RT Configuration Register to allow RT operation.
RT1LOCK RT2LOCK	Inputs 50KΩ pull-down	Pin states are latched to the Lock bit in the RTx Operational Status register when rising edge occurs on the $\overline{\text{MR}}$ pin. If status register Lock bit is high, the host cannot overwrite the terminal address in the same register. If status register Lock bit is low, the host can overwrite the terminal address and parity (and the Lock bit) in the RTx Operational Status register.
$\overline{\text{RT1MC8}}$ $\overline{\text{RT2MC8}}$	Outputs	Remote Terminal “Reset RT” mode command (MC8) received. This active low output is asserted at Status Word completion when RT1 or RT2 received a “Reset Remote Terminal” mode code command. The minimum output pulse width is 100ns, unaffected by $\overline{\text{MR}}$ assertion.
RT1SSF RT2SSF	Inputs 50KΩ pull-down	RT Subsystem Fail input, active high. When this input is high, the selected RT1 or RT2 sets the SUBSYS flag in its transmit status word. This input is logically-ORed with the same bit in the terminal’s RT1 or RT2 1553 Status Word Bits register.
MTPKRDY	Output	Monitor Packet Ready output, active high. This pin is asserted when a message data packet is complete, as defined by the various MT configuration registers (maximum word or message count, maximum packet time, etc.) Assertion of this bit indicates the MT has stopped.
$\overline{\text{IRQ}}$	Output	Interrupt request, active low. This pin is asserted each time an enabled interrupt event occurs. This signal is programmed as a brief low-going pulse output or as a level output by the INTSEL bit in the Master Configuration Register. If level output is selected, $\overline{\text{IRQ}}$ stays low until the host acknowledges $\overline{\text{IRQ}}$ by pulsing a rising edge at the ACKIRQ pin, or by reading the pending interrupt register(s) containing active interrupt flags.
ACKIRQ	Input 50KΩ pull-down	Interrupt Acknowledge, active high. This input is only used when the INTSEL bit in Configuration Register 1 is high, enabling level interrupt assertion for the $\overline{\text{IRQ}}$ pin. When interrupt assertion causes the $\overline{\text{IRQ}}$ pin to go low, a high-going pulse on ACKIRQ (60ns minimum duration) clears the $\overline{\text{IRQ}}$ output to logic 1. Reading all non-zero Pending Interrupt registers also clears the $\overline{\text{IRQ}}$ interrupt output.
RT1A4:0 RT1AP RT2A4:0 RT2AP	Inputs 50KΩ pull-ups	Remote terminal address bits 4 - 0, and parity bit for RT1 and RT2. The RTAP pin provides odd parity for the address on pins RTA4:0. The terminal address and parity pin levels are latched into the respective RT Operational Status Registers when rising edge occurs on the $\overline{\text{MR}}$ pin. The RT Operational Status Register value (not these pins) reflects the active terminal address. The host can overwrite the RT Operational Status register address value only when the register Lock bit is reset.

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Pin	Function	Description
BENDI	Input 50KΩ pull-up	Big Endian configuration pin for selecting “endianness” or byte order, when using byte transfers. Endianness is the system attribute that indicates whether integers are represented with the most significant byte stored at the lowest address (big endian) or at the highest address (little endian). Internal register / RAM storage is “big endian.” When using the HI-6130, this pin only applies when the host parallel bus is configured for 8-bit width, that is, when BWID equals 0. When the HI-6130 is configured for 16-bit bus width, the BENDI input pin is “don’t care.” When using the HI-6131, this pin controls the byte order of transferred 16-bit data following the SPI command. When BENDI is low, “little endian” is chosen; the low order byte (bits 7:0) is transacted on the SPI before the high order byte (bits 15:8). When BENDI is high, “big endian” is chosen and the high order byte is transacted on the SPI before the low order byte.
RAMEDC	Input 50KΩ pull-down	RAM EDC (Error Detection / Correction) enable. When pin is low, device operates with 32K word RAM address space, EDC disabled. When pin is high, device operates with 24K word RAM address space with EDC enabled. All single-bit RAM read errors are automatically corrected. The corrected errors and uncorrectable multi-bit RAM read errors can generate separate, optional interrupts.
TEST	Input 50KΩ pull-down	Test enable input. The host asserts this pin to perform RAM self-test and loop-back tests.
MODE	Input 50KΩ pull-up	Pin used for factory test. Do not connect.
VCC VCCP GND	Power Supply	3.3VDC power supply for logic and bus transceiver.
BUSA $\overline{\text{BUSA}}$	Analog	Bi-directional Bus A interface to external MIL-STD-1553 isolation transformer. Observe positive / negative polarity.
BUSB $\overline{\text{BUSB}}$	Analog	Bi-directional Bus B interface to external MIL-STD-1553 isolation transformer. Observe positive / negative polarity.

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Table 2. Pins that apply to HI-6130 only (Host parallel bus interface)

Pin	Function	Description
$\overline{CE}$	Input 50KΩ pull-up	Chip Enable, active low. When asserted, this pin enables host read or write accesses to device RAM or registers using the host's parallel bus interface. This pin is normally connected to a Chip Select output from the host's bus interface.
D15:0	In / Out 50KΩ pull-down	Tri-state data bus for host read/write operations upon registers and shared RAM. All bus read/write operations transact 16 bit words, but bus width can be configured for 8 or 16 bits. For 8-bit bus width, pins D15:8 are not connected. Sixteen-bit words are transacted over an 8-bit bus as a pair of byte operations, with data presented sequentially on pins D7:0. For compatibility with different host processors when 8-bit bus width is enabled, the BENDI input determines whether the low order byte is transferred before the high order byte, or vice versa.
A14:1 A0 / $\overline{LB}$	Input 50KΩ pull-up	Address bus for host read/write operations upon registers and shared RAM. When using 16-bit bus width, address bit A0 / ($\overline{LB}$) from the host is not used. For 8-bit bus width, output A0 equals 0 during the first byte read/write access; and equals 1 during the second byte access.
BWID	Input 50KΩ pull-up	Configuration pin for host bus width. High selects 16-bit bus width, low selects 8-bit bus width.
BTYPE	Input 50KΩ pull-up	Configuration pin for host bus read/write control signal style. High selects "Intel style" using separate read strobe $\overline{OE}$ (output enable) and write strobe $\overline{WE}$. Low selects "Motorola style" using single active-low read/write strobe $\overline{STR}$ and read/write select signal, R/$\overline{W}$.
R/$\overline{W}$ / $\overline{WE}$	Input 50KΩ pull-up	Read/write direction signal R/$\overline{W}$ when BTYPE pin is low. Active-low Write Enable $\overline{WE}$ when BTYPE pin is high. Used for host read or write accesses to device RAM or registers. This pin or the $\overline{CE}$ pin should be high during all address transitions.
$\overline{STR}$ / $\overline{OE}$	Input 50KΩ pull-up	Active-low common read/write strobe $\overline{STR}$ when BTYPE pin is low. Active-low Output Enable $\overline{OE}$ when BTYPE pin is high. Used for host read or write accesses to device RAM or registers.
WPOL	Input 50KΩ pull-up	Configuration pin for WAIT output polarity. When the WPOL pin is low, the "wait" output is active low ($\overline{WAIT}$). When WPOL is high, the "wait" output is active high (WAIT).

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Pin	Function	Description
WAIT / $\overline{\text{WAIT}}$	Output	Host bus read cycle WAIT or $\overline{\text{WAIT}}$ output. The HI-6130 WPOL input pin sets the active level for this “wait” output. Read cycles are slower than write cycles, but prefetching speeds data availability for multi-word sequential address read cycles. For every new bus read cycle, the HI-6130 asserts WAIT. Connected to the processor WAIT or $\overline{\text{WAIT}}$ input, this action inserts one or more processor wait states (depending on processor clock frequency) while the HI-6130 fetches the first word. After reading each HI-6130 register or RAM address, the device prefetches and retains data from the next address. If the next bus access reads that sequential address, the data is ready without WAIT assertion, even if that read cycle occurs some time later. While the prefetch “chain” is broken by any write cycle, each read cycle prefetches and retains data from the next address, whether or not it is needed. Thus WAIT assertion only occurs for the first word read. The WAIT output is useful when the host processor runs at high clock rates and/or when processor read wait states do not provide adequate timing margin for worst case (slowest) read cycle timing for the HI-6130. Using the WAIT output for the slow, first read cycle means the processor bus interface can be optimized to use faster no-wait cycles for write operations, and for reading words 2 through N in successive address, N-word read operations. Processors lacking a WAIT or $\overline{\text{WAIT}}$ input pin are typically configured to insert a fixed number of wait states for every read/write cycle.

Table 3. Pins that apply to HI-6131 only (Host SPI bus interface)

Pin	Function	Description
$\overline{\text{CE}}$	Input 50KΩ pull-up	Chip Enable, active low. When asserted, this pin enables host read or write accesses to device RAM or registers via host SPI port. The HI-6131 SPI port operates in Slave mode. This pin is connected to the Slave Select output on the host SPI port.
SO	Output	Serial Peripheral Interface (SPI) Serial Output pin. This pin is connected to MISO (Master In - Slave Out) pin on host SPI port. The SO pin is tri-stated when not transmitting serial data to the host.
SI	Input 50KΩ pull-down	Serial Peripheral Interface (SPI) Serial Input pin. This pin is connected to MOSI (Master Out - Slave In) pin on host SPI port.
SCK	Input 50KΩ pull-down	Serial Peripheral Interface (SPI) Serial Clock pin. This pin is connected to SCK output pin on host SPI port.

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4. MEMORY MAP

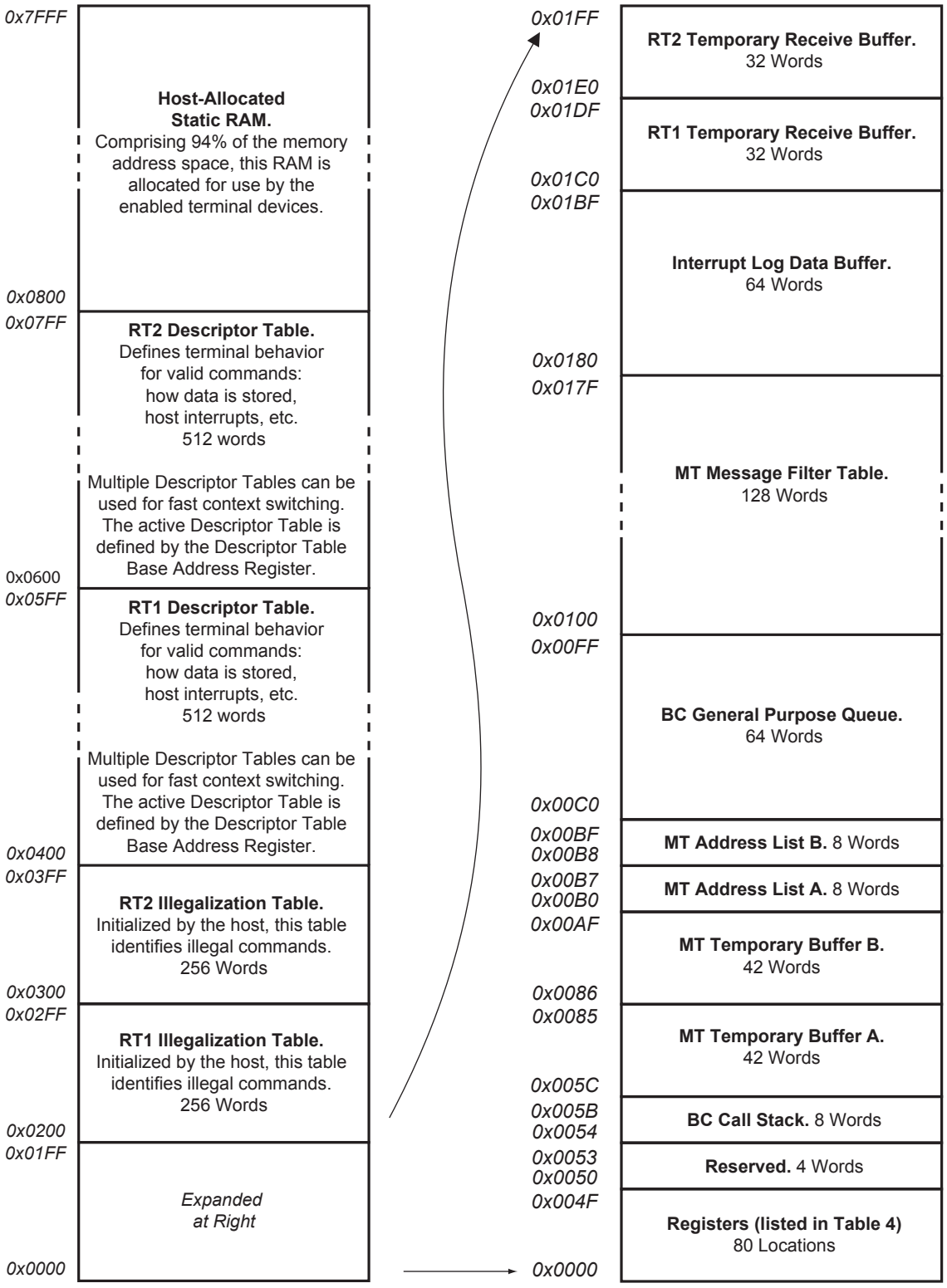

Figure 2. Address Mapping for Registers and RAM

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5. RAM STRUCTURES

Figure 2 shows a memory map for HI-613x memory and registers. Application requirements dictate the specific RAM structures needed. These structures listed here are explained later.

5.1. Interrupt Log Data Buffer

The device maintains information from the last 32 interrupts in a 64-word circular buffer in RAM known as the Interrupt Log. Two 16-bit words characterize each interrupt; one word identifies the interrupt type (Interrupt Identification Word) and one word identifies the command that generated the interrupt (Interrupt Address Word). After reset, the Interrupt Log Address Register contains the fixed buffer start address of 0x0180. After each occurring interrupt, the device updates the register to point to the log address used for the next occurring interrupt.

5.2. Bus Controller (BC) Instruction List

BC message sequencing uses an instruction list, comprised of multiple 2-word entries. Each entry consists of an instruction word (op code plus execution condition code) followed by a parameter word. Some op codes execute unconditionally, but most are conditional, and execute only if the condition code specified in the instruction word tests true. This architecture provides flexibility for message frame scheduling and autonomous BC program execution, based on various conditions.

5.3. Bus Controller (BC) Msg Control / Status Stack

Referenced when a BC Instruction List parameter is an address pointer, the Message Control Status Stack consists of 8- or 16-word control blocks for individual MIL-STD-1553 messages. Within the message control/ status block, execution parameters are provided including inter-message gap, message format, active bus, message command word(s), then address pointer to a message data block in RAM (when the command includes data) and the expected RT status response.

5.4. Bus Controller (BC) Call Stack

When the Bus Controller executes a “subroutine call” op code, the BC Subroutine Call Stack stores the list address for the next op code, to be executed upon return from subroutine. The BC call stack allows 8 levels of nesting.

5.5. Bus Controller (BC) General Purpose Queue

The Bus Controller General Purpose Queue provides a convenient way for the BC to convey information to the external host. Numerous BC op codes push various data onto the queue, including time tag count, data values, message Block Status Word or the data at specific RAM address locations.

5.6. Monitor Terminal Temporary Buffers A & B

The HI-613x Monitor Terminal (MT) has a 42 word receive buffer for each bus. Received command words, status words and data words are temporarily stored in these buffers. At message completion, the recorded data is copied to Monitor Terminal stack(s).

5.7. Monitor Terminal (MT) Stack Address Table

The stack address table contains four addresses each, for the MT command stack and MT data stack. These addresses are: stack start address, stack end address, current address value and a user-written address used for generating a “stack utilization” interrupt.

5.8. Monitor Terminal (MT) Message Filter Table

This 128-word table is optionally used to selectively monitor MIL-STD-1553 messages based on each command’s RT address and subaddress, and the transmit/receive bit status.

5.9. Monitor Terminal (MT) Command & Data Stacks

For applications that include a monitor terminal, the MT operational mode uses either a single Command Stack for recording both commands and data, or a Command Stack plus Data Stack for segregated storage. Stack base address and stack size are programmable. Interrupts can be triggered at stack rollover, or at programmable utilization levels.

5.10. RT1 and RT2 Command Illegalization Tables

For each RT, optional illegal command detection utilizes this table in RAM. The table can illegalize any logical

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combination of 11 command word bits comprising subaddress, the transmit/receive bit and word count (or mode code), plus broadcast vs non-broadcast status, resulting in a total of 4,096 possible combinations. Terminal response to an illegal command sets “Message Error” status and transmits Status Word only. If illegal command detection is not used (that is, no “illegal” entries in Illegalization Table), the terminal responds “in form” to all valid commands.

5.11. RT1 and RT2 Descriptor Tables

For each RT, a host-initialized Descriptor Table in RAM defines how the terminal responds to valid commands. The table is comprised of 128 four-word descriptor blocks. Each of 32 subaddresses and 32 mode code values has one descriptor block for transmit and another for receive. The descriptor table defines message options (interrupt selections, data buffer mode, etc.) and contains pointers to allocated data storage in RAM.

5.12. RT1 and RT2 Temporary Receive Buffers

Remote Terminals RT1 and RT2 temporarily store command and data words during message transaction. At successful message completion, all data is transferred to assigned subaddress buffers. This strategy prevents valid data from being overwritten by incomplete or bad data from a later message ending in error.

5.13. RT Message Data Buffers

Ordinary transmit and receive commands transact from 1 to 32 data words. The host allocates space in RAM for storing transacted message data words as well as message information words.

5.14. RT Storage for Mode Code Commands

In addition to commands used for data transmit and receive, MIL-STD-1553 also defines “mode code commands” for command and control. These “mode commands” transfer a single data word, or no data word at all. The user has the option for storing mode command data in RAM buffers assigned in the Descriptor Table, or stored within the RT Descriptor Table itself. The second option is often preferred for its simplicity.

6. HARDWARE FEATURES

6.1. Remote Terminal Address Inputs

The 5-bit Remote Terminal address is set using pins RTA4:0. The RTAP input pin should be set or reset to present matching odd parity. The state of the RT address and parity pins is latched into the RT Operational Status register upon rising edge on the $\overline{MR}$ master reset input. The state of the LOCK input is latched into the RT Operational Status register at the same time, and controls whether or not the active terminal address and parity in the RT Operational Status register can be overwritten by host writes into the register. When the LOCK input pin is high, autoinitialization cannot overwrite the RT address value latched from the input pins. Between Master Reset assertions, the state of the RTA and RTAP input pins is “don’t care”. If the value of RT address and parity in the RT Operational Status register has parity error, terminal operation is disabled.

6.2. Dual Transceivers for MIL-STD-1553 Bus

Built-in bus transceivers provide direct interface between the device and MIL-STD-1553 bus isolation transformers. The transceivers convert digital data to and from differential Manchester II encoded bus signals. A pair of “transmit inhibit” input pins exercises direct control over transmission for both buses.

6.3. Encoder and Decoders

The device uses separate Manchester II encoders and decoders for each bus. Decoders check for proper sync pulse and Manchester waveform, edge skew, correct number of bits and parity. Encoders are used for transmission. During transmit, each encoded word is looped back through the bus decoder for error checking. Receiver bus sampling is clocked at 50 MHz, providing excellent tolerance to zero-crossing distortion.

6.4. Auto-Initialization Serial EEPROM Interface

The device has an automatic self-initialization feature. If self-initialization is enabled after $\overline{MR}$ master reset, the device reads configuration settings from an external serial EEPROM to initialize registers and RAM structures. A method is provided to initially program or later modify the external serial EEPROM by copying host-loaded tables and register values to the serial EEPROM.

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7. REGISTER & MEMORY ADDRESSING

The HI-613x has an internal address space of 32K 16-bit words. Registers occupy the low 80 locations in this address space. In this data sheet, register / RAM addresses are expressed as hexadecimal numbers, using the C programming convention where the prefix “0x” denotes a hexadecimal value; e.g., 0x00FF represents 00FF hex.

Figure 2 shows address mapping for registers and RAM. All registers and some RAM structures have fixed addresses. Other RAM structures shown are relocatable; Each relocatable structure has a base address register. Figure 2 shows the default locations for relocatable structures. RAM allocations for unused MIL-STD-1553 functions can be reassigned as needed. For example, an application using just a Bus Monitor can reassign all BC and RT RAM for monitor needs.

Device RAM and register address mapping is word oriented, rather than byte oriented. Register and memory addresses throughout this document reflect word addressing. For all parallel bus-interface applications (HI-6130) and most SPI interface applications (HI-6131), word oriented addressing applies. Word oriented addressing uses address inputs A15 to A1; address input A0 is not used. Fifteen bits are sufficient for a 32K address range.

7.1. 8-bit Bus Operation: (HI-6130 Only)

When required by the application, parallel bus interface HI-6130 devices can use byte transfers. All 8-bit microprocessors (and some 16-bit and 32-bit microprocessors) use (or can use) byte-oriented memory accesses. To provide byte capability, the HI-6130 uses the sixteenth bus address input, A0. Thus 16 address pins A15:0 address 64K bytes. The A0 input denotes whether the first or second byte in the word is being addressed, while A15-A1 indicate the word address. This difference must be considered when assigning HI-6130 pointer values or accessing RAM or registers. From the microprocessor’s standpoint, any host-assigned RAM buffer address will be double the value of the buffer’s pointer stored in RAM. This paragraph only applies to HI-6130 using 8-bit bus width. From this point on, all register and memory addresses presented in this data sheet are 15-bit word addresses.

From the host standpoint, register operations and RAM operations are performed identically. Depending on function, individual registers may be read-only, read-write, or a combination of read-only and read-write bit fields. Read-only registers and read-only register bit fields, are protected against accidental host overwrite by device logic.

Addresses in the range 0x004C to 0x7FFF apply to static RAM memory. All RAM is read-write and can be written or read by either the host or the internal device logic. Both host and the device update certain RAM locations (e.g., RT Descriptor Table Control Words). These locations are protected against accidental data collision by arbitration logic which acts when concurrent writes by both host and device occur.

8. REGISTER DEFINITIONS

Residing at the start of the memory address space, 80 addresses are reserved for HI-613x registers. Register addresses overlay the shared RAM address space. Register bits are active high and bit 15 is the most significant.

Table 4 lists all device registers.

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Table 4. Register Summary

Register Number	*Hex Address*	*Used By*	*Register Name*
0	0x0000	All	Master Configuration Register (page 29)
1	0x0001	All	Master Status and Reset Register (page 33)
2	0x0002	RT1	RT1 Current Command Register (and Test Receive Data Register) (page 146)
3	0x0003	RT1	RT1 Current Control Word Address Register (page 147)
4	0x0004	RT2	RT2 Current Command Register (page 146)
5	0x0005	RT2	RT2 Current Control Word Address Register (page 147)
6	0x0006	All	Hardware Pending Interrupt Register (page 38)
7	0x0007	BC	BC Pending Interrupt Register (page 88)
8	0x0008	MT	SMT Pending Interrupt Register (page 109) IMT Pending Interrupt Register (page 138)
9	0x0009	RT1/RT2	RT1 & RT2 Pending Interrupt Register (page 155)
10	0x000A	All	Interrupt Count & Log Address Register (page 37)
11	0x000B	All	Memory Address Pointer 1 (page 47)
12	0x000C	All	Memory Address Pointer 2 (page 47)
13	0x000D	All	Memory Address Pointer 3 (page 47)
14	0x000E	All	Memory Address Pointer 4 (page 47)
15	0x000F	All	Hardware Interrupt Enable Register (page 38)
16	0x0010	BC	BC Interrupt Enable Register (page 88)
17	0x0011	MT	SMT Interrupt Enable Register (page 109) IMT Interrupt Enable Register (page 138)
18	0x0012	RT/RT2	RT1 & RT2 Interrupt Enable Register (page 155)
19	0x0013	All	Hardware Interrupt Output Enable Register (page 38)
20	0x0014	BC	BC Interrupt Output Enable Register (page 88)
21	0x0015	MT	SMT Interrupt Output Enable Register (page 109) IMT Interrupt Output Enable Register (page 138)
22	0x0016	RT1/RT2	RT1 & RT2 Interrupt Output Enable Register (page 155)
23	0x0017	RT1	RT1 Configuration Register (page 142)
24	0x0018	RT1	RT1 Operational Status Register (page 145)
25	0x0019	RT1	RT1 Descriptor Table Base Address Register (page 147)
26	0x001A	RT1	RT1 1553 Status Word Bits Register (page 148)
27	0x001B	RT1	RT1 Current Message Info Word Reg (and BIST Fail Address Reg) (page 149)

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Register Number	*Hex Address*	*Used By*	*Register Name*
28	0x001C	RT1	RT1 Bus A Select Register (page 150)
29	0x001D	RT1	RT1 Bus B Select Register (page 150)
30	0x001E	RT1	RT1 Built-In Test (BIT) Word Register (page 151)
31	0x001F	RT1	RT1 Alternate BIT Word Register (and Test Transmit Data Register) (page 152)
32	0x0020	RT2	RT2 Configuration Register (page 142)
33	0x0021	RT2	RT2 Operational Status Register (page 145)
34	0x0022	RT2	RT2 Descriptor Table Base Address Register (page 147)
35	0x0023	RT2	RT2 1553 Status Word Bits Register (page 148)
36	0x0024	RT2	RT2 Current Message Info Word Reg (also: Memory Test Fail Addr) (page 149)
37	0x0025	RT2	RT2 Bus A Select Register (page 150)
38	0x0026	RT2	RT2 Bus B Select Register (page 150)
39	0x0027	RT2	RT2 Built-In Test (BIT) Word Register (page 151)
40	0x0028	RT2	RT2 Alt. BIT Word Register (and Loopback/BIST Test Control Reg) (page 152)
41	0x0029	MT	SMT (Bus Monitor) Configuration Register (page 101) IMT (Bus Monitor) Configuration Register (page 126)
42	0x002A	MT	IMT Packet Maximum Message Count (page 131)
43	0x002B	MT	IMT Packet Maximum 1553 Word Count (page 131)
44	0x002C	MT	IMT Packet Maximum Time (page 132)
45	0x002D	MT	IMT Packet Maximum Gap Time (page 132)
46	0x002E	MT	IMT Channel ID Register (single-stack IRIG 106 only) (page 133)
47	0x002F	MT	SMT Address List Start Address Register (page 104) IMT Address List Start Address Register (page 130)
48	0x0030	MT	SMT Next Message Stack Address Pointer (page 105) IMT Next Message Stack Address Pointer (page 130)
49	0x0031	MT	SMT Last Message Stack Address Register (page 104) IMT Last Message Stack Address Register (page 130)
50	0x0032	BC	BC Configuration Register (page 71)
51	0x0033	BC	Start Address Register for BC Instruction List (page 80)
52	0x0034	BC	BC Instruction List Pointer (page 80)
53	0x0035	BC	BC Frame Time Remaining Register (page 81)
54	0x0036	BC	BC Time to Next Message Register (page 81)

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Register Number	*Hex Address*	*Used By*	*Register Name*
55	0x0037	BC	BC Condition Code (page 81) BC General Purpose Flag Register (page 84)
56	0x0038	BC	BC General Purpose Queue Pointer Register (page 84)
57	0x0039	All	Time Tag Counter Configuration Register (page 43)
58	0x003A	MT	SMT Time Tag Counter Low (page 105) IMT Time Tag Counter Low (page 134)
59	0x003B	MT	SMT Time Tag Counter Mid (page 105) IMT Time Tag Counter Mid (page 134)
60	0x003C	MT	SMT Time Tag Counter High (page 105) IMT Time Tag Counter High (page 134)
61	0x003D	MT	SMT Time Tag Utility Register Low (count load or capture) (page 106) IMT Time Tag Utility Register Low (count load or capture) (page 134)
62	0x003E	MT	SMT Time Tag Utility Register Mid (count load or capture) (page 106) IMT Time Tag Utility Register Mid (count load or capture) (page 135)
63	0x003F	MT	SMT Time Tag Utility Register High (count load or capture) (page 106) IMT Time Tag Utility Register High (count load or capture) (page 135)
64	0x0040	MT	SMT Time Tag Match Register Low (count match interrupt) (page 107) IMT Time Tag Match Register Low (count match interrupt) (page 135)
65	0x0041	MT	SMT Time Tag Match Register Mid (count match interrupt) (page 107) IMT Time Tag Match Register Mid (count match interrupt) (page 135)
66	0x0042	MT	SMT Time Tag Match Register High (count match interrupt) (page 107) IMT Time Tag Match Register High (count match interrupt) (page 136)
67	0x0043	BC	BC Time Tag Counter Low (page 85)
68	0x0044	BC	BC Time Tag Counter High (page 85)
69	0x0045	BC	BC Time Tag Utility Register Low (count load or capture) (page 86)
70	0x0046	BC	BC Time Tag Utility Register High (count load or capture) (page 86)
71	0x0047	BC	BC Time Tag Match Register Low (count match interrupt) (page 86)
72	0x0048	BC	BC Time Tag Match Register High (count match interrupt) (page 86)
73	0x0049	RT1	RT1 Time Tag Counter (page 152)
74	0x004A	RT1	RT1 Time Tag Utility Register (count load / count match interrupt) (page 153)
75	0x004B	RT2	RT2 Time Tag Counter (page 152)
76	0x004C	RT2	RT2 Time Tag Utility Register (count load / count match interrupt) (page 153)
77	0x004D	Test	Factory Test Control Register
78	0x004E	----	Checksum Fail Address & EEPROM Lock/Unlock

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Register Number	*Hex Address*	*Used By*	*Register Name*
79	0x004F	BC	BC Last Message Block Address
80	0x0050	BC	Default location for BC WMI address pointer

Register descriptions are grouped by function: Bus Controller, Bus Monitor, Remote Terminal. Here is the presentation order:

1. Registers used by all device functions (configuration, status and time tag registers),
2. Bus Controller registers,
3. Bus Controller configuration and operation,
4. Bus Monitor registers,
5. Bus Monitor configuration and operation,
6. Remote Terminal registers,
7. Remote Terminal configuration and operation

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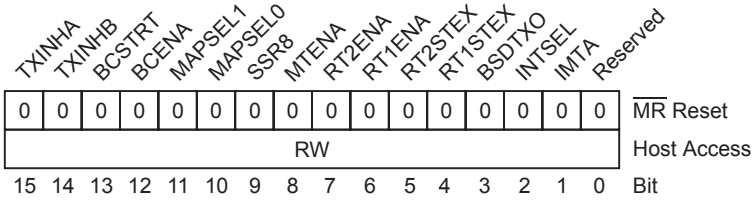
9. REGISTERS USED BY ALL DEVICE FUNCTIONS

9.1. Master Configuration Register (0x0000)



All bits in this 16-bit register are read-write and are fully maintained by the host. This register is cleared after $\overline{MR}$ pin master reset, and is unaffected by assertion of the MTRESET, RT1RESET or RT2RESET bits in the Master Status and Reset Register (0x0001).

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	TXINHA	R/W	0	Transmit Inhibit Bus A. This bit is logically ORed with the TXINHA input pin. This register bit and the corresponding TXINHA pin globally affect all enabled 1553 devices (BC, MT, RT). This inhibit disables all transmission on Bus A.
14	TXINHB	R/W	0	Transmit Inhibit Bus B. This bit is logically ORed with the TXINHB input pin. This register bit and the corresponding TXINHB pin globally affect all enabled 1553 devices (BC, MT, RT). This inhibit disables all transmission on Bus B.
13	BCSTRT	R/W	0	Bus Controller Start. If the BCENA input pin and BCENA register bit are both logic 1, a host write which sets this bit to 1 begins Bus Controller operation. When written to 1, this bit self-resets to 0. This bit always reads back at logic 0 state.
12	BCENA	R/W	0	Bus Controller Enable. This bit is logically ANDed with the BCENA input pin. If either the input pin or this register bit is logic 0, Bus Controller operation is disabled. The BCENA input pin should be connected to ground in applications not using BC mode. This bit cannot be set if BCENA input pin = 0. When the BCENA pin and BCENA register bit are both logic 1, the Bus Controller device is enabled, but BC operation does not begin until BCSTRT bit 13 is set. If this register bit or the BCENA input pin becomes logic 0 while BC operation is underway, BC operation is immediately terminated without waiting for message completion.

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>11 – 10</td><td>MAPSEL1:0
(HI-6130 only)</td><td>R/W</td><td>0</td><td>MAP (Memory Address Pointer) Select.
This 2-bit field only applies to the HI-6131 with SPI host interface. The host SPI relies on a hardware memory address pointer for many SPI register or RAM accesses. This 2-bit field specifies which MAP is active for SPI transactions:
<table>
<tr><th>Register Bit 11-10</th><th>Active Map</th><th>MAP Register Address</th><th>Enabling SPI Op Code</th></tr>
<tr><td>0-0</td><td>MAP1</td><td>0x000B</td><td>0xD8</td></tr>
<tr><td>0-1</td><td>MAP2</td><td>0x000C</td><td>0xD9</td></tr>
<tr><td>1-0</td><td>MAP3</td><td>0x000D</td><td>0xDA</td></tr>
<tr><td>1-1</td><td>MAP4</td><td>0x000E</td><td>0xDB</td></tr>
</table>
The full 16-bit register can be directly written by the host using SPI op code 0x10, followed by 16-bit data word. An alternative method uses SPI op codes 0xD8 – 0xDA that write just the 2-bit MAPSEL field, without affecting other register data. These four SPI op codes only require transmission of an 8-bit instruction, without accompanying data.
Note: “Fast access” SPI op codes contain embedded register addresses and use a separate memory address pointer. This preserves values contained in MAP1 through MAP4. The “fast access MAP” cannot be read by the host but is written each time a “fast access” op code is processed. Fast Access op codes are provided for these SPI operations:
• SPI reads to register addresses 0 through 0x000F (decimal 15)
• SPI writes to register addresses 0 through 0x003F (decimal 63)</td></tr>
<tr><td>9</td><td>SSR8
(HI-6130 only)</td><td>R/W</td><td>0</td><td>Single-Strobe Read for 8-Bit Parallel Bus.
This option only applies to HI-6130 devices with host parallel bus interface configured for 8-bit bus width. When performing 2-byte memory read accesses, some microprocessors with 8-bit bus assert separate Read_Enable (or STROBE) pulses for high and low bytes. Other microprocessors assert a single, wider Read_Enable (or STROBE) pulse, while simply changing the low address bit (A0 / LB) to access the two bytes. For this last case, the SSRD8 bit should be set when writing device configuration, before the first register or RAM read access is performed.</td></tr>
<tr><td>8</td><td>MTENA</td><td>R/W</td><td>0</td><td>Bus Monitor Enable.
This bit is logically ANDed with the MTENA input pin. If input pin or register bit equals logic 0, Bus Monitor operation is disabled. The MTENA input pin should be connected to ground in applications not using monitor mode.
When the pin and MTENA register bit are both logic 1, the Bus Monitor is enabled, Operation commences when the receiver first decodes MIL-STD-1553 activity meeting the “start record” criteria selected by bits 6:5 in the MT Configuration Register. If monitor operation is underway when the MTENA register bit or input pin becomes logic 0, monitor operation stops after completion of any message already underway; monitor resumes when the MTENA register bit and input pin are both logic 1.</td></tr>
</table>

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Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
7	RT2ENA	R/W	0	Remote Terminal 2 Enable. This bit is logically ANDed with the RT2ENA input pin. If input pin or register bit equals logic 0, RT2 operation is disabled. The RT2ENA input pin should be connected to ground in applications not using Remote Terminal 2. This bit cannot be set if RT2ENA input pin = 0. When the register bit and RT2ENA input pin are both logic 1, Remote Terminal 2 is enabled, but operation is controlled by the state of the RT2STEX register bit.
6	RT1ENA	R/W	0	Remote Terminal 1 Enable. This bit is logically ANDed with the RT1ENA input pin. If input pin or register bit equals logic 0, RT1 operation is disabled. The RT1ENA input pin should be connected to ground in applications not using Remote Terminal 1. This bit cannot be set if RT1ENA input pin = 0. When the register bit and RT1ENA input pin are both logic 1, Remote Terminal 1 is enabled, but operation is controlled by the state of the RT1STEX register bit.
5	RT2STEX	R/W	0	Remote Terminal 2 Start Execution. If register bit 7 and the RT2ENA input pin are both logic 1, setting this bit begins Remote Terminal 2 operation. Once running, resetting this bit (or the RT2ENA register bit or RT2ENA input pin) immediately stops RT2 operation.
4	RT1STEX	R/W	0	Remote Terminal 1 Start Execution. If register bit 6 and the RT1ENA input pin are both logic 1, setting this bit begins Remote Terminal 1 operation. Once running, resetting this bit (or the RT1ENA register bit or RT1ENA input pin) immediately stops RT1 operation.

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Bit No.	Mnemonic	R/W	Reset	Function
3	BSDTXO	R/W	0	Bus Shutdown Transmit Only. The bit only applies when Remote Terminal RT1 and/or RT2 is enabled. The BSDTXO bit determines how a 1553 bus inhibit works when (a) the RTxINHA or RTxINHB bit is set in the RT Configuration Register, or (b) the RT receives a valid “bus shutdown” mode code command, either MC4 or MC21: • When the BSDTXO bit is reset, logic 1 for an RTxINHA or RTxINHB bit in a RT Configuration Register (or a “bus shutdown” mode command with auto shutdown enabled) **inhibits both transmit and receive** on the selected bus. • When the BSDTXO bit is set, logic 1 for an RTxINHA or RTxINHB bit in a RT Configuration Register (or a “bus shutdown” mode command with auto shutdown enabled) **inhibits transmit only** on the selected bus; but receive functions are unaffected. Valid commands are heeded, but the RT transmits no responses. **NOT RECOMMENDED**. The HI-613x RT1 and RT2 automatically fulfill unconditional MC4 “bus shutdown” in accordance with the BSDTXO setting, as well as MC5 “override bus shutdown.” The AUTOBSD bit in the RT Configuration Register determines whether conditional MC20 “selected bus shutdown” and MC21 “override selected bus shutdown” are fulfilled automatically, or by host writes to the RTxINHA or RTxINHB bits in the appropriate RT Configuration Register: • When the AUTOBSD bit is logic 0 in the RT1 or RT2 Configuration Register, **automatic fulfillment is disabled** for MC20 “selected bus shutdown” and MC21 “override selected bus shutdown” mode commands. The host fulfills bus shutdown and override by writing the RTxINHA and RTxINHB bits in the appropriate RT Configuration Register. • When the AUTOBSD bit is logic 1 in the RT1 or RT2 Configuration Register, **automatic fulfillment is enabled** for MC20 “selected bus shutdown” and MC21 “override selected bus shutdown” mode commands. When the received mode data word matches the value stored in the RT “Bus A (or B) Select” register, the RT automatically fulfills MC20 “selected bus shutdown” in accordance with the BSDTXO setting, as well as MC21 “override selected bus shutdown”. Auto-shutdown bypasses the RTxINHA and RTxINHB bits in the RT Configuration Register, but the upper 4 bits in the RT’s BIT Word register indicate Tx and Rx bus shutdown status.
2	INTSEL	R/W	0	IRQ Output Type Select. When this bit is 0, the $\overline{\text{IRQ}}$ (interrupt request) output generates a 1µs negative pulse when enabled interrupt events occur. When this bit is logic 1, the $\overline{\text{IRQ}}$ output consists of a continuous low level output requiring host action to negate $\overline{\text{IRQ}}$ to the high state. The host can negate $\overline{\text{IRQ}}$ by asserting the IRQACK input 250ns minimum, or by reading the pending interrupt register(s) containing one or more interrupt-identification bits.

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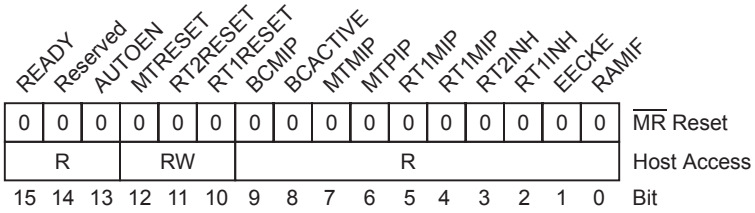
Bit No.	Mnemonic	R/W	Reset	Function
1	IMTA	R/W	0	Indicate MT Activity. When this bit equals 0, the ACTIVE status output is not asserted for Bus Monitor activity, unless the monitored message involves another on-chip terminal). When this bit equals 1, enabled Bus Monitor activity is logically-ORed with the activity of the other on-chip devices to determine ACTIVE status; the ACTIVE output is asserted during such Bus Monitor activity, whether or not the monitored message involves another on-chip terminal.
0	Reserved	-	-	This bit is not used and reads logic 0.

9.2. Master Status and Reset Register (0x0001)



This 16-bit register has a combination of read only and read-write bits. This register is cleared after $\overline{MR}$ pin master reset, but is unaffected by assertion of MTRESET, RT1RESET or RT2RESET register bits.

Bit No.	Mnemonic	R/W	Reset	Function
15	READY	R	0	The READY output pin reflects the state of this register bit. READY is low when auto-initialization, a soft reset caused by bit 12~10 assertion, or built-in test is underway. Host access to device registers or RAM is locked out while READY is low. While READY = 0, any host read access returns the value in this register, regardless of address provided. When READY goes high, the host may access registers and RAM.
14	Reserved	R	0	This bit is not used.
13	AUTOEN	R	0	Auto-Initialization Enable Status. This bit reflects the state of the AUTOEN input pin that applied at the rising edge on the $\overline{MR}$ Master Reset input pin. If the register bit is high, auto-initialization was performed following $\overline{MR}$ reset.
12	MTRESET	R/W	0	Bus Monitor Reset. When written to logic 1, this bit initiates Bus Monitor reset. This bit remains high until reset is complete. While this bit remains high, the READY output pin and register bit 15 are held low, host RAM and register access is suspended. While READY = 0, any host read access returns the value in this register, regardless of address provided. Upon reset completion, this bit self-clears to logic 0, the READY pin goes high and host read/write access is restored.

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Bit No.	Mnemonic	R/W	Reset	Function
11	RT2RESET	R/W	0	Remote Terminal 2 Reset. When written to logic 1, this bit initiates RT2 reset by clearing the STEX Start Execution bit in the RT2 Configuration Register, then performing the RT soft reset actions described in the section entitled, “Reset and Initialization”. This bit remains high until reset is complete. While this bit remains high, the READY output pin and register bit 15 are held low, host RAM and register access is suspended. While READY = 0, any host read access returns the value in this register, regardless of address provided. Upon reset completion, this bit self-clears to logic 0, the READY pin goes high and host read/write access is restored.
10	RT1RESET	R/W	0	Remote Terminal 1 Reset. When written to logic 1, this bit initiates RT1 reset by clearing the STEX Start Execution bit in the RT1 Configuration Register, then performing the RT soft reset actions described in the section entitled, “Reset and Initialization”. This bit remains high until reset is complete. While this bit remains high, the READY output pin and register bit 15 are held low, host RAM and register access is suspended. While READY = 0, any host read access returns the value in this register, regardless of address provided. Upon reset completion, this bit self-clears to logic 0, the READY pin goes high and host read/write access is restored.
9	BCMIP	R	0	BC Message in Process. This bit is high when the BC is processing a MIL-STD-1553 message. Falling edge occurs at message completion, after register and RAM buffer updates.
8	BCACTIVE	R	0	BC Active. This bit is high when the BC is enabled and running. It will read logic 1 during MIL-STD-1553 message processing and during programmed delays.
7	MTMIP	R	0	Bus Monitor Message in Process. This bit is set when a valid MIL-STD-1553 command is decoded, and is reset upon monitored message completion.
6	MTPIP	R	0	Bus Monitor Packet in Process. This bit is set at start of a data packet and is reset when the packet is deemed complete.
5	RT2MIP	R	0	Remote Terminal 2 Message in Process. This bit is set when a valid MIL-STD-1553 command is decoded for RT2, and is reset upon message completion.
4	RT1MIP	R	0	Remote Terminal 1 Message in Process. This bit is set when a valid MIL-STD-1553 command is decoded for RT1, and is reset upon message completion.

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Bit No.	Mnemonic	R/W	Reset	Function
3	RT2INH	R	0	Remote Terminal 2 Bus Inhibited. This bit is high when one bus is inhibited for RT2 due to execution of a "bus shutdown" mode code command. The shut-down bus is identified in the RT2 BIT (built-in test) Word Register. Shut-down can be ended by "bus shutdown override" mode code command, $\overline{MR}$ reset or setting the RT2RESET bit in this register.
2	RT1INH	R	0	Remote Terminal 1 Bus Inhibited. This bit is high when one bus is inhibited for RT1 due to execution of a "bus shutdown" mode code command. The shut-down bus is identified in the RT1 BIT (built-in test) Word Register. Shut-down can be ended by "bus shutdown override" mode code command, $\overline{MR}$ reset or setting the RT1RESET bit in this register.
1	EECKE	R	0	EEPROM Checksum Error. This function only applies when the AUTOEN input pin is logic 1 at rising edge of $\overline{MR}$ Master Reset. This enables auto-initialization from serial EEPROM, as well as RT or MT soft reset with auto-initialization. The EECKE bit is set (as well as bit 14 in the Hardware Pending Interrupt Register, 0x0006) when a serial EEPROM checksum failure occurs. Such failure may occur during full auto-initialization after $\overline{MR}$ master reset, or during execution of a partial, terminal-specific reset after assertion of the RT1RESET, RT2RESET or MTRESET bits in this register.
0	RAMIF	R	0	RAM Initialization Fail Interrupt. This function only applies when the AUTOEN input pin is logic 1 at rising edge of $\overline{MR}$ Master Reset. This enables auto-initialization from serial EEPROM, as well as terminal-specific partial auto-initialization during RT or MT soft reset. The RAMIF bit is set (as well as bit 13 in the Hardware Pending Interrupt Register, 0x0006) when one or more initialized RAM locations do not match their two corresponding serial EEPROM byte locations. Such failure may occur during full auto-initialization after $\overline{MR}$ master reset, or during execution of a partial, terminal-specific reset after assertion of the RT1RESET, RT2RESET or MTRESET bits in this register.

9.3. Hardware Interrupt Registers and the Interrupt Log Buffer

Thirteen HI-613x registers are used for host interrupt management. There are four 3-register groups, separated by function. One register triplet is used for Hardware interrupts, plus one register triplet each for Bus Controller, Bus Monitor and Remote Terminal interrupts. Each group (BC, MT, RT, Hardware) has

- An Interrupt Enable Register to enable and disable interrupts
- A Pending Interrupt Register to capture the occurrence of enabled interrupts
- An Interrupt Output Enable Register to also enable $\overline{IRQ}$ output to the host, for interrupts enabled in the Interrupt Enable Register

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The BC, RT and MT register triplets are described in the respective data sheet sections dedicated to each of those terminal functions. This data sheet section describes the Hardware Interrupt register triplet, shared by all terminal modes.

Each individual bit in all three Hardware Interrupt registers is mapped to the same interrupt-causing event when the corresponding interrupt condition is enabled. Numerous hardware interrupt options are available. At initialization, bits must be set in the Hardware Interrupt Enable register to identify which interrupt-causing events are heeded by the HI-613x. Some hardware interrupts (identified later) are automatically enabled after $\overline{MR}$ master reset. When applications use just a subset of available interrupt options, selected hardware interrupts are ignored when their corresponding bits are reset in the Hardware Interrupt Enable Register. Setting an Interrupt Enable register bit from 0 to 1 does not trigger interrupt recognition for events that occurred while the bit was zero.

Whenever an enabled hardware interrupt event occurs, the Interrupt Log Buffer is updated and a bit is set in the Hardware Pending Interrupt Register. This action takes place only when the corresponding bit is already set in the Hardware Interrupt Enable Register when the interrupt event occurs. The host can poll Pending Interrupt Registers to detect interrupt occurrence, indicated by non-zero value. When the host reads a pending interrupt register, it automatically clears to 0x0000.

When an enabled hardware interrupt event occurs and the corresponding bit is also set in the Hardware Interrupt Output Enable Register, the $\overline{IRQ}$ output pin is asserted. Thus, the Hardware Interrupt Output Enable Register establishes two interrupt priority levels: high priority hardware interrupts generate an $\overline{IRQ}$ signal output, while low priority hardware interrupts do not. The host identifies low priority hardware interrupts by polling the Hardware Pending Interrupt Register.

A single $\overline{IRQ}$ host interrupt output signal is shared by all enabled interrupt conditions having bits set in the respective Interrupt Output Enable registers. Since one MIL-STD-1553 message can contain multiple interrupt-causing events, each $\overline{IRQ}$ output assertion can result from a single interrupt condition or a combination of interrupt conditions.

When the host receives an $\overline{IRQ}$ signal from the device, it must identify the event (or events) that triggered the interrupt. A hardware-assisted interrupt-decoding scheme simplifies interrupt identification. This scheme uses the three low order bits in the Hardware Pending Interrupt Register.

Upon $\overline{IRQ}$ interrupt assertion, the host should first read the Hardware Pending Interrupt Register. Bits 15-3 in this register identify hardware interrupt conditions. The three low-order bits the Hardware Pending Interrupt Register indicate zero vs. non-zero status for the RT, MT and BC Pending Interrupt Registers. If any of these bits is logic 1, the corresponding Pending Interrupt Register has one or more interrupt flags set. Any combination of these 3 bits may be set. Each of the four Pending Interrupt registers self-resets to 0x0000 after the host reads its value. Thus, the host should retain the value read from the Hardware Pending Interrupt Register when 2 or more bits are non-zero in the bit 2-0 range.

When polling the Pending Interrupt registers to identify low priority interrupts that do not assert the $\overline{IRQ}$ output, the same method can be applied. At a single read of the Hardware Pending Interrupt Register reveals zero / non-zero status of all four Pending Interrupt registers.

To help the host process interrupts, the HI-613x device maintains information from the 32 most recent interrupts in a 64-word ring buffer in RAM, located at the fixed address range 0x0180 to 0x01BF. Each interrupt stores two information words: the Interrupt Identification Word (IIW) identifies the interrupt type(s) that occurred; the Interrupt Address Word (IAW) identifies the interrupt source. For interrupts that result from message processing, the IAW contains the 16-bit address of the command's Control Word in the Descriptor Table. For hardware interrupts, the IAW value is 0x0000.

The 13th interrupt management register is the Interrupt Count & Log Address Register.

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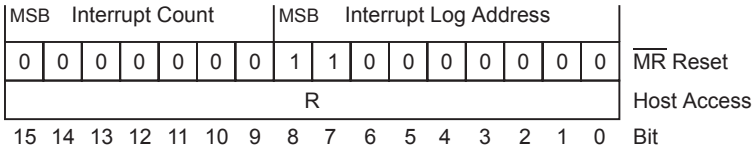
9.4. Interrupt Count & Log Address Register (0x000A)



This 16-bit register is read-only and is fully maintained by HI-613x logic. The register contains 0x0180 after $\overline{MR}$ pin master reset. It is not affected by assertion of MTRESET, RT1RESET or RT2RESET bits in the Master Status and Reset Register (0x0001). Bits 8:0 contain a 9-bit address pointer to the 64-word Interrupt Log Buffer located in RAM. The value in Interrupt Log Address register bits 8:0 indicates the storage address where interrupt information words will be stored for the next occurring interrupt, 0x0180 - 0x019E. The value is always even since two words are stored for each interrupt. The three highest address bits (register bits 8:6) are always 1-1-0.

Bits 15:9 contain a 7-bit count value for the number of interrupts logged (0 - 127) since the Interrupt Count & Log Address Register was last read. The count increment stops at 127. Counting continues above 32 so the host can detect when buffer overrun has occurred. Bits 15:9 are reset automatically when the host reads this register.

After $\overline{MR}$ master reset, the HI-613x initializes this register to 0x0180, an interrupt count of zero and log address of 0x180. During terminal operation, the host can read bits 15:9 to see the number of interrupts logged in the buffer since the last read operation upon the register. Information words for the 32nd interrupt are stored in buffer addresses 0x01BE and 0x01BF, and the Interrupt Log Address “rolls over” to read 0x0180, where interrupt information for the 33rd interrupt will be stored.

In the respective terminal device sections, definitions are provided for the interrupt management register triplets used for BC (bus controller), MT (bus monitor terminal) and RT (remote terminal) interrupts.

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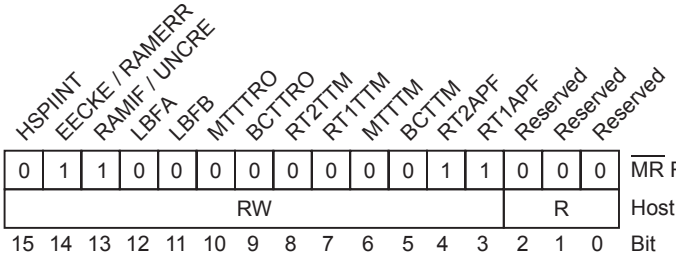
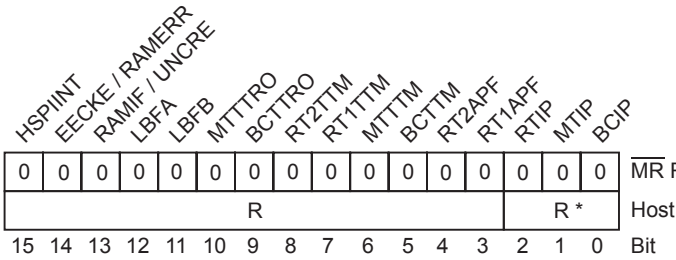
9.5. Hardware Interrupt Registers

9.5.1. Hardware Interrupt Enable Register (0x000F)



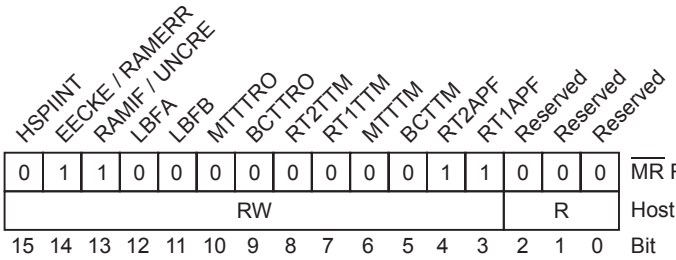
* *Bits 2 - 0 are read-only and cannot be set by host.*

9.5.2. Hardware Pending Interrupt Register (0x0006)



* *Bits 2 - 0 are set for pending interrupts from RT (RT1 or RT2), MT or BC*

9.5.3. Hardware Interrupt Output Enable Register (0x0013)



* *Bits 2 - 0 are read-only and cannot be set by host.*

These three registers govern hardware interrupt behavior. As explained on the preceding page, bits 2-0 in the Hardware Pending Interrupt Register are set whenever interrupt bits are set in the other three pending interrupt registers (RT, MT and BC). The table below first describes the common bits 15-3 in all three registers and then describes register-to-register differences for bits 2-0.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	HSPIINT	R/W	0	Host SPI Interrupt. This bit only applies to HI-6131 with SPI host interface, which operates in SPI Slave mode. An unexpected number of SCK clock pulses occured during a SPI transaction.

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Bit No.	Mnemonic	R/W	Reset	Function
14	EECKE	R/W	1	EEPROM Checksum Error Interrupt. This function only applies when the RAMEDC input pin is logic 0 and the AUTOEN input pin is logic 1 at rising edge of $\overline{MR}$ Master Reset. This enables auto-initialization from serial EEPROM, as well as RT or MT soft reset with auto-initialization. This bit is logic 1 in the Hardware Interrupt Enable Register and in the Hardware Interrupt Output Enable Register after $\overline{MR}$ master reset. The EECKE bit is set in the Hardware Pending Interrupt Register (as well as bit 1 in the Master Status and Reset Register, 0x0001) when a serial EEPROM checksum failure occurs during auto initialization, or execution of a partial reset caused by assertion of the RT1RESET, RT2RESET or MTRESET bits in the Master Status and Reset Register, 0x0001. Register bit 14 has a secondary function when input pin RAMEDC is connected to logic 1. When the RAMEDC pin is high, the available RAM address space is reduced from 32K words to 24K words, but error detection and correction (EDC) is performed after every RAM address read cycle.
	RAMERR			Detected and Corrected 24K RAM Error. This function only applies when the device RAMEDC input pin is connected high, configuring the device for 24K RAM with EDC enabled. Single-bit errors are automatically corrected by the device, but multiple-bit errors are not correctable. When a single-bit RAM data error is detected and corrected, register bit 14 is set to logic 1. The EECKE bit 1 in register 0x0001 is also cleared. When bit 14 is asserted in the Hardware Pending Interrupt Register 0x0009, the host can distinguish an EECKE interrupt from a RAMERR interrupt by reading the Master Status and Reset Register 0x0001. EECKE bit 1 in that register will be logic 1 for EECKE interrupt, logic 0 for CRAMERR interrupt.

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Bit No.	Mnemonic	R/W	Reset	Function
13	RAMIF	R/W	1	RAM Initialization Fail Interrupt. This function only applies when the RAMEDC input pin is logic 0 and the AUTOEN input pin is logic 1 at rising edge of $\overline{MR}$ Master Reset. This enables auto-initialization from serial EEPROM, as well as RT or MT soft reset with auto-initialization. This bit is logic 1 in the Hardware Interrupt Enable Register and in the Hardware Interrupt Output Enable Register after $\overline{MR}$ master reset. The RAMIF bit is set in the Hardware Pending Interrupt Register (as well as bit 0 in the Master Status and Reset Register, 0x0001) when one or more initialized RAM locations do not match their two corresponding serial EEPROM byte locations. Such failure occurs during auto initialization, or execution of a partial reset caused by assertion of the RT1RESET, RT2RESET or MTRESET bits in the Master Status and Reset Register, 0x0001. Register bit 14 has a secondary function when input pin RAMEDC is connected to logic 1. When the RAMEDC pin is high, the available RAM address space is reduced from 32K words to 24K words, but error detection and correction (EDC) is performed after every RAM address read cycle.
	UNCRE			Uncorrected 24K RAM Error. This function only applies when the device RAMEDC input pin is connected high, configuring the device for 24K RAM with EDC enabled. The device automatically corrects single-bit errors, but multiple-bit errors are not correctable. When an uncorrectable RAM data error is detected, register bit 13 is set to logic 1. The RAMIF bit 1 in register 0x0001 is also cleared. When bit 13 is asserted in the Hardware Pending Interrupt Register 0x0009, the host can distinguish a RAMIF interrupt from a UNCRE interrupt by reading the Master Status and Reset Register 0x0001. RAMIF bit 1 in that register will be logic 1 for RAMIF interrupt, logic 0 for UNCRE interrupt.
12 11	LBFA LBFB	R/W	0	Loopback Fail Bus A Interrupt (LBFA) Loopback Fail Bus B Interrupt (LBFB) For all transmitted words, the device checks MIL-STD-1553 word validity for the subsequently received/decoded word detected on the bus. This includes sync, encoding, bit count and parity checking. The last word in each message transmitted by the device is also checked for data matching. The LBFA bit is set each time loop-back detects an invalid or mismatched word on Bus A. The LBFB bit is set each time loop-back detects an invalid or mismatched word on Bus B.
10	MTTTRO	R/W	0	MT Time Tag Counter Rollover. The Bus Monitor time tag counter rolled over from full count to zero. Depending on options selected in the Time Tag Configuration Register, the MT time count may be either 16 or 48 bits.

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Bit No.	Mnemonic	R/W	Reset	Function
9	BCTTRO	R/W	0	BC Time Tag Counter Rollover. The Bus Controller time tag counter rolled over from full count to zero. Depending on options selected in the Time Tag Configuration Register, the BC time count may be either 16 or 32 bits.
8	RT2TTM	R/W	0	RT2 Time Tag Match. The 16-bit Remote Terminal 2 time tag counter incremented to a count matching the contained value in the RT2 Time Tag Reload / Match Register.
7	RT1TTM	R/W	0	RT1 Time Tag Match. The 16-bit Remote Terminal 1 time tag counter incremented to a count matching the contained value in the RT1 Time Tag Reload / Match Register.
6	MTTTM	R/W	0	MT Time Tag Match. The Bus Monitor time tag counter incremented to a count matching the contained value in the MT Time Tag Match Registers.
5	BCTTM	R/W	0	BC Time Tag Match. The Bus Controller time tag counter incremented to a count matching the contained value in the BC Time Tag Match Register(s).
4	RT2APF	R/W	1	RT2 Terminal Address Parity Fail Interrupt. The Remote Terminal address and parity bits (latched into the RT2 Operational Status Register at rising edge of $\overline{MR}$) do not exhibit odd parity (do not have an odd number of bits having logic 1 state). Note: RT2 address parity is only checked if the RT2ENA pin is logic 1 at rising edge of $\overline{MR}$.
3	RT1APF	R/W	1	RT1 Terminal Address Parity Fail Interrupt. The Remote Terminal address and parity bits (latched into the RT1 Operational Status Register at rising edge of $\overline{MR}$) do not exhibit odd parity (do not have an odd number of bits having logic 1 state). Note: RT1 address parity is only checked if the RT1ENA pin is logic 1 at rising edge of $\overline{MR}$.
For the Hardware Interrupt Enable Register and the Hardware Interrupt Output Enable Register only				
2 − 0	Reserved			Bits 2-0 cannot be written and read back 000.
For the Hardware Pending Interrupt Register only				
2	RTIP	R	0	RT Interrupt Pending. When this bit is high, one or more bits are set in the RT Pending Interrupt Register. The host can read that register (0x0009) to determine the RT1 or RT2 interrupt event(s).
1	MTIP	R	0	MT Interrupt Pending. When this bit is high, one or more bits are set in the MT Pending Interrupt Register. The host can read that register (0x0008) to determine the MT interrupt event(s).

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Bit No.	Mnemonic	R/W	Reset	Function
0	BCIP	R	0	BC Interrupt Pending. When this bit is high, one or more bits are set in the BC Pending Interrupt Register. The host can read that register (0x0007) to determine the BC interrupt event(s).

9.6. Time Tag Counter Configuration

Each device (RT1, RT2, BC or MT) has an independent time tag counter used for time-stamping messages. The two remote terminals RT1 and RT2 have independent 16-bit time tag counters because each RT needs independent count reset and “synchronization” loading. In the Time Tag Counter Configuration Register, bits 2-0 select the clock source for both of the RT1 and RT2 time tag counters. The same clock source is shared by the Bus Controller. The host controls the free-running RT1 and RT2 time tag counters using bit pairs 11-10 (RT2) or 9-8 (RT1) in the Time Tag Counter Configuration Register. Here is a summary of host-initiated operations involving the RT time tag counters:

a. Clearing the 16-bit RT1 or RT2 time tag count to 0x0000.

b. Copying the RT1 or RT2 TT16 Time Tag Utility Register value into the 16-bit RT1 or RT2 time tag counter.

c. Copying the current 16-bit RT1 or RT2 time tag count value into the RT1 or RT2 TT16 Time Tag Utility Register.

The bus controller (BC) can operate using either a 16- or 32-bit time tag counter, selected using register bit 3, BCTT32, in the Time Tag Counter Configuration Register. The BC time tag counter clock source is selected using register bits 2-0. This common clock source is shared by the BC, RT1 and RT2. Bit pair 13-12 is used for clearing BC time tag counter, loading the counter with a 16- or 32-bit value contained in the BC Time Tag Reload Register, or writing the current 16- or 32-bit BC time tag counter value to the BCMT Time Tag Utility Register set (shared by the BC and MT.)

The free-running BC time tag counter can be reset to zero, loaded with an arbitrary value, or the current count can be captured. In 32-bit time tag mode, the full count is captured by simultaneously loading two utility registers. Writing bits 13-12 in the Time Tag Counter Configuration Register initiates these operations. Here is a summary of host-initiated operations involving the BC time tag counter:

a. Clearing a 16- or 32-bit BC time tag count, whichever is enabled.

b. When 16-bit BC time tag count is enabled,

- loading the 16-bit BC time tag counter with the 16-bit value contained in the BC TT16 Time Tag Utility Register
- capturing the current 16-bit BC time tag counter value to the BC TT16 Time Tag Utility Register

c. When 32-bit BC time tag count is enabled,

- loading the 32-bit BC time tag counter with the 32-bit value contained in the BC TT32 Time Tag Utility Register pair
- capturing the current 32-bit BC time tag counter value to the BC TT32 Time Tag Utility Register pair

The bus monitor (MT) can operate using either a 16- or 48-bit time tag counter, selected using MT Configuration Register bits 1-0. When using 16-bit resolution, one register is adequate for holding time tag values. When using 48-bit time tag count resolution, three 16-bit registers are needed for each stored time tag count. The MT time tag counter clock source is selected using bits 7-5 in the Time Tag Counter Configuration Register, 0x0039. The MT time tag clock source is separate from the source shared by the BC, RT1 and RT2.

The free-running MT time tag counter can be reset to zero, loaded with an arbitrary value, or the current count can be captured. In 48-bit time tag mode, the full count is captured by simultaneously loading three utility registers. Writing bits 15-14 in the Time Tag Counter Configuration Register 0x0039 initiates these operations.

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Here is a summary of host-initiated operations involving the MT time tag counter:

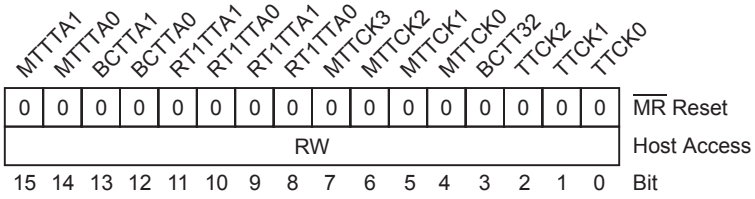
a. Clearing a 16- or 48-bit MT time tag count, whichever is enabled.

b. When 16-bit MT time tag count is enabled,
   - loading the 16-bit MT time tag counter with the 16-bit value contained in the MT TT16 Time Tag Utility Register
   - capturing the current 16-bit MT time tag counter value to the MT TT16 Time Tag Utility Register

c. When 48-bit MT time tag count is enabled,
   - loading the 48-bit MT time tag counter with the 48-bit value contained in the MT TT48 Time Tag Utility Register triplet
   - capturing the current 48-bit MT time tag counter value to the MT TT48 Time Tag Utility Register triplet when 48-bit MT time tag count is enabled

Host interrupts can be generated when any of the four time tag counters in the device reach preset values contained in Time Tag Match registers. Refer to the Interrupt Management section of the data sheet.

9.7. Time Tag Counter Configuration Register (0x0039)



This 16-bit read-write register is cleared after $\overline{MR}$ pin master reset, but is unaffected by assertion of MTRESET, RT1RESET or RT2RESET register bits.

When written, register bits 15-8 work in pairs to initiate a particular action, such as clearing or loading one of these counters. When written, register bits 15-8 self reset to zero after initiating the assigned action. Thus, bits 15-8 always read logic 0. Register bits 7-0 are used for configuring the various time tag counters in the HI-613x device. These bits will read back the last value written by the host.

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>15
14</td><td>MTTTA1
MTTTA0</td><td>R/W</td><td>0</td><td>
MT Time Tag Action Bits 1-0.
After performing the action below, these host-written bits self reset to 00:
<table>
<tr><th>Bits 15-14</th><th>Action</th></tr>
<tr><td>00</td><td>Do Nothing.</td></tr>
<tr><td>01</td><td>Reset 16- or 48-bit MT Time Tag count to zero.</td></tr>
<tr><td>10</td><td>Load the 16- or 48-bit value from BCMT Time Tag Utility Register(s) into the MT Time Tag Count register(s).</td></tr>
<tr><td>11</td><td>Capture current 16- or 48-bit value in the MT Time Tag Count Register(s) into the BCMT Time Tag Utility Register(s).</td></tr>
</table>
If the MT is using 16-bit time tag, the MT Time Tag Counter uses a single register address, 0x003A. The BCMT Time Tag Utility Register used for the load and capture operations is register address 0x003D.
If the MT is using 48-bit time tag, the MT Time Tag Counter uses three register addresses. The High-Mid-Low words are found at 0x003C, 0x003B and 0x003A. The triplet of BCMT Time Tag Utility Registers used for the load and capture operations is located at register addresses 0x003F (High), 0x003E (Mid) and 0x003D (Low).
</td></tr>
</table>

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>15
14</td><td>MTTTA1
MTTTA0
(continued)</td><td>R/W</td><td>0</td><td>
Bits 1-0 in the MT Configuration Register, 0x0029 select IRIG-106 monitor, IMT (always 48-bit time tag counting), or simple monitor, SMT, (choice of 16-bit or 48-bit time tag counting):
<table>
<tr><th>MT Configuration Register, bits 1-0</th><th>MT Operation</th><th>Time Tag Mode</th></tr>
<tr><td>00 or 10</td><td>IMT (IRIG-106 mode, 1 stack)</td><td>48-bit time tag</td></tr>
<tr><td>01</td><td>SMT mode, Command & Data Stacks</td><td>16-bit time tag</td></tr>
<tr><td>11</td><td>SMT mode, Command & Data Stacks</td><td>48-bit time tag</td></tr>
</table>
When the MT is operating in Simple mode with 48-bit time tag, the recorded Command Stack entry for each 1553 message has eight 16-bit words. When operating with 16-bit time tag, the recorded Command Stack entry for each 1553 message has four 16-bit words.
</td></tr>
</table>

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td rowspan="6">13
12</td><td rowspan="6">BCTTA1
BCTTA0</td><td rowspan="6">R/W</td><td rowspan="6">0</td><td colspan="2">BC Time Tag Action Bits 1-0.
After performing the action below, these host-written bits self reset to 00:</td></tr>
<tr><td>Bits 13-12</td><td>Action</td></tr>
<tr><td>00 or 11</td><td>Do Nothing.</td></tr>
<tr><td>01</td><td>Reset 16- or 32-bit BC Time Tag count to zero.</td></tr>
<tr><td>10</td><td>Load the 16- or 32-bit value from BCMT Time Tag Utility Register(s) into the BC Time Tag Count register(s).</td></tr>
<tr><td colspan="2">If BCTT32 register bit 3 equals 0, the BC is using 16-bit time tag. The BC Time Tag Counter uses a single register address, 0x0043. The BCMT Time Tag Utility Register used for these operations is register address 0x003D.
If BCTT32 register bit 3 equals 1 the BC is using 32-bit time tagging, so the BC Time Tag Counter requires two 16-bit register addresses. The High and Low BC time tag counter words are found at 0x0044 and 0x0043. The pair of BCMT Time Tag Utility Registers used for timer operations is located at register addresses 0x003E (High word) and 0x003D (Low word).</td></tr>
<tr><td rowspan="6">11
10</td><td rowspan="6">RT2TTA1
RT2TTA0</td><td rowspan="6">R/W</td><td rowspan="6">0</td><td colspan="2">RT2 Time Tag Action Bits 1-0.
After performing the RT2 time tag counter action below, these host-written bits self reset to 00:</td></tr>
<tr><td>Bits 11-10</td><td>Action</td></tr>
<tr><td>00 or 11</td><td>Do Nothing.</td></tr>
<tr><td>01</td><td>Reset 16-bit RT2 Time Tag count to zero.</td></tr>
<tr><td>10</td><td>Load the 16-bit value from the RT2 Time Tag Utility Register(s) into the RT2 Time Tag Counter.</td></tr>
<tr><td rowspan="6">9
8</td><td rowspan="6">RT1TTA1
RT1TTA0</td><td rowspan="6">R/W</td><td rowspan="6">0</td><td colspan="2">RT1 Time Tag Action Bits 1-0.
After performing the RT1 time tag counter action below, these host-written bits self reset to 00:</td></tr>
<tr><td>Bits 9-8</td><td>Action</td></tr>
<tr><td>00 or 11</td><td>Do Nothing.</td></tr>
<tr><td>01</td><td>Reset 16-bit RT1 Time Tag count to zero.</td></tr>
<tr><td>10</td><td>Load the 16-bit value from the RT1 Time Tag Utility Register(s) into the RT1 Time Tag Counter.</td></tr>
</table>

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td rowspan="3">7
6
5
4</td><td rowspan="3">MTTCK3
MTTCK2
MTTCK1
MTTCK0</td><td rowspan="3">R/W</td><td rowspan="3">0</td><td>MT Time Tag Clock Selection Bits 3-0.
These three bits select the clock source for the BC, RT1 and RT2 Time Tag Counters from the following options:</td></tr>
<tr><td>Bits 3-2-1-0</td><td>MT Time Tag Counter Clock Source</td></tr>
<tr><td>0-0-0-0
0-0-0-1
0-0-1-0
0-0-1-1
0-1-0-0
0-1-0-1
0-1-1-0
0-1-1-1
1-x-x-x</td><td>Time Tag Counter Disabled.
External clock provided at the MTTCLK input pin.
Internally generated 2µs clock.
Internally generated 4µs clock.
Internally generated 8µs clock.
Internally generated 16µs clock.
Internally generated 32µs clock.
Internally generated 64µs clock.
Internally generated 100µs clock.</td></tr>
<tr><td>3</td><td>BCTT32</td><td>R/W</td><td>0</td><td>BC Time Tag 32-Bit Count Enable.
When the BCTT32 bit equals 0, the BC time tag counter is 16 bits.
When the BCTT32 bit equals 1, the BC time tag counter is 32 bits.</td></tr>
<tr><td rowspan="3">2
1
0</td><td rowspan="3">TTCK2
TTCK1
TTCK0</td><td rowspan="3">R/W</td><td rowspan="3">0</td><td>BC and RT Time Tag Clock Selection Bits 2-0.
These three bits select the clock source for the BC, RT1 and RT2 Time Tag Counters from the following options:</td></tr>
<tr><td>Bits 2-1-0</td><td>Time Tag Counter Clock Source</td></tr>
<tr><td>0-0-0
0-0-1
0-1-0
0-1-1
1-0-0
1-0-1
1-1-0
1-1-1</td><td>Time Tag Counter Disabled.
External clock provided at TTCLK input pin.
Internally generated 2µs clock.
Internally generated 4µs clock.
Internally generated 8µs clock.
Internally generated 16µs clock.
Internally generated 32µs clock.
Internally generated 64µs clock.</td></tr>
</table>

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9.8. Memory Address Pointer Registers (HI-6131 only)

This section only applies for the HI-6131 with SPI host interface. It does not apply to the HI-6130 with parallel bus interface.

The HI-6131 SPI uses predefined 8-bit instruction op codes to perform a variety of predetermined actions. Some op codes must be followed by two or more operand bytes, while other SPI codes perform their desired action without additional operands. Examples of self-contained SPI op codes include the “Fast access” op codes used for reading or writing registers at the low end of the address space.

“Fast access” op codes used for direct addressing contain embedded register addresses, but only work over a limited address range.

- SPI reads to register addresses 0 through 0x000F (decimal 15) use an 8-bit op code of the form **0x00 + (Reg_Addr << 2)** where Reg_Addr = 0 to 0xF before left-shifting two bits.
- SPI writes to register addresses 0 through 0x003F (decimal 63) use an 8-bit op code of the form **0x80 + Reg_Addr** where Reg_Addr equals 0 to 0x3F.

The two “fast access” op codes use a dedicated memory address pointer to perform their duties without affecting values contained in other Memory Address Pointer registers. The “fast access” Memory Address Pointer cannot be read by the host, but is written each time a “fast access” op code is processed.

The HI-6131 uses a Memory Address Pointer for SPI reads to register addresses over 0x000F, or for SPI writes to register addresses over 0x003F. For most SPI read and write operations, the starting memory address for the requested operation is written to the Memory Address Pointer (or MAP) before the op code (using the MAP) is invoked.

In the case of a multiword data transfer involving a range of sequential addresses, the memory address pointer is initialized with the starting (lowest) address. After the SPI transfers data from the first address, the memory address pointer automatically increments to the next address. When read access occurs, the device prefetches the data stored at the next address to support the fastest possible data rates. As long as the chip select stays low (asserted) and the SPI master continues to provide serial clocks, data read/write transfers for sequential addresses continue until the chip select is negated. Please refer to the later section describing SPI host access and the SPI op codes used for data transfer.

For flexibility in configuring the HI-6131device, four independent Memory Address Pointers are available. These can be assigned in any manner that supports application requirements. For example:

- To simplify data access while supporting concurrent terminal devices (BC, MT, RT1 and RT2), some devices may need a dedicated Memory Address Pointer (MAP) while other devices may be able to share a MAP.
- Consider using a dedicated Memory Address Pointer for interrupt service routines. Many SPI operations are multiword transfers that utilize the Memory Address Pointer auto-increment feature. If interrupts are enabled during multiword transfers, a dedicated Memory Address Pointer for the interrupt service routine avoids corruption of the MAP used by the interrupted routine.

Residing in the lower register address space, the four Memory Address Pointers can be read or written with a single 8-bit “fast access” op code (plus the desired 16-bit data value, when writing).

Just one of the four MAP registers is enabled at any time. Each of the four Memory Address Pointers has a dedicated 8-bit “MAP Select” op code that enables it by writing the Master Configuration Register. Or the host can directly write the MAPSEL (Memory Address Pointer select) bits 11-10 in the Master Configuration Register to enable the desired MAP register. Full descriptions of SPI data transfer methods are provided later in this document.

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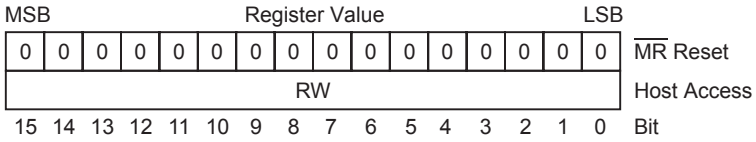
The four memory address pointer registers are:

MAP1 Memory Address Pointer Register 0x000B

MAP2 Memory Address Pointer Register 0x000C

MAP3 Memory Address Pointer Register 0x000D

MAP4 Memory Address Pointer Register 0x000E



These 16-bit registers are read-write and are fully maintained by the host. These registers are cleared after $\overline{MR}$ pin master reset, but are unaffected by assertion of RT1RESET, RT2RESET or MTRESET bits in the Master Status and Reset Register (0x0001).

Each of these registers has a unique SPI op code that reads the MAP value in the register, and another op code that writes a new MAP value into the register. See SPI op code table. The host selects the active MAP register by writing the MAPSEL (memory address pointer select) bits 11-10 in the Master Configuration Register (see Section 9.1), or by using the four defined “MAP Select” SPI op codes, described in Section XX. The active MAP register contains the memory address used for SPI read write access to registers and RAM.

Please refer to section “SPI Interface” for a full description of the interface and the SPI instruction op codes.

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10. BUS CONTROLLER − CONFIGURATION AND OPERATION

The HI-613x can operate as an autonomous MIL-STD-1553 Bus Controller (BC), requiring minimal host processor support. All MIL-STD-1553B error-checking is automatically performed, including RT response time, Manchester II encoding, sync type, bit count, word parity, word count, responding RT address, and detection of the full range of possible error conditions encountered during BC operation. The device implements all MIL-STD-1553B message formats. Message format is configurable on a message by message basis. Each message is individually programmable for command type. Individual messages can be programmed for automatic retries on either bus, and interrupt requests may be enabled or disabled.

The HI-613x Bus Controller provides a flexible means for scheduling major and minor frames, allowing insertion of asynchronous messages during frame execution. Upon error, individual messages can be programmed for one or two automatic retries, and the BC can switch buses before retry occurs. Message data is separated from control and status data, to serve the needs for double buffering in RAM and bulk data transfers.

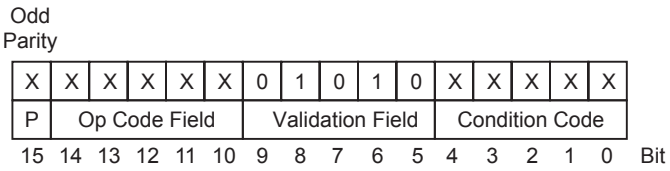
Before Bus Controller operation can begin, the BCENA input pin must be connected to logic 1 to allow BC operation. All Bus Controller operational registers (see Section 11) must be properly configured. The BC Instruction List in RAM must be initialized to define message sequencing and conditional execution, and finally the host must assert BCSTRT bit 13 in the Master Configuration Register 0x0000 to initiate execution of Instruction List op codes. The following pages provide the necessary details for successful Bus Controller operation.

Figure 3 shows the registers and RAM resources utilized by the Bus Controller. All Bus Controller registers are fully described in Section 11.

Initial control of BC message sequencing involves the BC Instruction List Pointer in register 0x0034. Before BC execution begins, the instruction list starting address is copied from the BC Instruction List Start Address Register, 0x0033. Once message sequencing is underway, the BC Instruction List Pointer in register 0x0034 is updated by the BC control logic.

The BC Instruction List in RAM comprises a series of 2-word entries, an instruction op code followed by a parameter word. While processing messages, the BC control logic fetches and executes the instruction op code referenced by the BC Instruction List Pointer from the BC Instruction List. The pointer parameter, referencing the first word in the Message Control/Status Block, must have the form 0xHHH8 or 0xHHH0, where each H represents a hex character, 0-9 or A-F. If the individual message is RT-to-RT, the address must have the form 0xHHH0.

Each op code word in the BC Instruction List has the format:



Bus Controller execution stops immediately if the BC logic fetches an op code word having one or more of these error conditions:

- Bit 15 contains even parity
- Bits 14-10 contain an undefined op code
- Validation field bits 9-5 do not equal 01010

If enabled in the BC Interrupt Enable Register 0x0010, a BCTRAP interrupt occurs when execution stops because of an illegal op code.

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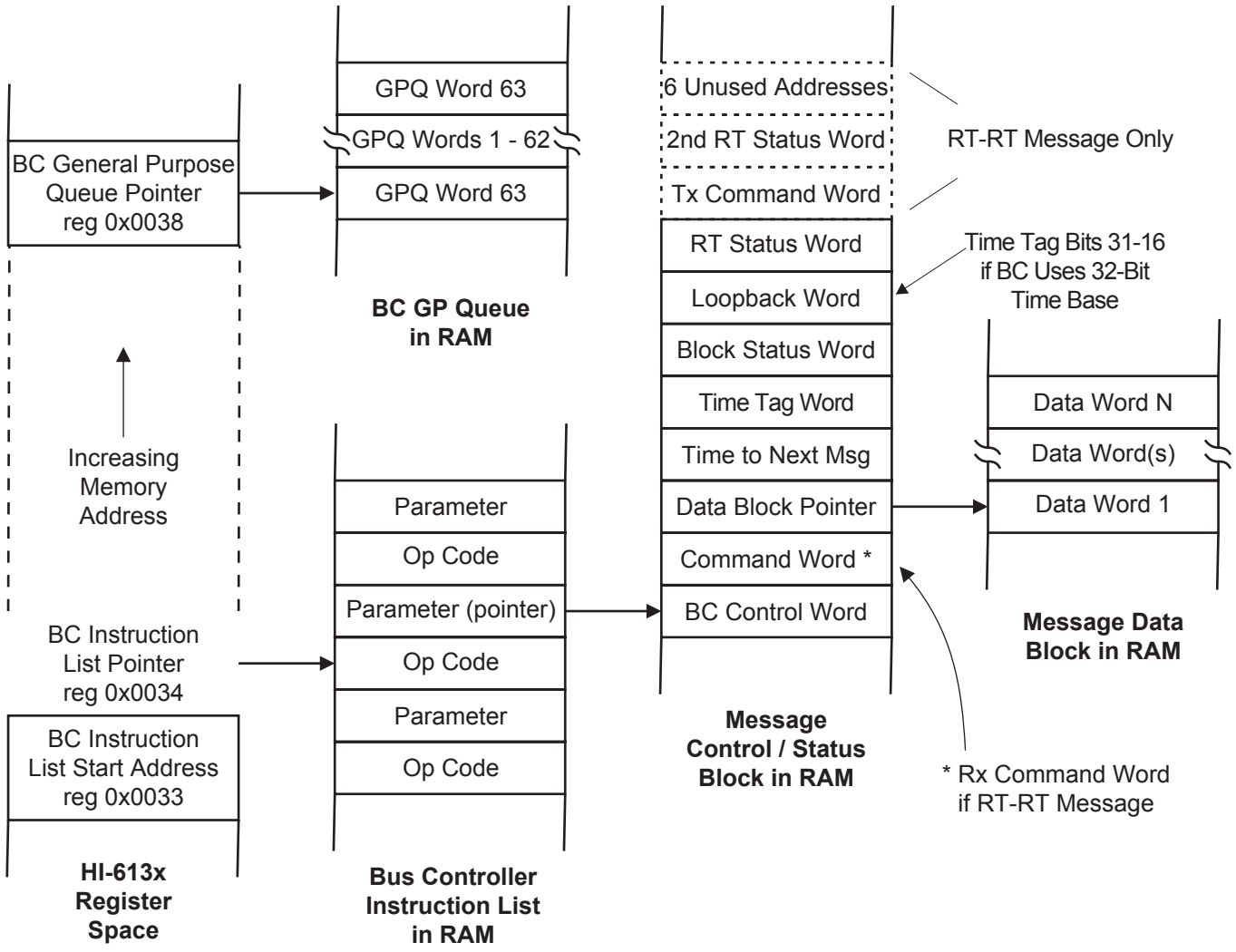

Figure 3. Bus Controller Message Sequence Structures

10.1. Bus Controller Condition Codes

For most op codes, execution is conditional, depending on evaluation of the Condition Code field. Condition Code bits 3-0 define the specific condition. Condition Code bit 4 identifies the required outcome for op code execution, true or false (1 or 0), following evaluation of Condition Code bits 3-0. The host has read-only access to the BC condition codes by reading the BC Condition Code Register 0x0037.

Eight of the condition codes (1000 through 1111) are set or cleared based on the outcome of the most recent message. The remaining eight codes are General Purpose Condition Codes, GP0 through GP7. Three processes affect values of the General Purpose Condition Code bits: (a) they may be toggled, set or cleared when the BC logic executes a FLG (GP Flags Bits) op code. (b) they may be toggled, set or cleared when the host writes the BC General Purpose Flag Register 0x0037. (c) only GP0 and GP1 may be set or cleared when the BC logic executes a CMT (Compare Message Timer) op code, or a CFT (Compare Frame Timer) op code. The sixteen BC Condition Codes are summarized in Table 5.

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Table 5. Bus Controller Condition Code Table

Code Bit 3-0	Condition Code *Negation Bit 4 = 0*	Condition Code *Negation Bit 4 = 0*	Function
0000	LT / GP0	GT-EQ / $\overline{GP0}$	Less Than or GP0 Flag. This flag may be toggled, set or cleared when the BC logic executes a FLG (General Purpose Flags Bits) op code, or when the host writes the BC General Purpose Flag Register 0x0037. This flag is also set or cleared based on the evaluation of a CMT (Compare Message Timer) or CFT (Compare Frame Timer) instruction op code:
	LT / GP0 = 1	GT-EQ / $\overline{GP0}$ = 0	If CMT parameter < BC Time to Next Message Reg If CFT parameter < BC Frame Time Remaining Reg
	LT / GP0 = 0	GT-EQ / $\overline{GP0}$ = 1	If CMT parameter = BC Time to Next Message Reg If CFT parameter = BC Frame Time Remaining Reg
	LT / GP0 = 0	GT-EQ / $\overline{GP0}$ = 1	If CMT parameter > BC Time to Next Message Reg If CFT parameter > BC Frame Time Remaining Reg
	LT / GP0 = 1 or 0 based on compared values	GT-EQ / $\overline{GP0}$ = 0 or 1 based on compared values	If CMT parameter ≠ BC Time to Next Message Reg If CFT parameter ≠ BC Frame Time Remaining Reg
0001	EQ / GP1	NE / $\overline{GP1}$	Equal To or GP1 Flag. This flag may be toggled, set or cleared when the BC logic executes a FLG (General Purpose Flags Bits) op code, or when the host writes the BC General Purpose Flag Register 0x0037. This flag is also set or cleared based on the evaluation of a CMT (Compare Message Timer) or CFT (Compare Frame Timer) instruction op code:
	EQ / GP1 = 0	NE / $\overline{GP1}$ = 1	If CMT parameter < BC Time to Next Message Reg If CFT parameter < BC Frame Time Remaining Reg
	EQ / GP1 = 1	NE / $\overline{GP1}$ = 0	If CMT parameter = BC Time to Next Message Reg If CFT parameter = BC Frame Time Remaining Reg
	EQ / GP1 = 0	NE / $\overline{GP1}$ = 1	If CMT parameter > BC Time to Next Message Reg If CFT parameter > BC Frame Time Remaining Reg
	EQ / GP1 = 0	NE / $\overline{GP1}$ = 1	If CMT parameter ≠ BC Time to Next Message Reg If CFT parameter ≠ BC Frame Time Remaining Reg

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Code Bit 3-0	Condition Code *Negation Bit 4 = 0*	Condition Code *Negation Bit 4 = 0*	Function
0010	GP2	$\overline{\text{GP2}}$	General Purpose Flag Bits 2-7. These flags may be toggled, set or cleared when the BC logic executes a FLG (General Purpose Flags Bits) op code, or when the host writes the BC General Purpose Flag Register 0x0037.
0011	GP3	$\overline{\text{GP3}}$	
0100	GP4	$\overline{\text{GP4}}$	
0101	GP5	$\overline{\text{GP5}}$	
0110	GP6	$\overline{\text{GP6}}$	
0111	GP7	$\overline{\text{GP7}}$	
1000	NORESP	RESP	No Response Flag. This flag is set when an RT failed to respond to a command, or responded later than the BC No Response Timeout programmed using bits 15-14 in the BC Configuration Register 0x0032.
1001	FMTERR	$\overline{\text{FMTERR}}$	Format Error Flag. This flag is set when the received response to the last message had one or more violations to MIL-STD-1553B validation criteria, including problems with sync, encoding, bit count, parity, or word count. This flag is also set when the received RT Status Word response from the last message contained an incorrect RT address field.
1010	GOODBLOCK	$\overline{\text{GOODBLOCK}}$	Good Data Block Transfer. Reflecting status for the last 1553 message, this flag is set after completion of error-free RT-to-BC transfers, RT-to-RT transfers, or transmit mode code commands with data. This flag is reset after invalid messages, or after completion of BC-to-RT transfers, receive mode code commands with data, or mode code commands without data. This flag may be used to determine when the transmit aspect of an RT-to-RT transfer is error-free.
1011	MSKSTATSET	$\overline{\text{MSKSTATSET}}$	Masked Status Set. Reflecting status for the last 1553 message, this flag is set when one or both of the following conditions occurred: • In the message BC Control Word, at least one of the Status Mask bits 14-9 are logic 0, but the corresponding bit or bits are set in the received RT Status Word. When the Reserved Bits Mask (message BC Control Word bit 9) is logic 0, this flag is set when any or all of the three reserved bits are set in the received RT Status Word. • In the BC Configuration Register 0x0032, the BCR (broadcast command received) Mask Enable bit 0 is logic 1. the Mask Broadcast bit 5 in the message BC Control Word is logic 0, and the BCR (Broadcast Command Received) bit 4 is logic 1 in the received RT Status Word.

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Code Bit 3-0	Condition Code *Negation Bit 4 = 0*	Condition Code *Negation Bit 4 = 0*	Function
1100	BADMSG	GOODMSG	Bad Message. Reflecting status for the last 1553 message, the Bad Message flag is set for Format Error, No Response error, or loopback test failure. A Status Set condition has no effect on the Bad Message condition code.
1101	1RETRY	$\overline{\text{1RETRY}}$	1 Retry. If Condition Code bits 3:0 = 0xD and bit 4 = 0, one or two message retries is indicated. If Condition Code bits 3:0 = 0xD and bit 4 = 1, zero message retries is indicated.
1110	2RETRY	Undefined	2 Retries. If Condition Code bits 3:0 = 0xE and bit 4 = 0, two message retries is indicated. Condition Code bits 3:0 = 0xE and bit 4 = 1 is undefined.
1111	ALWAYS	NEVER	Always. The ALWAYS bit is set (Condition Code bit 4 = 0) to designate an instruction op code as unconditional. The NEVER bit is set (Condition Code bit 4 = 1) to designate an instruction op code as NOP (no op).

10.2. Bus Controller Instruction OP Codes

In the BC Instruction List, each op code word contains a 5-bit instruction field that spans bits 14-10. The instruction op codes are described in Table 6. Four instructions execute unconditionally, without evaluating the condition code test. For these instructions, the Condition Code field is “don’t care”.

The four unconditional instruction op codes are:

1. CMT (Compare Message Timer)
2. CFT (Compare Frame Timer)
3. FLG (General Purpose Flag Bits)
4. XQF (execute and Flip)

All other instruction op codes execute conditionally. They execute only if evaluation of the Condition Code tests true, logic 1. If the Condition Code field tests false, the BC Instruction List Pointer skips to the next instruction op code in the BC Instruction List.

Many instruction op codes utilize the following parameter word in the BC Instruction List. Depending on the op code, the parameter may be a RAM address, a time value, an interrupt bit pattern, an argument that sets or clears General Purpose Flag bits, or an immediate value. For some op codes, the parameter word is not used and is therefore “don’t care.” For an XEQ (execute message) instruction, the parameter is a RAM address pointer referencing the start of the message Control/Status Block.

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These instructions control program execution: Halt, Jump, Subroutine Call and Subroutine Return. Subroutine calls can be nested 8 levels deep. If BC Call Stack overflow or underflow occurs, device logic generates a CSTKERR (Call Stack Pointer Error) interrupt, if enabled. Other host interrupts are generated under program control using the Interrupt Request instruction. In this case, a 4-bit user-defined interrupt code is written to the BC Interrupt Request Bits 3-0 in the BC Pending Interrupt Register.

Other instructions are formed various duties: set, reset or toggle General Purpose Flag bits; load the Time Tag counter; load the Frame Time counter; begin a new BC frame; wait for external trigger, then start a new BC frame; evaluate remaining Frame Time; or evaluate time to next message.

Table 6. Bus Controller Instruction Op Codes

Name	*Instruction*	*Op Code*	*Parameter*	*Function*
XEQ	Execute Message *Conditional*	0x01	RAM Address for Message Control/ Status Block	If the Condition Code evaluates True, execute the message at the parameter-specified Message Control Status Block address. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List. At the start of XEQ message execution, if the fourth word in the Message Control/Status Block is nonzero, it is copied to the BC Time to Next Message Register, and message timer begins decrementing. The BC message sequencer does not fetch the next instruction op code until the message timer reaches zero. Regarding Condition Codes used with XEQ: • If using LT, GT-EQ, EQ and NE (which are only modified by the device upon completion of CMT or CFT op codes) the host must not change the value of the shared function GP0 or GP1 flag bit during execution of the contingent message. • If using GP Flag Bit status (GP0 through GP7) to enable a message, host must not alter the tested GP Flag bit during execution of a contingent message. • The ALWAYS and NEVER Condition Codes may be used with XEQ. The following Condition Codes must not be used with XEQ: BADMSG, RETRY1 or RETRY2, NORESP, MSKSTATSET, FMTERR or GOODBLOCK.

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Name	*Instruction*	*Op Code*	*Parameter*	*Function*
XQG	Execute Message and Go *Conditional*	0x16	RAM Address for Message Control/ Status Block	If the Condition Code evaluates True, execute the message at the parameter-specified Message Control Status Block address. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List. Regarding Condition Codes used with XQG: • If using LT, GT-EQ, EQ and NE (which are only modified by the device upon completion of CMT or CFT op codes) the host must not change the value of the shared function GP0 or GP1 flag bit during execution of the contingent message. • If using GP Flag Bit status (GP0 through GP7) to enable a message, host must not alter the tested GP Flag bit during execution of a contingent message. • The ALWAYS and NEVER Condition Codes may be used with XQG. The following Condition Codes must not be used with XQG: BADMSG, RETRY1 or RETRY2, NORESP, MSKSTATSET, FMTERR or GOODBLOCK. At the start of XQG message execution, if the fourth (Time to Next Message) word in the Message Control/Status Block is nonzero, it is copied to the BC Time to Next Message Register 0x0036, and this message timer begins countdown. Completion of an XQG message may occur while message timer countdown continues. Unlike XEQ, the XQG op code does not wait for the decrementing message timer to hit 0 before fetching the next instruction op code. As long as op codes following XQG do not execute a 1553 message, each op code is performed after fetch. Upon reaching a following XEQ, XQG, XQF or XFG execute-message instruction, transaction of its 1553 message does not begin until Time to Next Message count reaches 0. Thus, programmed 1553 message timing is maintained, while allowing execution of non-message instruction op codes.
JMP	Jump *Conditional*	0x02	RAM Address within the BC Instruction List	If the Condition Code evaluates True, jump to the parameter-specified instruction op code in the BC Instruction List. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.
CAL	Call Subroutine *Conditional*	0x03	RAM Address within the BC Instruction List	If the Condition Code evaluates True, push address of the next instruction op code onto the 8-level BC Call Stack, then jump to the parameter-specified instruction op code in the BC Instruction List. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.

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Name	*Instruction*	*Op Code*	*Parameter*	*Function*
RTN	Return from Subroutine *Conditional*	0x04	Not Used (Don't Care)	If the Condition Code evaluates True, pop the top address from the BC Call Stack, then jump to the popped instruction op code address in the BC Instruction List. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.
IRQ	Interrupt Request *Conditional*	0x06	4-Bit Interrupt Pattern, 0x000N	If the Condition Code evaluates True, generate a host interrupt by writing the parameter-specified 4-bit value N to bits 8-5 in the BC Pending Interrupt Register. Otherwise, continue execution at the next op code in the BC Instruction List. Note: no interrupt is generated if N = 0
HLT	Halt *Conditional*	0x07	Not Used (Don't Care)	If the Condition Code evaluates True, stop execution of the BC Instruction List until a new BC Start is issued by the host. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.
DLY	Delay *Conditional*	0x08	Delay Time Value (1 µs per LSB resolution)	If the Condition Code evaluates True, initiate a delay equal to the parameter-specified value. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List. If the Time-to-Next Message counter is in use, the DLY parameter has higher priority than the count for an unfinished Message Timer delay.
WFT	Wait until Frame Timer Equals 0 *Conditional*	0x09	Not Used (Don't Care)	If the Condition Code evaluates True, stop BC Instruction List execution until the BC Frame Time Counter decrements to 0. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.
CFT	Compare to Frame Timer *Conditional*	0x0A	Time Value (100 µs / LSB resolution)	Compare the parameter-specified Time Value to the BC Frame Time Remaining Register 0x0035. Set and clear LT and EQ bits 1 and 0 in the BC General Purpose Flag Register (Section 11.7).
CMT	Compare to Message Timer Unconditional	0x0B	Time Value (1 µs per LSB resolution)	Compare the parameter-specified Time Value to the BC Time to Next Message Register 0x0036. Set and clear LT and EQ bits 1 and 0 in the BC General Purpose Flag Register (Section 11.7). When CMT is preceded by an XEQ or XQF instruction, the BC Time to Next Message Register 0x0036 value used for comparison is always 0x0000 because the message timer (initiated by XEQ or XQF) decrements to zero before fetching the CMP instruction. In this case, a CMT with non-zero parameter word always sets GT-EQ and NE and always resets LT and EQ flags. When CMT is preceded by an XEQ or XQF instruction, a CMT with parameter word 0x0000 always sets GT-EQ and EQ and always resets LT and NE flags. Further, the CMT op code will never set LT and NE, while clearing GT-EQ and EQ flags.

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Name	*Instruction*	*Op Code*	*Parameter*	*Function*
LTT	Load Time Tag Counter *Conditional*	0x0D	Time Value (Resolution is programmed by bits 2-0 in the Time Tag Counter Configuration Register 0x0039)	If the Condition Code evaluates True, load the BC Time Tag Count Register 0x0043 with the parameter-specified Time Value. This represents bits 15-0 when the BC operates with 32-bit time tag. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List. Read LTH regarding LTT-LTH sequences.
LTH	Load Time Tag Counter High *Conditional* LTH only applies when 32-bit time base is enabled	0x18	Time Value (Resolution is programmed by bits 2-0 in the Time Tag Counter Configuration Register 0x0039)	If the Condition Code evaluates True, load the BC Time Tag Count High Register 0x0044 with the parameter-specified Time Value. This represents bits 31-16 when BC operates with 32-bit time tag. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List. If LTH immediately follows an LTT instruction, all 32 counter bits are loaded simultaneously. If LTH is not preceded by an LTT instruction, time count bits 15-0 in 0x0043 will be cleared to 0x0000 when bits 31-16 are written to register 0x0044. This instruction is only allowed when BCTT32 bit 3 is logic 1 in the Time Tag Counter Configuration register 0x0039, selecting 32-bit time base operation for the BC and RT(s). If BCTT32 is logic 0, this instruction stops instruction list execution, and generates an illegal instruction BCTRAP interrupt, if enabled.
LFT	Load Frame Timer *Conditional*	0x0E	Time Value (100 µs / LSB resolution)	If the Condition Code evaluates True, load the BC Frame Time Remaining Register 0x0035 with the parameter-specified Time Value. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.
SFT	Start Frame Timer *Conditional*	0x0F	Not Used (Don't Care)	If the Condition Code evaluates True, start decrementing the BC Frame Time Remaining Register 0x0035. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.
PTT	Push Time Tag Count *Conditional*	0x10	Not Used (Don't Care)	If the Condition Code evaluates True, push the value in the BC Time Tag Count Register 0x0043 onto the BC General Purpose Queue. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.

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Name	*Instruction*	*Op Code*	*Parameter*	*Function*
PTH	Push Time Tag Count High *Conditional* PTH only applies when 32-bit time base is enabled	0x19	Not Used (Don't Care)	If the Condition Code evaluates True, push the value in the BC Time Tag Count High Register 0x0044 onto the BC General Purpose Queue. This represents bits 31-16 when BC operates with 32-bit time tag. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List. This instruction is only allowed when BCTT32 bit 3 is logic 1 in the Time Tag Counter Configuration register 0x0039, selecting 32-bit time base operation for the BC and RT(s). If BCTT32 is logic 0, this instruction stops instruction list execution, and generates an illegal instruction BCTRAP interrupt, if enabled.
PTB	Push Time Tag Count Both *Conditional* PTB only applies when 32-bit time base is enabled	0x1A	Not Used (Don't Care)	If the Condition Code evaluates True, push the value in the BC Time Tag Count High Register 0x0044 and then push the value in the BC Time Tag Count (Low) Register 0x0043 onto the BC General Purpose Queue. (Both words are fetched simultaneously but pushed serially.) Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List. This instruction is only allowed when BCTT32 bit 3 is logic 1 in the Time Tag Counter Configuration register 0x0039, selecting 32-bit time base operation for the BC and RT(s). If BCTT32 is logic 0, this instruction stops instruction list execution, and generates an illegal instruction BCTRAP interrupt, if enabled.
PBS	Push Block Status Word *Conditional*	0x11	Not Used (Don't Care)	If the Condition Code evaluates True, push the value of the Block Status Word from the most recent message onto the BC General Purpose Queue. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.
PSI	Push Immediate Value *Conditional*	0x12	Immediate Value	If the Condition Code evaluates True, push the parameter-specified immediate value onto the BC General Purpose Queue. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.
PSM	Push Indirect *Conditional*	0x13	Memory Address	If the Condition Code evaluates True, push the value stored at the parameter-specified address onto the BC General Purpose Queue. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.
WTG	Wait for External Trigger *Conditional*	0x14	Not Used (Don't Care)	If the Condition Code evaluates True, wait for a rising edge (logic 0 to 1 transition) on the BCTRIG pin before continuing execution at the next op code in the BC Instruction List Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.

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Name	*Instruction*	*Op Code*	*Parameter*	*Function*
XQF	Execute and Flip *Unconditional*	0x15	RAM Address for Message Control/ Status Block	Unconditionally execute the message at the parameter-specified Message Control/Status Block Address. **At message completion**, if the Condition Code evaluates True, then toggle bit 4 of the Message Control/Status Block Address, and store the new Message Control/Status Block Address as the updated value of the parameter following the XQF instruction op code. As a result, the next time this address in the BC Instruction List is executed, the processed Message Control/ Status Block resides at the updated address (old address XOR 0x0010) instead of the old address. Otherwise (Condition Code Evaluates False) the value of the Message Control/Status Block Address parameter is not changed. At the start of XQF message execution, if the fourth word in the Message Control/Status Block is nonzero, it is copied to the BC Time to Next Message Register, and message timer begins decrementing. The BC message sequencer does not fetch the next instruction op code until this message timer reaches zero.
XFG	Execute, Flip and Go *Unconditional*	0x1A	RAM Address for Message Control/ Status Block	Unconditionally execute the message at the parameter-specified Message Control/Status Block Address. **At message completion**, if the Condition Code evaluates True, then toggle bit 4 of the Message Control/Status Block Address, and store the new Message Control/Status Block Address as the updated value of the parameter following the XFG instruction op code. As a result, the next time this address in the BC Instruction List is executed, the processed Message Control/ Status Block resides at the updated address (old address XOR 0x0010) instead of the old address. Otherwise (Condition Code Evaluates False) the value of the Message Control/Status Block Address parameter is not changed. At the start of XQG message execution, if the fourth (Time to Next Message) word in the Message Control/Status Block is nonzero, it is copied to the BC Time to Next Message Register 0x0036, and this message timer begins countdown. Completion of an XQG message may occur while message timer countdown continues. Unlike XQF, the XFG op code does not wait for the decrementing message timer to hit 0 before fetching the next instruction op code. As long as op codes following XFG do not execute a 1553 message, each op code is performed after fetch. Upon reaching a following XEQ, XQG, XQF or XFG execute-message instruction, transaction of its 1553 message does not begin until Time to Next Message count reaches 0. Thus, programmed 1553 message timing is maintained, while allowing execution of non-message instruction op codes.

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Name	*Instruction*	*Op Code*	*Parameter*	*Function*
WMP	Write Immediate Value to WMI Memory Pointer *Conditional*	0x1B	Immediate Value	If the Condition Code evaluates True, write the parameter-specified immediate value to the dedicated WMI memory pointer (a register not accessible by the host). Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List. Immediate value must exceed 0x4F or WMP instruction has no effect. After reset, the default WMI memory pointer value is 0x0050.
WMI	Write Immediate Value to Memory *Conditional*	0x1C	Immediate Value	If the Condition Code evaluates True, write the parameter-specified immediate value to 0x0050 or the memory address specified by the last WMP instruction performed. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List.
DSZ	Decrement RAM Specified by Memory Address, Skip the Next Instruction if Zero *Conditional*	0x1D	Memory Address	If the Condition Code evaluates True, the memory address specified by the parameter word is decremented. If the new value is non-zero, the next instruction is executed. If the decremented value is zero, the next instruction is skipped. Otherwise (Condition Code Evaluates False), continue execution at the next op code in the BC Instruction List. The primary purpose of DSZ is N-iteration repeating execution loops. N is initialized with a WMI op code, and the instruction following DSZ is a JMP to top-of-loop.
FLG	General Purpose Flag Bits *Unconditional*	0x0C	Word value sets, clears or toggles General Purpose Flag Bits	The parameter word value is used to set, clear, or toggle the lower byte in the BC General Purpose Flag Register 0x0037. The upper and lower bytes in the parameter word provide 2-bit arguments that modify each of the eight GP flag bits, as illustrated below.

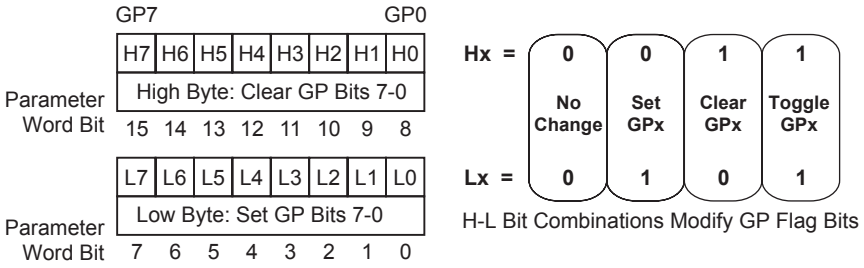

Figure 4. Bus Controller Flag Operation

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10.3. Bus Controller General Purpose Queue

The HI-613x BC architecture includes a General Purpose Queue, a 64-word circular stack which the BC can use to convey information to the external BC host. Various BC instruction op codes push data values onto the queue, such as the Block Status Word for the last message, Time Tag Counter values, immediate data values, or values stored in specific RAM addresses.

The BC General Purpose Queue Pointer 0x0038 (see Section 11.8) is initialized with the default starting address 0x00C0 after reset. The queue is relocatable, so the host may overwrite the default base address. Updated by the BC logic each time a data word is pushed onto the queue, the pointer in register 0x0038 always points to the next storage address in the queue to be written. The address pointer rolls over every 64th word written. If the BCGPQ bit 13 is logic 1 In the BC Interrupt Enable Register, a BC interrupt is generated when the General Purpose Queue Pointer rolls over from its ending address to its base address.

10.4. Bus Controller Message Control / Status Blocks

In the BC Instruction List, each occurrence of the “execute message” instructions, XEQ, XQG, XQF and XFG, references a MIL-STD-1553B message. The op code word is followed by the parameter word, a memory pointer indicating the RAM start address for a corresponding Message Control/Status Block. The pointer address indicates the first word in the Message Control/Status Block, the BC Control Word. Figure 5 illustrates this relationship.

The HI-613x is fully compatible with all MIL-STD-1553B message formats. For most MIL-STD-1553 messages, the corresponding Message Control/Status Block contains 8 words:

- **BC Control Word.** This word contains flags that select message format, choose the active bus, enable message retry and end-of-message interrupt, indicate expected RT status word flags, etc.
- **MIL-STD-1553 Command Word.** When message is RT-to-RT, this is the Receive Command Word.
- **Data Address Pointer.** For subaddress commands and mode code commands with data, this word identifies the start address of the Message Data Block in RAM. For mode commands without data, this word is not used.
- **Time-to-Next Message.** The time count loaded here begins decrementing at start of message. When value exceeds message execution time, it paces delivery of the next message.
- **Time Tag Word.** The current value of the internal time tag count is written to the Time Tag Word at Start-of-Message and again at the End-of-Message. When the BC uses a 16-bit time base, this location contains the complete time count. When the BC uses 32-bit time base, this word contains time bits 15-0 and block word 7 contains time bits 31-16 (instead of Loopback Word).
- **Block Status Word.** This word contains various message result flags.
- **Loopback Word,** containing the last word transmitted by the BC (16-bit time base only) or
  Time Tag Bits 31-16 (32-bit time base only)
- **RT Status Word** received.
  This is the **Transmit RT Status Word** when message is RT-to-RT.

When the message is RT-to-RT, the Message Control/Status Block contains 8 additional words:

- **Transmit Command Word.**
- **Receive RT Status Word.**
- Six unused word locations, to maintain 8 or 16 words per Message Control/Status Block.

Figure 5 shows the range of Message Control/Status Block variations. Selected words in the Message Control/Status Block are described next.

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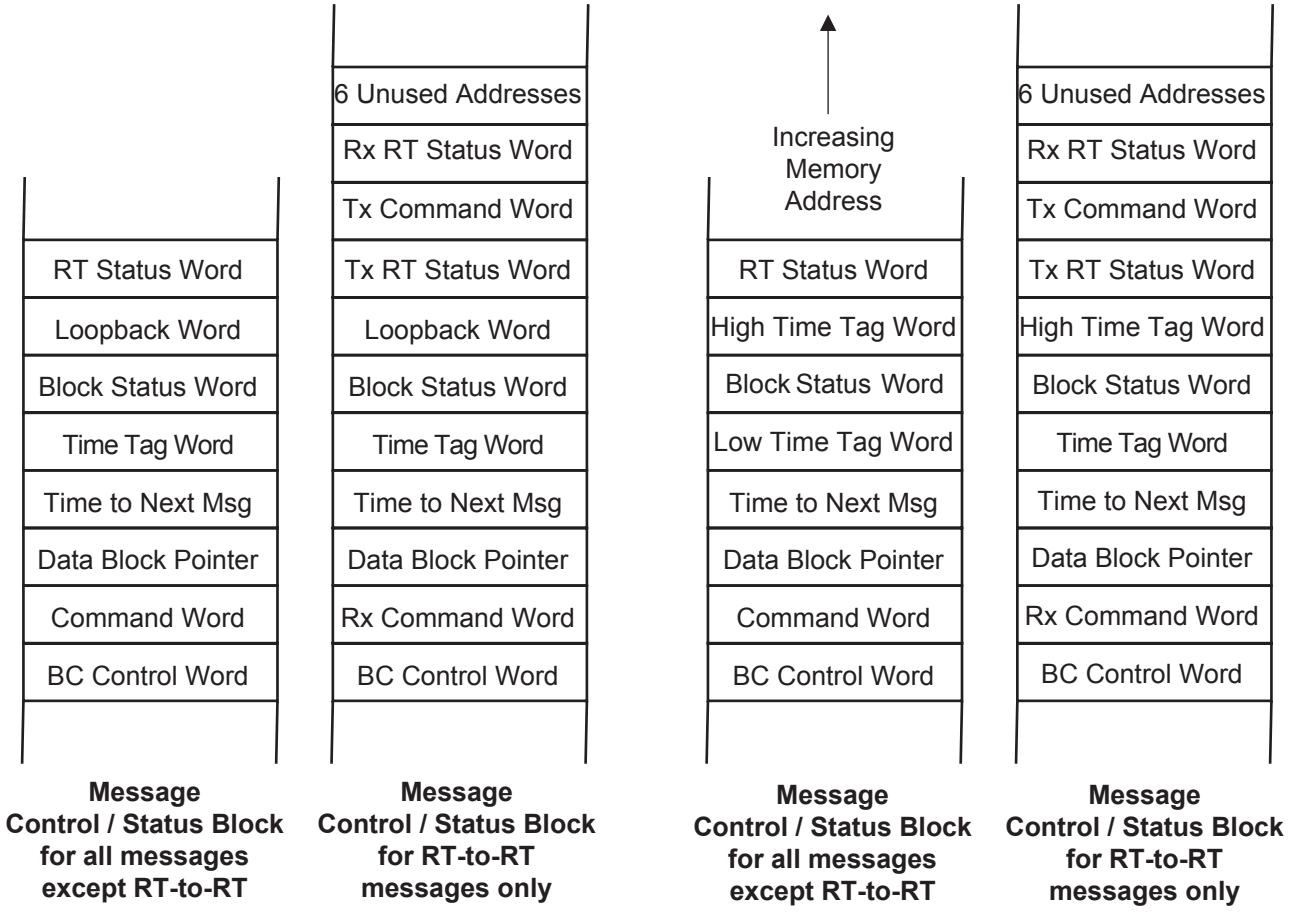
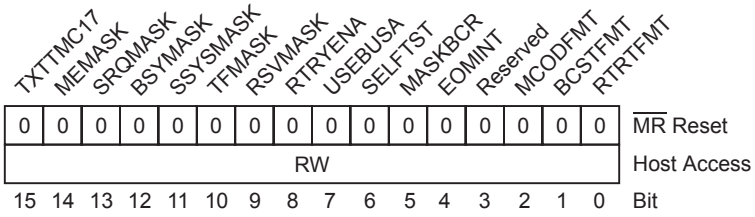


Figure 5. Structure of Bus Controller Message Control / Status Blocks in RAM

10.4.1. BC Control Word



The BC Control Word is the first word in each Message Control / Status Block. The BC Control Word is not transmitted on the MIL-STD-1553 bus. This word is initialized and maintained by the host to specify message attributes: message format, which bus to use, bit masks for the received RT Status Word, enabling interrupt at end-of-message, and enabling self test:

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Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*

15	TXTTMC17	R/W	0	Transmit Time Tag for Synchronize Mode Code Command MC17.
				This option bit only applies when BC Configuration Register TTSYNEN bit 3 is logic 1. See page 26. This bit affects only the “synchronize with data” mode code command, (mode code 0x11 or decimal 17).
				• If this Control Word bit is logic 0 (**or** if BC Configuration Register TTSYNEN bit 3 is logic 0) the BC transmits the value contained in the Message Data Block as the data word for a “synchronize” mode code command MC17. The transmitted word is fetched from the RAM address referenced by the Data Address Pointer.
				• If this Control Word bit **and** BC Configuration Register TTSYNEN bit 3 are both logic 1, the “synchronize” mode data word value originates from the 16-bit BC time base counter (low order 16 bits when using the 32-bit BC time base option).
				  • If BC Configuration Register ETTSYN bit 2 is also logic 1, the transmitted time tag data word is always an even value; the least significant bit is always 0.
				  • When ETTSYN bit 2 is logic 0, the data word least significant bit may be 0 or 1. See page 26.
				The transmitted data value is saved in the message data block, at the address indicated by the Data Address Pointer word.

14	MEMASK	R/W	0	Message Error Bit Mask. If this BC Control Word bit is logic 0 **and** the Message Error bit 10 is logic 1 in the received RT Status Word, a “Status Set” condition will result. If this BC Control Word bit is logic 1, the Message Error bit 10 in the received RT Status Word has no effect on the outcome for a “Status Set” condition. **Note:** A “Status Set” condition results if one or more of these events occurs: • one or more of the mask bits 14-9 in the BC Control Word is logic 0 **and** the corresponding bit is logic 1 in the received RT Status Word, • the BCRME bit 0 is logic 1 in the BC Configuration Register 0x0032 **and** the MASKBCR bit in the BC Control Word is logic 0 **and** the Broadcast Command Received bit 4 is logic 1 in the RT Status Word • the BCRME bit 0 is logic 0 in the BC Configuration Register 0x0032 **and** the MASKBCR bit in the BC Control Word differs from the Broadcast Command Received bit 4 in the RT Status Word • The received RT Status Word contains an RT Address field different from the RT Address field in the transmitted Command Word
13	SRQMASK	R/W	0	Service Request Bit Mask. If this BC Control Word bit is logic 0 **and** the Service Request bit 8 is logic 1 in the received RT Status Word, a “Status Set” condition will result. If this BC Control Word bit is logic 1, the Service Request bit 8 in the received RT Status Word has no effect on the outcome for a “Status Set” condition. See “Note” at end of MEMASK bit description above.

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Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
12	BSYMASK	R/W	0	Busy Bit Mask. If this BC Control Word bit is logic 0 **and** the Busy bit 3 is logic 1 in the received RT Status Word, a “Status Set” condition will result. If this BC Control Word bit is logic 1, the Busy bit 3 in the received RT Status Word has no effect on the outcome for a “Status Set” condition. See “Note” at end of MEMASK bit description above.
11	SSYSMASK	R/W	0	Subsystem Flag Bit Mask. If this BC Control Word bit is logic 0 **and** the Subsystem Flag bit 2 is logic 1 in the received RT Status Word, a “Status Set” condition will result. If this BC Control Word bit is logic 1, the Subsystem Flag bit 2 in the received RT Status Word has no effect on the outcome for a “Status Set” condition. See “Note” at end of MEMASK bit description above.
10	TFMASK	R/W	0	Terminal Flag Bit Mask. If this BC Control Word bit is logic 0 **and** the Terminal Flag bit 0 is logic 1 in the received RT Status Word, a “Status Set” condition will result. If this BC Control Word bit is logic 1, the Terminal Flag bit 0 in the received RT Status Word has no effect on the outcome for a “Status Set” condition. See “Note” at end of MEMASK bit description above.
9	RSVMASK	R/W	0	Reserved Bits Mask. If this BC Control Word bit is logic 0 **and** one or more of the three Reserved bits 7-5 is logic 1 in the received RT Status Word, a “Status Set” condition will result. If this BC Control Word bit is logic 1, the three Reserved bits 7-5 in the received RT Status Word have no effect on the outcome for a “Status Set” condition. See “Note” at end of MEMASK bit description above.
8	RTRYENA	R/W	0	Retry Enabled. If this Control Word bit is logic 1 **and** BCRE (BC Retry Enable) bit 12 is logic 1 in the BC Configuration Register 0x0032, the BC will retry a message if RT response timeout or Format Error occurs. If this Control Word bit is logic 1 **and** BCRE (BC Retry Enable) bit 12 is logic 1 **and** BCRSB (BC Retry If Status Word Bits Set) bit 8 is also logic 1 in the BC Configuration Register 0x0032, the BC will retry a message when a “Status Set” condition occurs. See “Note” at end of MEMASK bit 14 description above.
7	USEBUSA	R/W	0	Use Bus A / $\overline{\text{Use Bus B}}$. If this Control Word bit is logic 1, the BC transmits the command on Bus A. If this Control Word bit is logic 0, the BC transmits the command on Bus B.

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Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
6	SFTST	R/W	0	Self-Test Message Off-Line. If this Control Word bit is logic 1, transmission of this message onto the 1553 bus is inhibited. Instead the digitally-encoded Command Word is looped back into the receive decoder for the selected bus. This tests both the encoding and decoding signal paths. Upon message completion, Loop Test Fail bit 8 in the Block Status Word indicates the self-test result. If BC is configured for 16-bit time base, the received Loopback Word is stored in the Message Control/Status Block. If the BC is configured for 32-bit time base, time tag bits 31-16 are stored in the Loopback Word location.
5	MASKBCR	R/W	0	Mask Broadcast Command Received Bit. **If the BCRME bit 0 is logic 1 in the BC Configuration Register** 0x0032, then this Control Word bit is a “mask bit” like bits 14-9, acting upon the BCR Broadcast Command Received bit 4 in the received RT Status Word: • If this MASKBCR Control Word bit is logic 0 **and** the Broadcast Command Received bit 4 is logic 1 in the received RT Status Word, a “Status Set” condition will result. • If this MASKBCR Control Word bit is logic 1, the Broadcast Command Received bit 4 in the received RT Status Word has no effect on the outcome for a “Status Set” condition. **If the BCRME bit 0 is logic 0 in the BC Configuration Register** 0x0032, then this MASKBCR Control Word bit reflects the expected state of the Broadcast Command Received bit 4 in the received RT Status Word: • If this MASKBCR Control Word bit **does not match** the logic state of the Broadcast Command Received bit 4 in the received RT Status Word, a “Status Set” condition will result. • If this MASKBCR Control Word bit **matches** the logic state of the Broadcast Command Received bit 4 in the received RT Status Word, then the Broadcast Command Received bit 4 in the received RT Status Word has no effect on the outcome for a “Status Set” condition. See Table 7.
4	EOMINT	R/W	0	End of Message Interrupt. If the BCEOM bit 3 is logic 1 in the BC Interrupt Enable Register 0x0010, an EOM interrupt will occur upon message completion, if this Control Word bit is logic 1.
3	Reserved	R/W	0	This bit is not used.

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>2
1
0</td><td>MCODFMT
BCSTFMT
RTRTFMT</td><td>R/W</td><td>0</td><td>Mode Code Message Format.
Broadcast Message Format.
RT to RT Message Format.
The combination of these three Message Format bits selects the MIL-STD-1553B message type:
<table>
<tr><th>Mode Code Bit 2</th><th>Broadcast Bit 1</th><th>RT-RT Bit 0</th><th>Message Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>BC-to-RT if the T/$\overline{R}$ bit * equals logic 0
RT-to-BC if the T/$\overline{R}$ bit * equals logic 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RT-to-RT</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Broadcast BC-to-RT</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Broadcast RT-to-RT</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Mode Code Command</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Do Not Use</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Broadcast Mode Code Command</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Do Not Use</td></tr>
</table>
* Transmit / $\overline{\text{Receive}}$ bit in Command Word
Note: Bit 0 must be logic 1 for RT-RT messages. This is the single control point enabling the 16-word Control Block that configures RT-RT messages.</td></tr>
</table>

10.4.2. Time to Next Message Word

The HI-613x Bus Controller provides a programmable delay for Time to Next Message. This word in the Message Control / Status Block specifies the delay from the start of this message, to the start of the next message. The delay is programmable with 1 µs per LSB resolution, and has a maximum value of 65.535 milliseconds.

When the specified Time to Next Message value is less than the actual time required to transact the current message, the next message starts immediately upon completion current message, after the minimum inter-message gap time of 4µs. This gap corresponds to a bus “dead time” of 2µs.

10.4.3. Data Block Pointer

The Data Block Pointer in the Message Control / Status Block provides the starting address in RAM for storage of message data words or mode code data. For BC-to-RT (receive) commands, this pointer contains the RAM location for the first data word transmitted by the BC.

For RT-to-BC (transmit) commands or RT-to-RT commands, this pointer contains the RAM location for storing the first data word transmitted by the RT (and received by the BC).

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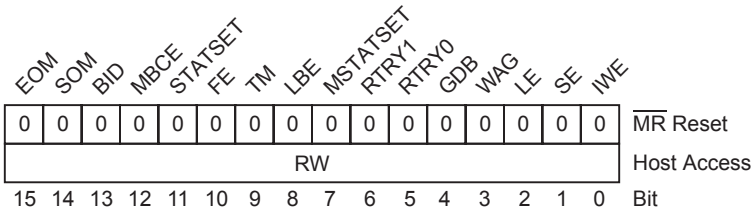
10.4.4. BC Block Status Word



The Block Status Word in the Message Control / Status Block provides information regarding message status (in-process or completed), the bus it was transmitted on, whether errors occurred during the message, and the type of occurring errors. This word is written into RAM by the device after message completion. Because it resides in RAM, the host has read-write access, although this word is usually treated as read-only by the host.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	EOM	R/W	0	End of Message. This bit is set upon completion of a BC message, whether or not errors occurred. When EOM is set, the current value of the Time Tag Word(s) is (are) written to the corresponding Time Tag Word(s) in the BC Message Control/Status Block.
14	SOM	R/W	0	Start of Message. This bit is set at the start of a BC message and cleared at the end of the message. When SOM is set (and reset), the current value of the Time Tag Word(s) is (are) written to the corresponding Time Tag Word(s) in the BC Message Control/Status Block.
13	BID	R/W	0	Bus ID (Bus B / $\overline{\text{Bus A}}$). This bit is logic 1 if the BC message was transacted on Bus B. This bIt is logic 0 if the BC message was transacted on Bus A.
12	MBCE	R/W	0	Message Block Coding Error. A programming test aid, this bit only applies when CHKFMT bit 13 is logic 1 in the BC Configuration Register. Each message BC Control Word has flags that indicate format: mode code command (bit 2), RT-RT message (bit 1) and broadcast message (bit 0). When CHKFMT is 1, these flags are compared to the message Command Word(s) that follow the Control Word in the Message Block. When message format mismatch occurs (a BC programming error), this MBCE bit is set in the message Block Status Word. See CHKFMT description in “BC (Bus Controller) Configuration Register (0x0032)” on page 71.

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Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
11	STATSET	R/W	0	Status Set. This bit is not affected by the values of mask bits 14-9 in the BC Control Word for the message. This bit is logic 1 when the received RT Status Word contains an unexpected bit value in the bit 10-0 range. The expected value is usually logic 0 for bits 10-0 in the received RT Status Word. Exception: the expected value for Broadcast Command Received bit 4 in the received RT Status Word is logic 1 when BCRME bit 0 is logic 1 in the BC Configuration Register 0x0032, **and** MASKBCR bit in the BC Control Word bit is logic 0
10	FE	R/W	0	Format Error. This bit is logic 1 when a received RT response violates MIL-STD-1553 message validation criteria. This includes sync, word count, encoding, bit count or parity errors. Word bits 2-0 provide additional information. This flag is also set when the received RT Status Word response from the last message contained an incorrect RT address field.
9	TM	R/W	0	No Response Timeout Error. This bit is logic 1 when an RT fails to respond, or responds later than the BC No Response Timeout interval specified by bits 15-14 in the BC Configuration Register 0x0032.
8	LBE	R/W	0	Loopback Error. The HI-613x BC evaluates its own 1553 message transmissions. The received version of each word transmitted by the BC is checked for 1553 validity (sync, encoding, bit count and/or parity error). In addition, for each message transacted, the received image for the last word transmitted by the BC is evaluated for data match. This bit is logic 1 when the received version for one or more words transmitted by the BC fails 1553 “word validity” criteria, and/or the received version for the last word transmitted by the BC does not match the Manchester II word transmitted by the BC.
7	MSTATSET	R/W	0	Masked Status Set. This bit is logic 1 when any of the following conditions occurs: • One or more of the mask bits 14-9 in the BC Control Word is logic 0 **and** the corresponding bit is logic 1 in the received RT Status Word. • Or the BCRME bit 0 is logic 1 in the BC Configuration Register 0x0032 **and** the MASKBCR bit in the BC Control Word is logic 0 **and** the Broadcast Command Received bit 4 is logic 1 in the RT Status Word. • Or the BCRME bit 0 is logic 0 in the BC Configuration Register 0x0032 **and** the MASKBCR bit in the BC Control Word **differs from** the Broadcast Command Received bit 4 in the RT Status Word. • Or the received RT Status Word contains an RT Address field different from the RT Address field in the transmitted Command Word.

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>6
5</td><td>RTRY1
RTRY0</td><td>R/W</td><td>0</td><td>Retry Count 1 and Retry Count 0

If BCRE (BC Retry Enable) bit 12 is logic 1 in the BC Configuration Register 0x0032 and RTRYENA bit 8 is logic 1 in the BC Control Word for this message, the BC will retry the message if RT response timeout or Format Error occurs.

Also, if BCRE (BC Retry Enable) bit 12 is logic 1 and BCRSB (BC Retry if Status Word Bits Set) bit 8 is logic 1 in the BC Configuration Register 0x0032 and RTRYENA bit 8 is logic 1 in the BC Control Word for this message, the BC will retry the message when a “Status Set” condition occurs. See “MSTATSET” bit 7 description above.

The combination of these two bits indicates the number of times this message was retried:
<table>
<tr><th>RTRY1 Bit 6</th><th>RTRY0 Bit 5</th><th>Number of Retries</th></tr>
<tr><td>0
0
1
1</td><td>0
1
0
1</td><td>0
1
2
Not Used</td></tr>
</table>
</td></tr>
<tr><td>4</td><td>GDB</td><td>R/W</td><td>0</td><td>Good Transmit Data Block Transfer.

This bit is set to logic 1 upon successful completion of an error-free RT-to-BC message, RT-to-RT message, or transmit mode code message with data. This bit always resets to logic 0 for any BC-to-RT message, mode code message without data, or any incomplete or invalid message.

This bit may be used for determining when the transmit portion of an RT-to-RT message is error-free. If this bit and Error Flag bit 12 are both set to logic 1 in the Block Status Word for an RT-to-RT message, the transmitting RT responded correctly but error occurred in the receiving RT portion of the message.</td></tr>
<tr><td>3</td><td>WAG</td><td>R/W</td><td>0</td><td>Wrong RT Address and/or No Gap.

This bit is logic 1 when one or both of the following conditions occur

• the RT address field within a received RT Status Word does not match the RT address field in the Command Word transmitted by the BC
• the BCGCE BC Gap Check Enable bit 1 in the BC Configuration Register 0x0032 and the RT responds with response time less than 4 µs per MIL-STD-1553B, mid-parity bit to mid-sync, (2 µs bus “dead time”).</td></tr>
<tr><td>2</td><td>LE</td><td>R/W</td><td>0</td><td>Word Count (Length) Error.

This bit is logic 1 when an RT-to-BC message, RT-to-RT message, or transmit mode code message with data is transacted with the wrong number of data words.

This bit always resets to logic 0 for BC-to-RT messages, receive mode code messages, or transmit mode code messages without data.</td></tr>
<tr><td>1</td><td>SE</td><td>R/W</td><td>0</td><td>Sync Error.

This bit is logic 1 when an RT responds with Data Sync in its Status Word, or with Command/Status Sync in a Data Word.</td></tr>
</table>

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Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
0	IWE	R/W	0	Invalid Word Error. This bit is logic 1 when an RT response in one or more words having at least one of the following errors: sync encoding error, Manchester II encoding error, bit count error, parity error.

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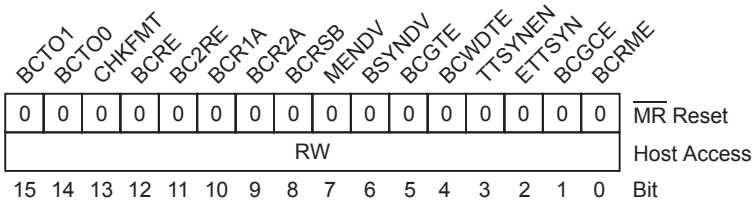
11. BUS CONTROLLER REGISTER DESCRIPTION

In addition to the registers described here, a HI-6131 Bus Controller also utilizes one or more Memory Address Pointer registers (described in Section 9.8) for managing SPI read/write operations. This comment does not apply for parallel bus interface HI-6130 designs.

11.1. BC (Bus Controller) Configuration Register (0x0032)



Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15 − 14	BCTO1:0	R/W	0	BC Time Out Select. This 2-bit field selects the BC “no response” time-out delay from four available selections. Excluding RT-RT commands, response delay is measured from command word mid-parity bit to status word mid-sync:

Bit 11:10	***Bus Dead Time***	***Time Out (excludes RT-RT)***
00	15µs	17µs
01	20µs	22µs
10	58µs	60µs
11	138µs	140µs

For RT-RT commands, time out delay is measured per Figure 8 in the RT Validation Test Plan, SAE AS4111. That is, from mid-parity of the receive command to mid-sync of the first received data word. This adds 42µs for the embedded parity half-bit, transmit command word, transmit-RT status word and data half-sync within this interval:

Bit 11:10	***TxRT Bus Dead Time***	***RT-RT Time Out****
00	18µs	60µs
01	23µs	65µs
10	58µs	100µs
11	138µs	180µs

***Note:** per RT Validation Test Plan, Fig. 8.

All time out select values have –100ns / +500ns tolerance.

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Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
13	CHKFMT	R/W	0	Check Message Format. When this bit equals logic 1, BC Control Word message format bits 2-0 (mode command, RT-RT message and broadcast flags) are compared to values for the message Command Word(s) that follow the Control Word in the Message Block. This is provided as a BC program development aid. When the CHKFMT bit is logic 1 and message format mismatch occurs, the MBCE Message Block Coding Error bit 12 is set in the message Block Status Word (**page xx**). If enabled, BC Trap interrupt is generated (**page xx**). When the CHKFMT bit is logic 0, no format checking occurs between BC Control Word bits 2-0 and the MIL-STD-1553 message Command Word(s). Even with message format checking disabled, BC Control Word bit 0 **must be** logic 1 for RT-RT messages. *This is the single control point enabling the 16-word BC Control Block that configures an RT-to-RT message*.
12	BCRE	R/W	0	BC Retry Enable. If bit 12 equals logic 0, command retries are disabled for all messages. If bit 12 equals logic 1, command retries can be enabled on an individual message basis by setting bit 8 in the BC Control Word for all messages to be retried.
11	BC2RE	R/W	0	BC Second Retry Enable. If retries are enabled (register bit 12 equals 1) this bit selects the number of retries performed, If bit 11 equals logic 0, a single retry is performed. If bit 11 equals logic 1, up to two retries are performed.
10	BCR1A	R/W	0	BC First Retry Use Alternate Bus. If retries are enabled (register bit 12 equals 1) this bit selects the bus used for the first retry. If bit 10 equals 0, the first retry is performed on the same bus from which the message was originally transmitted. If bit 10 equals 1, first retry is performed on the alternate bus from which the message was originally transmitted.
9	BCR2A	R/W	0	BC Second Retry Use Alternate Bus. If first and second retries are enabled (register bits 12:11 equal 1-1) this bit selects the bus used for the second retry. If bit 9 equals 0, the second retry is performed on the same bus where the message was originally transmitted. If bit 9 equals 1, second retry is performed on the alternate bus from where the message was originally transmitted.

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>8</td><td>BCRSB</td><td>R/W</td><td>0</td><td>BC Retry If Unmasked Status Word Bit Set.

This bit affects operation of BC retries. If bit 8 equals logic 0, the BC will not retry messages because of status bit(s) set in the RT Status Word, or Status Word with non-matching RT address field.

If retries are enabled and bit 8 equals logic 1, the BC will retry messages for these RT status word results:

1. One or more BC Control Word mask bits 14-9 is logic 0 (bits are not masked) and the corresponding bit is logic 1 in the received RT Status Word.

2. The BCR Mask Enable bit 0 equals 0 in the BC Configuration Register 0x0032. The Broadcast Command Received (BCR) bit in the received RT Status Word differs from the Mask BCR bit (bit 5) in the BC Control Word.

3. Received Status Word RT address does not match Command Word RT address.</td></tr>
<tr><td>7</td><td>MENDV</td><td>R/W</td><td>0</td><td>Message Error Status, No Data is Valid

Bit 7 affects BC validation of RT responses to transmit commands when the Message Error (ME) bit is asserted in the received RT Status Word.

When the MENDV bit equals logic 0:

• When an RT responds Message Error status to a transmit command, the response is valid only if the Status Word is followed by the commanded number of data words. Message result:
<table>
<tr><th>Condition</th><th>Block Status Word</th><th>Condition Code Register</th></tr>
<tr><td>Commanded number of data words</td><td>Good Data Block (GDB) bit = 1</td><td>Good Data Block (GDBT) bit = 1</td></tr>
<tr><td rowspan="2">If MEMASK = 1 in BC Control Word</td><td>Masked Status Set (MSTATSET) bit = 1.</td><td>Masked Status Set (MSTATSET) bit = 1.</td></tr>
<tr><td>Status Set (STATSET) bit = 1.</td><td>----------</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td rowspan="2">7</td><td rowspan="2">MENDV (continued)</td><td rowspan="2">R/W</td><td rowspan="2">0</td><td>
• If the RT responds Message Error status to a transmit command with the wrong number of data words or no data words, here is the message result:
<table>
<tr><th>Condition</th><th>Block Status Word</th><th>Condition Code Register</th></tr>
<tr><td>Wrong number of (or no) data words</td><td>Format Error (FE) bit = 1</td><td>Format Error (FMTERR) bit = 1</td></tr>
<tr><td rowspan="3">If MEMASK = 1 in BC Control Word</td><td>Masked Status Set (MSTATSET) bit = 1.</td><td>Masked Status Set (MSTATSET) bit = 1.</td></tr>
<tr><td>Word Count Error (LE) bit = 1.</td><td>Bad Message (BADMSG) bit = 1</td></tr>
<tr><td>Status Set (STATSET) bit = 1.</td><td>----------</td></tr>
</table>
</td></tr>
<tr><td>
When the MENDV bit equals logic 1:
• When an RT responds Message Error status to a transmit command, the response is valid with the commanded number of data words, or ME status with no data words. Here is the message result:
<table>
<tr><th>Condition</th><th>Block Status Word</th><th>Condition Code Register</th></tr>
<tr><td>Commanded # of data words only, “Good Data” is not shown if no data</td><td>Good Data Block (GDB) bit = 1</td><td>Good Data Block (GDBT) bit = 1</td></tr>
<tr><td rowspan="2">If MEMASK = 0 in BC Control Word</td><td>Masked Status Set (MSTATSET) bit = 1.</td><td>Masked Status Set (MSTATSET) bit = 1.</td></tr>
<tr><td>Status Set (STATSET) bit = 1.</td><td>----------</td></tr>
</table>
</td></tr>
</table>

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td rowspan="2">7</td><td rowspan="2">MENDV
(continued)</td><td rowspan="2">R/W</td><td rowspan="2">0</td><td>
• If the RT responds Message Error status to a transmit command with the wrong number of data words (not 0), here is the message result:
<table>
<tr><th>Condition</th><th>Block Status Word</th><th>Condition Code Register</th></tr>
<tr><td>Wrong number of data words</td><td>Format Error (FE) bit = 1</td><td>Format Error (FMTERR) bit = 1</td></tr>
<tr><td rowspan="3">If MEMASK = 0 in BC Control Word</td><td>Masked Status Set (MSTATSET) bit = 1.</td><td>Masked Status Set (MSTATSET) bit = 1.</td></tr>
<tr><td>Word Count Error (LE) bit = 1.</td><td>Bad Message (BADMSG) bit = 1</td></tr>
<tr><td>Status Set (STATSET) bit = 1.</td><td>----------</td></tr>
</table>
</td></tr>
<tr><td>
The only 3 cases when an RT transmits Message Error status onto the bus:
1. An RT using “illegal command detection” receives an illegal command that otherwise meets all other validation requirements. The RT responds with Status Word only, with Message Error bit set. No data words are sent.
2. An RT receives a “transmit status” mode command (MC2). The previous valid command for the RT had Message Error status. The RT responds with Status Word only, with Message Error bit set. No data words are sent.
3. An RT receives a “transmit last command” mode command (MC18 decimal). The previous valid command for the RT set Message Error status. The RT responds with Status Word (with Message Error bit set) and one data word, the previous Command Word.
In summary, Message Error status never occurs with more than one data word, and only occurs with one data word for the “transmit last command” mode code.
Besides illegal command detection, there is just one situation where Message Error status occurs, but Status transmission is suppressed: The RT detects a valid receive command having correct RT address, but an invalid word is detected in the accompanying data words, or a gap occurs between words. In this situation, Message Error status is set but the RT suppresses its Status Word transmission. This suppressed ME status is only seen by the BC if retrieved by a following “transmit status’’ or “transmit last command” mode command.
</td></tr>
</table>

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>6</td><td>BSYNDV</td><td>R/W</td><td>0</td><td>
Busy Status, No Data, is Valid
Bit 6 affects BC validation of RT responses to transmit commands when the Busy bit is asserted in the received RT Status Word.
When the BSNDV bit equals logic 0:
When an RT responds Busy status to a transmit command, the response is valid only if the Status Word is followed by the commanded number of data words. Here is the message result:
<table>
<tr><th>Condition</th><th>Block Status Word</th><th>Condition Code Register</th></tr>
<tr><td>Commanded number of data words</td><td>Good Data Block (GDB) bit = 1</td><td>Good Data Block (GDBT) bit = 1</td></tr>
<tr><td rowspan="2">If BSYMASK = 1 in BC Control Word</td><td>Masked Status Set (MSTATSET) bit = 1.</td><td>Masked Status Set (MSTATSET) bit = 1.</td></tr>
<tr><td>Status Set (STATSET) bit = 1.</td><td>----------</td></tr>
</table>
• If the RT responds Busy status to a transmit command with the wrong number of data words or no data words, here is the message result:
<table>
<tr><th>Condition</th><th>Block Status Word</th><th>Condition Code Register</th></tr>
<tr><td>Wrong number of (or no) data words</td><td>Format Error (FE) bit = 1</td><td>Format Error (FMTERR) bit = 1</td></tr>
<tr><td rowspan="3">If BSYMASK = 1 in BC Control Word</td><td>Masked Status Set (MSTATSET) bit = 1.</td><td>Masked Status Set (MSTATSET) bit = 1.</td></tr>
<tr><td>Word Count Error (LE) bit = 1.</td><td>Bad Message (BADMSG) bit = 1</td></tr>
<tr><td>Status Set (STATSET) bit = 1.</td><td>----------</td></tr>
</table>
When the BSNDV bit equals logic 1:
• When an RT responds to a transmit command with Busy status, the response is valid when accompanied by the commanded number of data words, or accompanied by no data words. Here is the message result:
<table>
<tr><th>Condition</th><th>Block Status Word</th><th>Condition Code Register</th></tr>
<tr><td>Commanded # of data words only, “Good Data” is not shown if no data</td><td>Good Data Block (GDB) bit = 1</td><td>Good Data Block (GDBT) bit = 1</td></tr>
<tr><td rowspan="2">If BSYMASK = 0 in BC Control Word</td><td>Masked Status Set (MSTATSET) bit = 1.</td><td>Masked Status Set (MSTATSET) bit = 1.</td></tr>
<tr><td>Status Set (STATSET) bit = 1.</td><td>----------</td></tr>
</table>
</td></tr>
</table>

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td rowspan="2">6</td><td rowspan="2">BSYNDV
(continued)</td><td rowspan="2">R/W</td><td rowspan="2">0</td><td>
• If the RT responds to a transmit command with Busy status and the wrong number of data words (but not 0), here is the message result:
<table>
<tr><th>Condition</th><th>Block Status Word</th><th>Condition Code Register</th></tr>
<tr><td>Wrong number of data words</td><td>Format Error (FE) bit = 1</td><td>Format Error (FMTERR) bit = 1</td></tr>
<tr><td rowspan="3">If BSYMASK = 0 in BC Control Word</td><td>Masked Status Set (MSTATSET) bit = 1.</td><td>Masked Status Set (MSTATSET) bit = 1.</td></tr>
<tr><td>Word Count Error (LE) bit = 1.</td><td>Bad Message (BADMSG) bit = 1</td></tr>
<tr><td>Status Set (STATSET) bit = 1.</td><td>----------</td></tr>
</table>
</td></tr>
<tr><td>A busy RT is one that is functional, but cannot send or receive data when commanded by the Bus Controller. An RT that is busy sets the Busy bit in its Status Word responses. In response to transmit commands, the busy terminal has no words to transmit, so only the Status Word is transmitted. In the case of the “transmit vector word” and transmit BIT word” mode code commands, even if the data is available to the terminal, it is prohibited to send the data word if the Busy bit is set in the Status Word.

There is just one defined situation in which an RT transmits Busy status with one (and only one) data word: An RT receives a “transmit last command” mode command (MC18 decimal). When the previous valid command for the RT had Busy status, the RT responds with last message status condition (with Busy bit set) and one data word, the previous Command Word.</td></tr>
<tr><td>5</td><td>BCGTE</td><td>R/W</td><td>0</td><td>BC Message Gap Timer Enable.

If bit 5 is logic 0, the BC does not add delay between 1553 messages. Message timing is paced by the time required for the BC to complete message post processing. In this case, the minimum inter-message gap will be used, with a bus “dead time” of approximately 6 to 9µs.

If bit 5 is logic 1, the BC Message Timer is enabled. The “Time to Next Message” value from the Message Control Block is decremented at 1µs rate. When the count decrements from 1 to 0, the next message starts. If the specified message gap time is less than the time needed for the current message, the next message will start immediately after completion of the current message. In this case, the minimum inter-message gap will be used, with a bus “dead time” of approximately 6 to 9µs. This allows the BC to implement minor frame cycle times without host processor intervention.</td></tr>
</table>

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Bit No.	Mnemonic	R/W	Reset	Function
4	BCWDTE	R/W	0	BC Watchdog Timer (WDT) Enabled. When this bit is logic 1, if the End of Frame (EOF) interrupt bit is set in the BC Interrupt Enable register, the BC sets the EOF bit in the BC Pending Interrupt register when the BC Frame Timer decrements from 1 to 0. When using this feature, it is necessary to periodically reload the Frame Time register by means of the LFT Load Frame Time op code in the BC message sequence control block. The loaded value must allow for the worst-case frame time (including message retries). The WDT provides a failsafe recovery from faults such as message sequence stuck in repetitive loop without LFT reload, or execution jumping to the wrong sequence.
3	TTSYNEN	R/W	0	BC Time Tag Synchronization Enable This option bit only affects the “synchronize with data” mode code command, MC17. When this bit is logic 1, the source of the mode data issued with the “synchronize” mode command is determined by message BC Control Word TXTTMC17 bit 15 (see Section 10.4.1) • If BC Control Word TXTTMC17 bit 15 = logic 0, the “synchronize” mode data word originates from the message data block, at the RAM address indicated by the Data Address Pointer word. • If BC Control Word TXTTMC17 bit 15 = logic 1, the “synchronize” mode data word value originates from the 16-bit BC time base counter (or the low order 16 bits, when using the 32-bit BC time base option). The transmitted data value is saved in the message data block, at the address indicated by the Data Address Pointer word. If the TTSYNEN bit is logic 0, regardless of the state of message Control Word bit 15, the “synchronize with data” mode command (MC17) is always issued with mode data originating from the message data block, at the RAM address indicated by the Data Address Pointer word.
2	ETTSYN	R/W	0	Even Time Tag Sync. This bit only applies when TTSYNEN bit 3 is logic 1 **and** BC Control Word TXTTMC17 bit 15 is also logic 1, selecting “synchronize” mode data origin as time base counter. In this case, if ETTSYN is logic 1, the transmitted time tag data word is always even; the low order bit is always 0. When the ETTSYN bit is logic 0, the data word may be even or odd; the LSB may be 0 or 1.

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Bit No.	Mnemonic	R/W	Reset	Function
1	BCGCE	R/W	0	BC Gap Check Enable. When this bit is logic 1, the BC verifies that any transmission by a Remote Terminal on the bus is preceded by an inter-word gap of at least 4µs. When this minimum gap time is violated, the BC declares the RT Status Word invalid, and the No Gap error bit is set in the Block Status Word. Gap detection measures the time span from mid-parity of last received word, to mid-sync of the following word (defined here as detection of a properly encoded sync plus two bits). Measured gap time is adjusted to evaluate just the interval of interest, corresponding to a bus "dead time" (end-of-parity to start-of-sync) of 2µs minimum. When this bit is logic 0 **(strongly recommended)** the BC does not check for minimum bus "dead time" prior to start of transmission by a device on the MIL-STD-1553 bus.
0	BCRME	R/W	0	BCR Mask Enable. This bit selects the function of BC Control Word bit 5, Mask Broadcast, when evaluating the BCR (Broadcast Command Received) bit in RT status words. **If BCR Mask Enable bit 0 is logic 1**, then RT status word BCR bit masking is enabled. The state of the Mask BCR bit in each BC Control Word selectively allows or disallows BCR status testing by the BC: • When "Mask BCR" is logic 1 in a message's BC Control Word (disabling BCR status bit test), the value of the RT status word BCR bit is "don't care" in terms of affecting the occurrence of a "Status Set" condition. • When "Mask BCR" is logic 0 in the message's BC Control Word, "Status Set" occurs when the BCR bit in the received RT Status Word is logic 1. • While broadcast commands never result in transmitted RT status, the "Mask BCR" bit should be set in BC Control Words for "transmit status" or "transmit last command" mode commands immediately following broadcast messages. Setting the "Mask BCR" bit of the message's BC Control Word to logic 1 indicates the expected value of the BCR bit in the received RT Status Word. **If BCR Mask Enable bit 0 is logic 0**, the "Mask BCR" bit in a message's BC Control Word indicates the expected state of the BCR bit in the received RT status word. In this situation, whenever the BCR bit in the received RT status word differs from the state of the "Mask BCR" bit in the BC Control Word, a "Status Set" condition occurs and the BC generates a Status Set interrupt, if enabled. Table 7 summarizes the effects of BC configuration, message Control Word and RT Status Word on "Status Set" bit in the Block Status Word.

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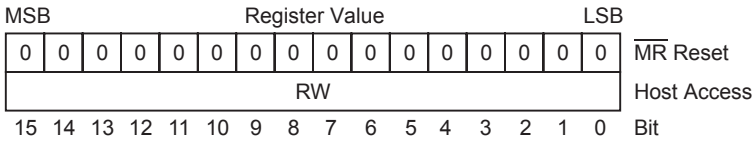
Table 7. Effect of “Broadcast Command Received” RT Status Bit on “Status Set” Condition

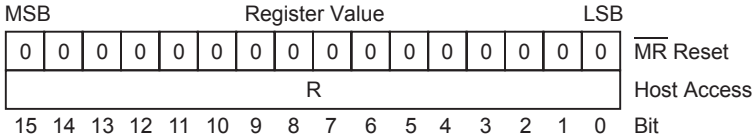
BC Configuration Register 0x0032 “BCR Mask Enable” bit 0	Message Control Word “Mask BCR” bit 5	Received BCR bit 4 in the Remote Terminal Status Word	Resultant Block Status Word “Status Set” bit 11
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	X	0

11.2. Start Address Register for Bus Controller (BC) Instruction List (0x0033)



This 16-bit register is Read-Write and is fully maintained by the host. This register is cleared after $\overline{MR}$ pin master reset. This register is initialized with the base address of the re-locatable BC Instruction List in device RAM.

11.3. Bus Controller (BC) Instruction List Pointer (0x0034)



This 16-bit register is Read-Only and is fully maintained by the device. When the bus controller is enabled, setting BCSTRT bit 13 in the Master Configuration Register begins bus controller operation. The device copies the Instruction List base address from register 0x0033 into this register. This pointer references pairs of words in the BC instruction list. Each word pair is comprised of an op code word followed by a parameter word. Pointer update occurs just before execution of the next BC instruction list op code, after execution of the prior op code, and evaluation of its result-dependent outcome.

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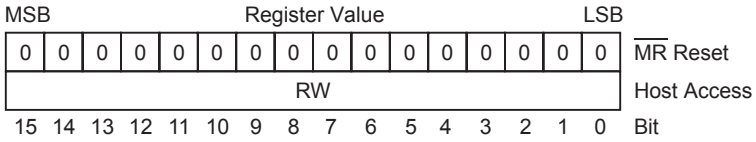
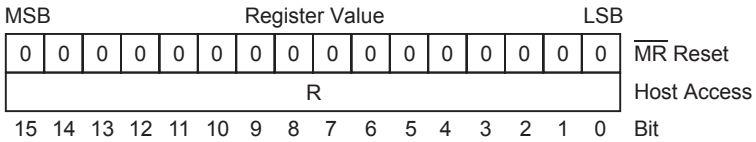
11.4. Bus Controller (BC) Frame Time Remaining Register (0x0035)



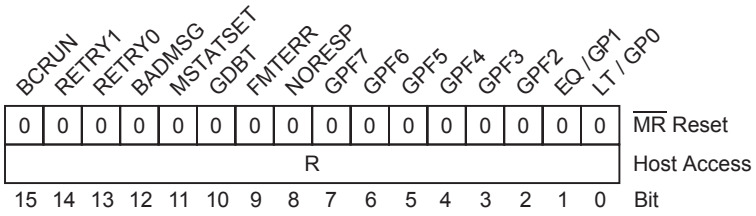
This 16-bit register is Read-Write. A value is written to this register upon execution of the BC instruction list op code, “Load Frame Timer” (LFT). Time remaining value begins decrementing upon execution of the Start Frame Timer (SFT) instruction op code. The parameter word accompanying the op code word is the desired time value, expressed with a resolution of 100 µs per LSB, with a maximum value of 6.5535 sec.

11.5. Bus Controller (BC) Time To Next Message Register (0x0036)



This 16-bit register is Read-Only. This programmable time-to-next message timer is loaded on a message-by-message basis, with values from word 4 in each Message Control / Status Block. The BC time-to-next message is defined as the time from the start of the current message to the start of the next message, i.e., mid-sync zero crossing to the next mid-sync zero crossing. This timer provides a 1 µs per LSB resolution, with a maximum value of 65.535 ms.

11.6. Bus Controller (BC) Condition Code Register (Read 0x0037)



Sharing the same register address as the Write-Only General Purpose Flag Register, this 16-bit register is Read-Only. Bit 15 indicates BC run/stop status. With this exception, the upper 8 bits indicate results from the last message processed by the Bus Controller. The lower 8 bits of this register are general purpose flag bits, which may be set, cleared, or toggled by the host using the BC General Purpose Flag Register (see page 33), or by the device by means of the General Purpose Flag Bits (FLG) instruction op code. Further, bits 1-0 can be set or cleared by the device BC logic by execution of two BC instruction op codes: Compare to Frame Timer (CFT) and Compare to Message Timer (CMT).

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>15</td><td>BC RUN</td><td>R</td><td>0</td><td>BC Run / $\overline{\text{Stop}}$

This is a status bit, not a condition code. This bit indicates whether the BC is running or stopped. The bit is set to logic 1 when the BCSTRT bit 13 in the Master Configuration Register is asserted and the BCENA input pin and BCENA bit 12 in the Master Configuration Register 0x0000 are both logic 1.

Once set, this bit resets to logic 0 if the BCENA input pin or BCENA register bit are reset to logic 0 by the host, or if the BC executes the HLT instruction, or if the BC executes an illegal op code. The “illegal op code” case will generate a BCTRAP interrupt, if enabled (page XX).</td></tr>
<tr><td>14
13</td><td>RETRY 1
RETRY 0</td><td>R</td><td>0</td><td>Message Retry Status Bits.

Bits 14-13 indicate the retry status of the most recent message the number of times message was retried:

<table><tr><th>Bit 14:13</th><th>Number of Message Re-tries</th></tr><tr><td>0-0
0-1
1-0
1-1</td><td>0
1
2
not used</td></tr></table></td></tr>
<tr><td>13</td><td>BADMSG</td><td>R</td><td>0</td><td>Bad Message.

This bit is logic 1 to indicate message format error, loopback test failure, or no response error for the last message.</td></tr>
<tr><td>11</td><td>MSTATSET</td><td>R</td><td>0</td><td>Masked Status Set.

This bit is set if one or more of the following conditions occurred during the last message:

• One or more of the Status Mask bits 14-9 are logic 0 in the BC Control Word, and the corresponding bits are logic 1 in the received RT Status Word. When BC Control Word “Reserved Bits Mask” bit 9 is logic 0, this Masked Status Set bit is set if any of the three Reserved bits are set in the received RT Status Word.

• The BCR Mask Enable bit 0 is logic 0 in the BC Configuration Register 0x0032. Opposite logic states occur for the Mask BCR bit in the message BC Control Word and the Broadcast Command Received (BCR) bit in the received RT Status Word.

• The BCR Mask Enable bit 0 is logic 1 in the BC Configuration Register 0x0032. Opposite logic states prevail for the Mask BCR bit in the message BC Control Word and the Broadcast Command Received (BCR) bit in the received RT Status Word.

The table on page 27 shows how the Broadcast Command Received (BCR) bit in the received RT Status Word affects Masked Status Set.</td></tr>
</table>

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Bit No.	Mnemonic	R/W	Reset	Function
10	GDBT	R	0	Good Data Block Transfer. Indicating status for the last transmit-data message, this bit is set to logic 1 after completion of an error-free RT-to-BC transfer, RT-to-RT transfer, or transmit mode command with data. This bit is reset to logic 0 following any message in which error occurs. This bit is always logic 0 after completion of a BC-to-RT transfer, a receive mode command with data, or any mode command without data. This bit can be used to determine when the transmit portion of an RT-to-RT message was error-free: A Block Status Word for an RT-to-RT message having both the Error Flag and Good Data Block Transfer bits set indicates that the transmitting RT responded correctly, but an error was detected in the receiving RT portion of the message. This bit is not affected by the device loop back function.
9	FMTERR	R	0	Format Error. This bit is logic 1 when the received data from the most recent message contains one or more violations of the MIL-STD-1553 message validation criteria, including sync, encoding, parity, bit count or word count errors. This bit is also set if the received Status Word from the responding RT contains incorrect RT address bits 15:10.
8	NORESP	R	0	No Response Error. This bit is set to logic 1 when an RT fails to respond to a command, or responds later then the BC No Response Timeout time. The No Response Timeout delay is programmed using BC Timeout Select bits 15-14 in the BC Configuration Register 0x0032.
7 – 2	GP7 – GP2	R	0	General Purpose Flags 7-2. Interpretation of these flag bits is user defined. These bits are set cleared or toggled by the host, through use of the BC General Purpose Flag Register, or by the BC, through use of the FLG instruction op code.
1	EQ / GP1	R	0	Equal / General Purpose Flag 1. This flag bit is manipulated using the same methods as General Purpose Flags 7-2, or may be set or cleared by two BC instruction op codes, Compare to Frame Time Counter (CFT) or Compare to Message Time Counter (CMT).
0	LT / GP0	R	0	Less Than / General Purpose Flag 0 This flag bit is manipulated using the same methods as General Purpose Flags 7-2, or may be set or cleared by two BC instruction op codes, Compare to Frame Time Counter (CFT) or Compared to Message Time Counter (CMT).

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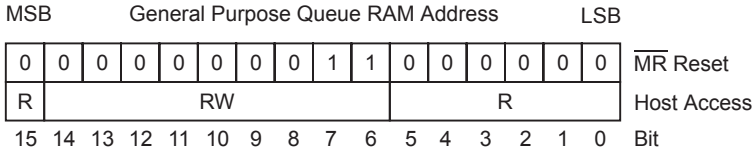
11.7. Bus Controller (BC) General Purpose Flag Register (Write 0x0037)

Sharing the same register address as the Read-Only BC Condition Code Register, this 16-bit register is Write-Only. This register is written by the host to set, clear or toggle any combination of the 8 general-purpose flags 7-0 in the BC Condition Code Register. When this register is written, general-purpose flags are modified. Reading register address 0x0037 returns the value in the BC Condition Code Register, containing the modified GP flag bits (see Section 11.6).

Each general-purpose flag in the BC Condition Code Register is mirrored twice in the General Purpose Flag Register, once in the upper byte and once in the lower byte. Bits asserted in the lower byte set the corresponding GP flag bits in the BC Condition Code Register to 1. Bits asserted in the upper byte clear the corresponding GP flag bits in the BC Condition Code Register to 0. Bits asserted in both the lower and upper bytes for a specific GP flag toggles (inverts) the corresponding GP flag bit in the BC Condition Code Register. When both bits are written to logic 0 state for a specific GP flag bit, no change occurs for that GP flag bit. The FLG instruction op code operates similarly, as shown in the diagram in Figure 4.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15 – 8	CLEAR GP7 – GP2	W	0	Clear General Purpose Flag 7-0. Bits asserted in the upper byte clear the corresponding GP flag bits in the BC Condition Code Register to 0.
7 – 0	SET GP7 – GP2	W	0	Set General Purpose Flag 7-0. Bits asserted in the lower byte set the corresponding GP flag bits in the BC Condition Code Register to 1. Bits asserted in both the lower and upper bytes for GPx toggles that GP flag bit in the BC Condition Code Register.

11.8. Bus Controller (BC) General Purpose Queue Pointer Register (0x0038)



This 16-bit register is a combination of Read-Only and Read-Write bits. This register contains 0x00C0 after $\overline{MR}$ pin master reset. The initialized value represents the base address for the 64-word BC General Purpose Queue. The host can overwrite the default 0x00C0 value, but low order bits 5-0 and bit 15 must equal logic 0 for the initialized value. These bits cannot be set to logic 1 by a host write cycle.

The general purpose queue provides a way for the Bus Controller message sequencer to convey various information to the external host. The BC instruction set includes op codes that push data values onto this queue, including immediate data values, the Block Status Word from the most recent message, the Time Tag Register count, or the contents of a specified memory address.

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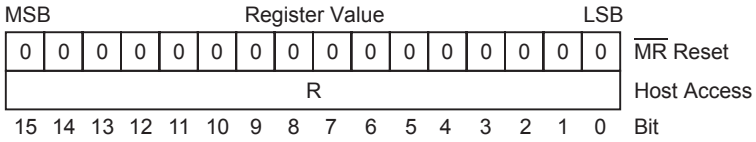
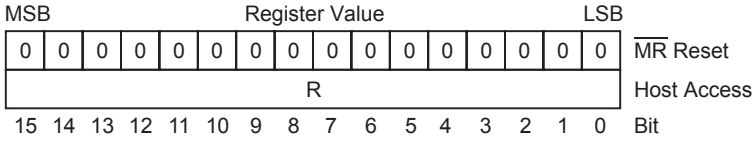
The General Purpose Queue is implemented as a 64-word circular buffer. **This register always points to the next queue address to be written,** the address following the last queue location written by the Bus Controller. This queue pointer rolls over from bits 5:0 = 11111 to 00000, every 64th word written. (Bits 15:6 are static.) If enabled in the BC Interrupt Enable Register, the BCGPQ interrupt will be generated each time queue pointer rollover occurs.

11.9. Bus Controller (BC) Time Tag Counter (0x0043)



11.10. Bus Controller (BC) Time Tag Counter High (0x0044)



These registers are read-only and are cleared after $\overline{MR}$ pin Master Reset. The Bus Controller can be configured for either 16- or 32-bit time base counting in the Time Tag Counter Configuration Register. When configured for 16-bit time base operation, register 0x0043 contains the entire 16-bit count. When configured for 32-bit time base operation, count bits 31-16 reside in register 0x0044 while register 0x0043 contains bits 15-0.

For programmed bus controller action, instruction op codes are provided for loading a time tag count value, or pushing the current time tag count onto the BC General Purpose Queue. If configured for 32-bit time base operation, separate op codes are provided for loading the upper or lower words individually, or pushing the individual words or simultaneously pushing both words onto the BC General Purpose Queue:

Configuration	*Op Code*	*Description*
16-Bit Time Base	LTT	Load Time Tag Count (parameter) into register 0x0043.
	LTH	Not used for 16-bit time base.
	PTT	Push Time Tag Count from register 0x0043 onto BC GP Queue.
	PTH	Not used for 16-bit time base.
	PTB	Not used for 16-bit time base.
32-Bit Time Base	LTT	Load Low Time Tag Count (parameter) into register 0x0043.
	LTH	Load High Time Tag Count (parameter) into register 0x0044.
	PTT	Push Low Time Tag Count from register 0x0043 onto BC GP Queue.
	PTH	Push High Time Tag Count from register 0x0044 onto BC GP Queue.
	PTB	Push Low and High Time Tag Counts from register 0x0043 and 0x0044 onto BC GP Queue (simultaneous 32-bit count capture)

The host can bypass BC Instruction List execution to exercise direct control over the BC Time Tag counter. By writing bits 13-12 in the Time Tag Counter Configuration Register 0x0039, the host can clear time tag count to zero, or load the current value contained in the BC Time Tag Utility Register(s) into the BC Time Tag counter(s). Finally, the BC Time Tag Match Register(s) provide capability for host interrupts when the time tag count reaches any predetermined 16- or 32-bit value.

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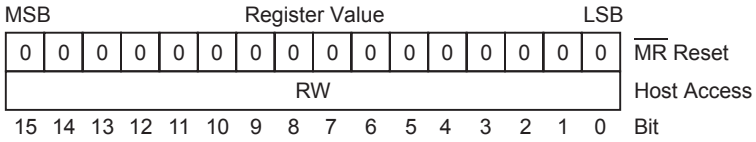
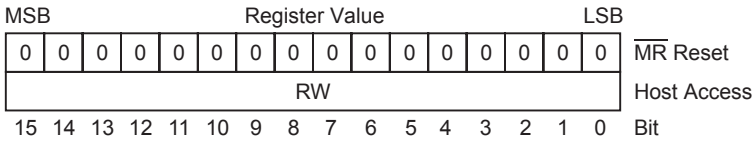
11.11. Bus Controller (BC) Time Tag Utility Register (0x0045)

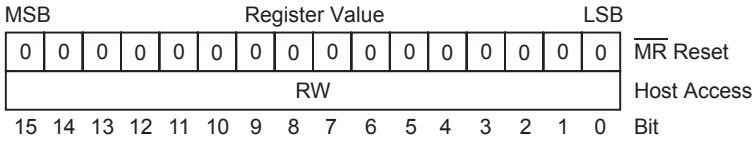


11.12. Bus Controller (BC) Time Tag Utility High Register (0x0046)

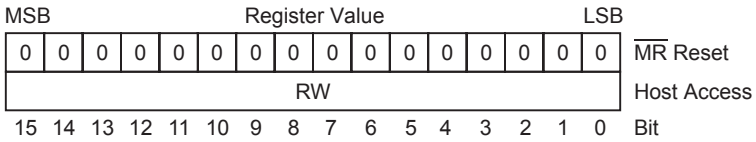


These registers are read-write and are cleared after $\overline{MR}$ pin Master Reset. This utility register pair is used for simultaneously loading a 16- or 32-bit value into the BC Time Tag Counter. When loading, the value contained in utility register 0x003D is copied into BC Time Tag Counter register 0x0043. If the BC is configured for 16-bit time base, register 0x0043 contains the entire 16-bit count. If configured for 32-bit time base operation, count bits 31-16 are simultaneously copied from utility register 0x003E into BC Time Tag Counter register 0x0044. Please refer to the description for bits 13-12 in the “Time Tag Counter Configuration Register (0x0039)” on page 43.

11.13. Bus Controller (BC) Time Tag Match Register (0x0047)



11.14. Bus Controller (BC) Time Tag Match High Register (0x0048)



These registers are read-write and are cleared after $\overline{MR}$ pin Master Reset. When the BCTTM bit 5 is logic 1 in the Hardware Interrupt Enable Register 0x000F, an interrupt occurs when the BC time tag count matches the value stored in this register pair. If the BC is configured for 16-bit time base, match register 0x0045 is compared to time base count register 0x0043 for match determination. If configured for 32-bit time base operation, count bits 31-16 in match register 0x0046 is also compared to BC Time Tag Counter register 0x0044 for match determination. Please refer to the description for BCTTM bit 5 in the Hardware Interrupt Registers in Section 9.5.

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11.15. Bus Controller Interrupt Registers and Their Use

Thirteen HI-613x registers are used for host interrupt management. In addition to the Interrupt Count &Log Address Register described in Section 9.4, there are four 3-register groups, separated by function. One register group is for Hardware interrupts, plus one register group each for Bus Controller, Bus Monitor and Remote Terminal interrupts. The Remote Terminal register set is shared between RT1 and RT2. Each group (BC, MT, RT or Hardware) has

- An Interrupt Enable Register to enable and disable interrupts
- A Pending Interrupt Register to capture the occurrence of enabled interrupts
- An Interrupt Output Enable Register to enable $\overline{IRQ}$ output to host, for pending enabled interrupts

Each individual bit in all three registers is mapped to the same interrupt-causing event when the corresponding interrupt condition is enabled. Numerous interrupt options are available for the BC. At initialization, bits must be set in the BC Interrupt Enable register to identify the interrupt-causing events for the BC which are heeded by the HI-613x. Most Bus Controller applications only use a subset of available BC interrupt options. Interrupt-causing events are ignored when their corresponding bits are reset in the BC Interrupt Enable Register. Setting an Interrupt Enable register bit from 0 to 1 does not trigger interrupt recognition for events that occurred while the bit was zero.

Whenever an enabled monitor interrupt event occurs, the Interrupt Log Buffer is updated and a bit is set in the BC Pending Interrupt Register. This action takes place only when the corresponding bit is already set in the BC Interrupt Enable Register. The host can poll the BC Pending Interrupt Register to detect the occurrence of Monitor interrupts, indicated by non-zero value. When the host reads the BC Pending Interrupt Register, it automatically clears to 0x0000.

When an enabled interrupt condition occurs and the corresponding bit is also set in the BC Interrupt Output Enable Register, the $\overline{IRQ}$ output is asserted to alert the host. Thus, the BC Interrupt Output Enable Register establishes two interrupt priority levels for the Monitor: high priority interrupts generate an $\overline{IRQ}$ signal output, while low priority interrupts do not. The host detects low priority interrupts by polling the BC Pending Interrupt Register.

A single $\overline{IRQ}$ host interrupt output signal is shared by all enabled interrupt conditions having bits set in the four Interrupt Output Enable registers. Multiple interrupt-causing events can occur simultaneously, so each $\overline{IRQ}$ output assertion can result from one or several interrupt conditions.

When the host receives an $\overline{IRQ}$ signal from the device, it must identify the event (or events) that triggered the interrupt. A hardware-assisted interrupt-decoding scheme simplifies interrupt identification. This scheme uses the three low order bits in the Hardware Pending Interrupt Register.

Upon $\overline{IRQ}$ interrupt assertion, the host first reads the Hardware Pending Interrupt Register. Bits 15-3 in this register identify hardware interrupt conditions. The three low-order bits the Hardware Pending Interrupt Register indicate zero vs. non-zero status for the RT, MT and BC Pending Interrupt Registers. If any of these bits is logic 1, the corresponding Pending Interrupt Register has one or more interrupt flags of set. Any combination of these 3 bits may be set. Each of the four Pending Interrupt registers self-resets to 0x0000 after the host reads its value. Thus, the host should retain the value read from the Hardware Pending Interrupt Register when 2 or more bits are non-zero in the bit 2-0 range.

When BCIP (BC Interrupt Pending) bit 0 is set in the Hardware Pending Interrupt Register, the BC Pending Interrupt Register contains a nonzero value, so should be read next to identify the specific BC interrupt event.

When polling the Pending Interrupt registers to identify low priority interrupts that do not assert the $\overline{IRQ}$ output, the same method can be applied. At a single read of the Hardware Pending Interrupt Register reveals zero / non-zero status of all four Pending Interrupt registers.

To help the host process interrupts, the HI-613x device maintains information from the 32 most recent interrupts in a 64-word ring buffer in RAM, located at the fixed address range 0x0180 to 0x01BF. Each interrupt stores two information words: the Interrupt Identification Word (IIW) identifies the interrupt type(s) that occurred; the Interrupt Address Word (IAW) identifies the interrupt source. For Bus Controller interrupts, the IAW contains a 16-bit Control/Status Block address, pointing to the Block Status Word of the message in which the interrupt occurred.

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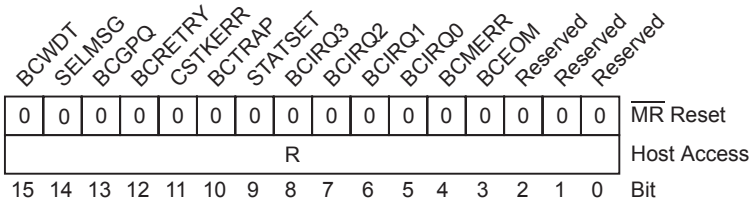
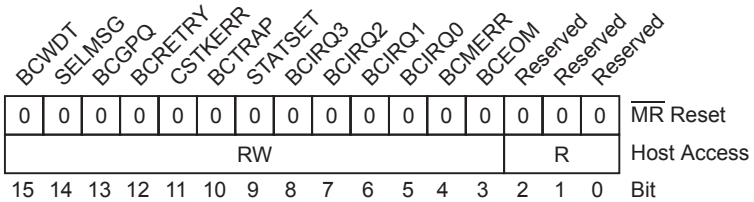
11.15.1. Bus Controller (BC) Interrupt Enable Register (0x0010)

11.15.2. Bus Controller (BC) Pending Interrupt Register (0x0007)



11.15.3. Bus Controller (BC) Interrupt Output Enable Register (0x0014)



Three registers govern BC interrupt behavior: the BC Interrupt Enable Register, the BC Pending Interrupt Register and the BC Interrupt Output Enable Register. When a bit is set in the BC Interrupt Enable Register, the corresponding BC interrupt is enabled. When a bit is reset in this register, the corresponding interrupt event is unconditionally disregarded. Setting a register bit from 0 to 1 does not trigger interrupt recognition for events that occurred while the bit was zero.

When an enabled BC interrupt event occurs, the corresponding bit is set in the BC Pending Interrupt Register and the Interrupt Log Buffer is updated. To simplify interrupt decoding, BCIP bit 0 in the Hardware Pending Interrupt Register is also set whenever a message sets at least one bit in the BC Pending Interrupt Register.

If the corresponding bit is set in the BC Interrupt Output Enable Register, the $\overline{\text{IRQ}}$ output is asserted at message completion. The BC Interrupt Output Enable Register establishes two priority levels: high priority interrupts generate an nIRQ output while low priority interrupts do not. Both priority levels update the Pending Interrupt Register and Interrupt Log Buffer. The host can detect low priority (masked) interrupts by polling Pending Interrupt registers.

The table below first describes the common bits 15-3 in all three BC interrupt registers and then describes register-to-register differences for bits 2-0.

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Bit No.	*Mnemonic*	*Function*
15	BCWDT	BC Watchdog Timer Interrupt. The BC Frame Timer expired.
14	SELMSG	BC Selected Message Interrupt. The completion of a MIL-STD-1553 message that has bit 4 set (EOM) in the message block Control Word.
13	BCGPQ	BC General Purpose Queue Rollover Interrupt. The 64-word circular BC General Purpose Queue Pointer rolled over to its base address value.
12	BCRETRY	BC Retry Interrupt. The occurrence of a retried message by the BC. If enabled, the interrupt will occur after the last enabled message retry (one or two) regardless of the outcome, successful or unsuccessful.
11	CSTKERR	BC Call Stack Pointer Error Interrupt. The BC subroutine stack depth was violated due to an overflow or underflow condition. Call stack level is incremented each time a BC “subroutine call” op code (CAL) is executed. Call stack level is decremented each time a BC “subroutine return” op code (RTN) is executed. The allowed range for the call stack level is 0-7. An interrupt occurs when a CAL op code executes when stack level is 7, An interrupt also occurs when a RTN op code executes when stack level is 0.
10	BCTRAP	BC Trap Interrupt. Two conditions can assert this interrupt: The BC fetched an illegal op code. The BC operation stops when the current 1553 message is complete. An illegal op code is either undefined, fails parity check, and/or has the wrong value for bits 9-5. When this occurs, BCRUN bit 15 resets to logic 0 in the BC Condition Code and GP Flag register 0x0037. When the CHKFMT bit 13 is set in the BC Configuration Register, the BC Control Word message format bits 2-0 (mode command, RT-RT and broadcast message flags) are compared to the stored value(s) for the message Command Word(s) following the Control Word in the Message Block. When mismatch occurs between Control Word format bits and Command Word(s), the BCTRAP interrupt is asserted, if enabled. BC instruction list execution continues, so this condition can be differentiated from illegal op code because BCRUN bit 15 remains high in the BC Condition Code and GP Flag register, 0x0037. For mode command or broadcast mismatch, the stored message block Command Word(s) are transmitted. For RT-RT format mismatch, RT-RT bit 1 in the Control Word has priority, determining whether the message block is treated as an 8- or 16-word entity. For RT-RT format mismatch, **message failure is likely for this message or the next message block**, since the message block boundary is misplaced. The CHKFMT option bit detects BC programming problems in the development phase. The option is normally disabled in the field.

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Bit No.	*Mnemonic*	*Function*
9	STATSET	BC Status Set Interrupt. The BC received an RT Status Word containing the wrong RT address field, or having an unexpected bit value for at least one of the eight non-reserved status bits. The expected value for these bits (excluding the BCR bit) is usually 0. The BCR (broadcast command received) bit can have an expected value of 1 when BCR Mask Enable bit in the BC Configuration Register is logic 0. In this case, the Mask Broadcast bit in the message block Control Word shows the expected value of the Status Word BCR bit. If the Control Word's Mask Broadcast bit is logic 1, the expected value of BCR in the RT Status Word is logic 1.
8 − 5	BCIRQ3:0	BC Interrupt Request Bits 3-0. When this 4-bit field is nonzero, the BC executed an IRQ op code. The value of bits 8:5 will equal the value of the 4 LSBs in the parameter associated with the IRQ op code. The user may define the 4- bit pattern to suit application requirements.
4	BCMERR	BC Message Error Interrupt. A non-broadcast message ended with RT Status Word containing the ME Message Error status bit set.
3	BCEOM	BC End of Message Interrupt. The successful completion of a message, regardless of validity.
For the BC Interrupt Enable Register and the BC Interrupt Output Enable Register only		
2 − 0	Reserved	Bits 2-0 cannot be written, and read back 000.
2 − 1	Reserved	Bits 2-1 cannot be written, and read back 00.
0	BCIP	BC Interrupt Pending. This bit is set when one or more additional bits are set in the bit range 15-3.

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12. SIMPLE MONITOR TERMINAL (SMT)

The HI-613x can operate as an autonomous MIL-STD-1553 Bus Monitor, requiring minimal host support. Two fundamentally different monitor modes are offered. Each of these modes has a separate data sheet section describing registers used and operational details. Information regarding the alternative IRIG-106 Monitor Terminal (IMT) begins in Section 14.

12.1. Overview

Simple Monitor Terminal (SMT) Mode has its own dedicated Time Tag counter, and can use either a 16- or 48-bit Time Tag scheme. The SMT monitor utilizes two stacks in RAM: a Command Stack and a Data Stack. Each recorded MIL-STD-1553 message appends a fixed length entry into the Command Stack and a variable length entry into the Data Stack.

The SMT message records a fixed length “message block” In the Command Stack for each MIL-STD-1553 message. The advantage of fixed length Command Stack message blocks is that the host can quickly jump to the block start address for any message.

The number of words added to the Data Stack for each message depends on the MIL-STD-1553 message type, ranging from zero (broadcast mode command without data) to 35 words (for a 32 data word RT-RT command).

In SMT mode, both stacks are fully utilized for recording message data. Unlike IMT mode, there is no option for generating a data header or data trailer. SMT monitor mode allows selective monitoring of MIL-STD-1553 messages, based on the address, subaddress and T/$\overline{R}$ status in each monitored Command Word, or can monitor all messages, when preferred. The SMT monitor offers flexible interrupt options.

In Master Configuration Register 0x0000, MTENA bit 8 is logically ANDed with the MTENA input pin to enable the SMT monitor. If the MTENA input pin or Master Configuration Register bit 8 equals logic 0, Bus Monitor operation is disabled. When the pin and Master Configuration Register MTENA bit 8 are both logic 1, the Bus Monitor is enabled. Operation commences when the receiver first decodes MIL-STD-1553 activity meeting the “start record” criteria selected by bits 6-5 in the MT Configuration Register 0x0029. If monitor operation is underway when Master Configuration Register MTENA bit 8 or MTENA input pin becomes logic 0, monitor operation stops after completion of any message already underway.

The HI-613x is configured for SMT operation by writing bits 1-0 in the MT Configuration Register 0x0029.

When MT Configuration Register bits 1-0 equal 11, the SMT operates with 16-bit Time Tag resolution and each recorded MIL-STD-1553 message adds a four word entry in the Command Stack. This is summarized in Table 8.

Table 8. Command Stack Message Block for SMT Monitor using 16-bit Time Tag

Message Word Block	***Word Name***	***Word Function when using 16-bit time tag***
Word 3	Message Command Word	Message Command Word. The MIL-STD-1553 Command Word that initiated the message. For an RT-RT message, Receive Command Word 1 is stored here; Transmit Command Word 2 is the first stored word in the Message Data Block.
Word 2	Data Block Pointer	Starting address in the Data Stack for the corresponding message data block.

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Message Word Block	*Word Name*	*Word Function when using 16-bit time tag*
Word 1	Message Time Stamp Bits 15 ~ 0	Sixteen bit message time stamp. Word 0 is the first word in the Command Stack entry for each message.
Word 0	Block Status Word	Message Block Status Word, defined in Section 12.2. Word 0 is the first word in the Command Stack entry for each message.

When MT Configuration Register bits 1-0 equal 01, the Simple Message Monitor operates with 48-bit Time Tag resolution. Each MIL-STD-1553 message adds an 8-word entry in the Command Stack. This is summarized in Table 9. The expanded message block accommodates two additional Time Tag words, a Message Length word and a Response Time word not found when using 16-bit Time tag resolution.

Table 9. Command Stack Message Block for SMT Monitor using 48-bit Time Tag

Message Word Block	*Word Name*	*Word Function when using 16-bit time tag*
Word 7	Message Command Word	Message Command Word. The MIL-STD-1553 Command Word that initiated the message. For an RT-RT message, Receive Command Word 1 is stored here; Transmit Command Word 2 is the first stored word in the Message Data Block.
Word 6	Data Block Pointer	Starting address in the Data Stack for the corresponding message data block.
Word 5	Message Length Word (bytes)	The Message Length Word indicates the number of bytes stored in the Message Data Block. The range is 0 to 72 bytes, corresponding to 0 to 36 16-bit words stored.
Word 4	Response Time Word	The Response Time Word contains two 8-bit fields: • Bits 15 ~ 8 contains GAP2 • Bits 7 ~ 0 contains GAP1 All GAP values are measured from mid-parity zero crossing of the preceding word, to the mid-sync zero crossing of the Status Word (the gap “dead time” interval plus 2 µs). Time resolution is 100 ns per LSB, so the maximum indicated gap time for GAP1 or GAP2 is 25.5 µs. For RT-RT messages, the GAP1 byte indicates transmit RT response time, and the GAP2 byte indicates received RT response time. For all other messages, the GAP1 byte indicates the only RT response time, and the GAP2 byte reads 0x00.
Word 3	Block Status Word	Message Block Status Word, defined in Section 12.2.

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Message Word Block	*Word Name*	*Word Function when using 16-bit time tag*
Word 2	Message Time Stamp Bits 47 ~ 32	Upper 16-bit word of message 48-bit time stamp.
Word 1	Message Time Stamp Bits 31 ~ 16	Middle 16-bit word of message 48-bit time stamp.
Word 0	Message Time Stamp Bits 15 ~ 0	Lower 16-bit word of message 48-bit time stamp. Word 0 is the first word in the Command Stack entry for each message.

The Command Stack address range is bounded by the values in Address List Words 0 and 2. The Data Stack address range is bounded by the values in Address List Words 4 and 6. The “Next Address” Words 1 and 5 must be initialized by the host for the first data written after reset; thereafter these values are maintained by the device each time a new MIL-STD-1553 message is recorded.

Two optional stack address interrupts are offered. When enabled, a Command or Data Stack Address Interrupt occurs whenever the matching RAM address in the Stack is written. The Address List contains the address values for these optional “stack utilization” interrupts.

For SMT mode, the 8-word Monitor Address List is defined in Table 10.

Table 10. Monitor Address List for SMT Mode

Message Word Block	*Word Name*	*Word Function when using 16-bit time tag*
Word 7	Data Stack Interrupt Address	Host initialized with a RAM address value if this interrupt is enabled. If enabled, an interrupt occurs when the matching RAM address is written. Address must occur within the range bounded by Words 4 and 6.
Word 6	Data Stack End Address	Host initialized, defines SMT Data Stack upper address boundary.
Word 5	Data Stack Next Address	**Must be host initialized**, usually to match SMT Data Stack Start Address. **Updated by device** each time a new MIL-STD-1553 message is recorded. This value advances through the address range in circular buffer fashion.
Word 4	Data Stack Start Address	Host initialized, defines SMT Data Stack lower address boundary.
Word 3	Command Stack Interrupt Address	Host initialized with a RAM address value if this interrupt is enabled. If enabled, an interrupt occurs when the matching RAM address is written. Address must occur within the range bounded by Words 0 and 2.

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Message Word Block	*Word Name*	*Word Function when using 16-bit time tag*
Word 2	Command Stack End Address	Host initialized, defines SMT Command Stack upper address boundary.
Word 1	Command Stack Next Address	**Must be host initialized**, usually to match Command Stack Start Address. **Updated by device** each time a new MIL-STD-1553 message is recorded. This value advances through the address range in circular buffer fashion.
Word 0	Command Stack Start Address	Host initialized, defines SMT Command Stack lower address boundary. Word 0 occurs at the Address List base address in register 0x002F.

For each monitored MIL-STD-1553 command, the written Command Stack entry is fixed at 4 or 8 words, depending on selected Time Tag resolution. Depending on MIL-STD-1553 message type, the written Data Stack entry varies in length, ranging from zero words (for broadcast mode code commands without data) to 35 words (for an RT-to-RT message with 32 data words). Simple Monitor Terminal Data Storage is summarized in Figure 6.

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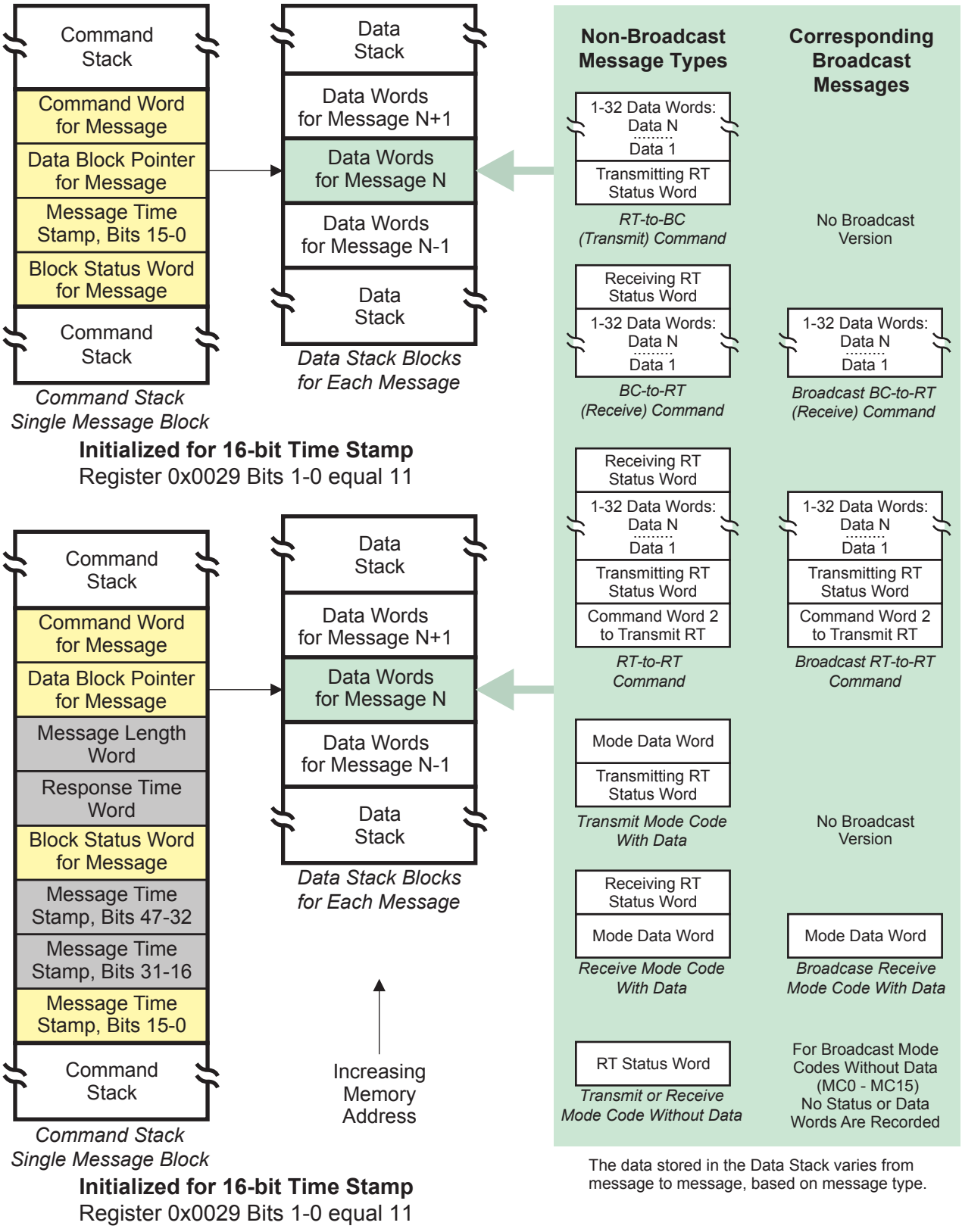

Figure 6. Simple Monitor Terminal (SMT) Data Storage

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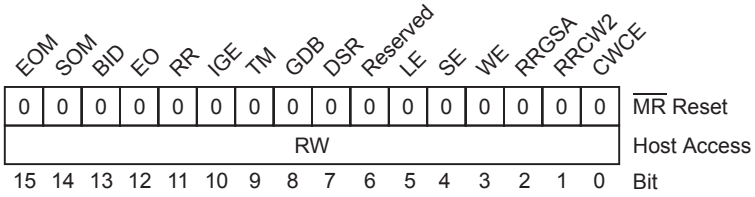
12.2. SMT Block Status Word (BSW) Description

The SMT bus monitor stores a Block Status Word in the Command Stack for each monitored MIL-STD-1553 message. This word provides information regarding message status, the bus on which the message occurred, whether errors occurred during the message, and the type of occurring errors. The Block Status Word for SMT mode is defined as follows:



SMT Block Status Word
with Extended Status Bits Enabled
(Not IRIG-106 Chapter 10 Compliant)

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	EOM	R/W	0	End of Message. Bit 15 is set upon completion of a monitored message, whether or not errors occurred. When EOM is set, SOM bit 14 is concurrently reset.
14	SOM	R/W	0	Start of Message. Bit 14 is set to logic 1 approximately 3-4 µs after completion of a valid Command Word, and is reset to logic 0 at the end of the message. If the monitor uses message filtering, SOM is only set for monitored messages.
13	BID	R/W	0	Bus ID (Bus B / $\overline{\text{Bus A}}$). Bit 13 indicates the bus ID for the message. This bit is logic 0 for a message occurring on Bus A. This bit is logic 1 for a message occurring on Bus B.

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Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
12	EO	R/W	0	Error Occurred Flag. This bit indicates a message error was encountered. This bit is set when one or more of the following conditions are true (logical-OR): • an unfinished message is superseded by another valid command • Bit 10 Illegal Gap Error is set • Bit 9 Response Timeout is set • Bit 5 Length (Word Count) Error is set • Bit 4 Sync Type Error is set • Bit 3 Invalid Word Error is set • Bit 2 RT-RT Gap / Sync / Address Error is set • Bit 1 RT-RT Command Word 2 Error is set (except as noted) • Bit 0 Command Word Content Error is set (except as noted) There are three exceptions where register bit 0 or 1 is set without affecting bit 12 state: **Bit 1 RT-RT Command Word 2 Errors that do not assert bit 12** • RT-RT Transmit Command Word 2 subaddress field equals 00000 or 11111 (mode code command indicated) • RT-RT Transmit Command Word 2 has the same RT Address as Receive Command Word 1 **Bit 0 Command Word Content Error that does not assert bit 12** • Undefined receive mode code 0~15 decimal.
11	RR	R/W	0	RT-to-RT Transfer When logic 1, bit 11 indicates an RT-to-RT message, beginning with two contiguous Command Words.
10	IGE	R/W	0	Illegal Gap Error When logic 1, bit 10 indicates an illegal gap occurred on the bus, other than Response Timeout.
9	TM	R/W	0	Response Timeout When logic 1, bit 9 indicates a response timeout occurred. This bit is set if an RT Status Word associated with this message failed to arrive within the response time interval specified by bits 15-14 in the MT Configuration Register 0x0029.
8	GDB	R/W	0	Good Data Block Transfer Bit 8 is set to logic 1 following completion of a valid, error-free message. This bit is reset to logic 0 following completion of a message in which error occurred. If an RT responds to a transmit command with Busy status and does not transmit the commanded data words, this is not considered a message error that causes GDB reset.

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Bit No.	Mnemonic	R/W	Reset	Function
7	DSR	R/W	0	Data Stack Rollover Bit 7 is logic 1 to indicate that this message overran the monitor Data Stack, causing the stack pointer to roll over to the base address.
6	SFS	R/W	0	Status Flag Set Bit 6 is logic 1 when a status bit was set in an RT Status Word response.
5	LE	R/W	0	Word Count (Length) Error Bit 5 indicates that the number of data words transmitted by the BC or RT differs from the Word Count specified in the Command Word. An RT Status Word with the Busy bit set will not cause Word Count Error. A transmit command with Response Timeout will not cause Word Count Error.
4	SE	R/W	0	Sync Type Error Bit 4 is logic 1 to indicate that a BC transmitted data sync with a Command Word, or a command / status sync occurred with Data Word, or an RT responded with data sync in its Status Word and/or command/ status sync in a Data Word.
3	WE	R/W	0	Invalid Word Error (WE) Bit 3 is logic 1 indicate on invalid word error occurred. This includes Manchester decoding errors in the sync pattern or word bits, or the wrong number of bits in the word, or parity error.
2	RRGSA	R/W	0	RT-to-RT Gap/Sync/Address Error (RRGSA) Bit 2 is logic 1 if one or more of the following RT-RT message conditions occur: • MT Gap Check is enabled (bit 12 equals 1 in register 0x0029) and an RT Status Word is received having a response time less than 4µs, per MIL-STD-1553B (mid-parity to mid-sync). In other words, the bus “dead time” was less than 2µs. • One of the RTs responds with an invalid Status Word, having a sync error, a Manchester encoding error, bit count error and/or parity error • One of the RT Status Words contains an RT Address that differs from the RT Address in the corresponding Command Word.
1	RRCW2	R/W	0	RT-to-RT Command Word 2 Error (RRCW2) Bit 1 is logic 1 if an RT-to-RT message occurs (two contiguous Command Words) with one or more of the following illogical conditions: • Transmit Command Word 2 T/$\overline{R}$ bit equals 0 (receive) • Transmit Command Word 2 subaddress field equals 00000 or 11111 (mode command indicated) • Transmit Command Word 2 has the same RT Address as Receive Command Word 1 • Transmit Command Word 2 has sync error

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Bit No.	Mnemonic	R/W	Reset	Function
0	CWCE	R/W	0	Command Word Content Error (CWCE) Bit 0 is logic 1 if a received Command Word violates one or more MIL-STD-1553B requirements: • A non-mode broadcast transmit Command Word occurred. (non-mode has 5-bit subaddress field equal to decimal 1~30) • A receive mode code Command Word was received with mode code in the range of 0~15 decimal (undefined) • A broadcast transmit mode code command occurred having a mode code value for which broadcast is not allowed (mode code = decimal 0, 2, 16, 18 or 19)

12.3. SMT Message Filter Table

The Simple Monitor Terminal can select messages for monitoring through the use of a 128-word MT Filter Table, located at fixed RAM address 0x0100. When the table bit corresponding to a new message Command Word is logic 1, that message is ignored by the monitor. If the table bit is logic 0, that message is recorded.

After $\overline{MR}$ master reset, 100% of MIL-STD-1553 messages are monitored, since the entire table address range 0x0100 through 0x017F inclusive is 0x0000. The result is that every valid Command Word, received on an idle bus, marks the start of a new MIL-STD-1553 message recorded by the monitor. The Message Filter Table is addressed using three fields in the received Command Word: the 5-bit RT Address field, the T/$\overline{R}$ Transmit/Receive bit, and the MSB of the 5-bit Subaddress field. This is illustrated in Figure 7.

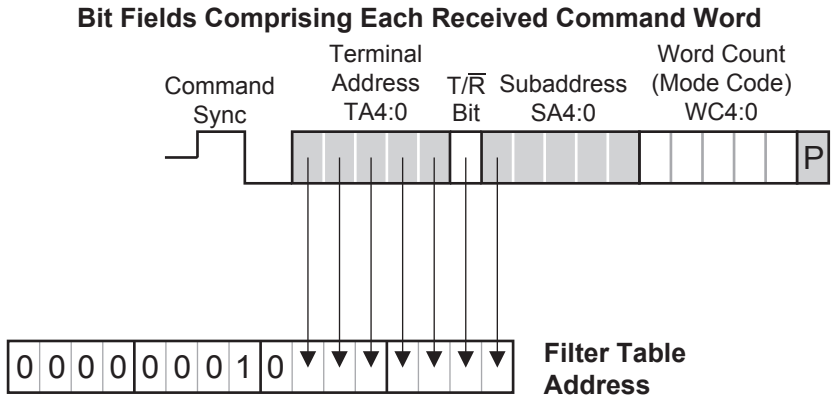

Figure 7. Deriving the Monitor Filter Table Address from the Received Command Word

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Each RT Address from 0 to 31 decimal has four 16-bit table words: two words enable/disable individual Receive Subaddresses, two more words enable/disable individual Transmit Subaddresses. The first four table words apply to Subaddress 0 and are illustrated in Table 11. This 4-word pattern repeats for all 32 Subaddresses, 0-31 decimal.

Table 11. SMT Message Filter Table (RT Address 0 example)

A subaddress message is monitored when the corresponding word bit equals logic 0. The message is not monitored when the bit equals 1.																
Table address 0x0103								**RT Address 0, Transmit Subaddresses 31 to 16**								
Word Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Transmit SA	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Table address 0x0102								**RT Address 0, Receive Subaddresses 31 to 16**								
Word Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Transmit SA	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Table address 0x0101								**RT Address 0, Transmit Subaddresses 15 to 0**								
Word Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Transmit SA	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Table address 0x0100								**RT Address 0, Receive Subaddresses 15 to 0**								
Word Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Transmit SA	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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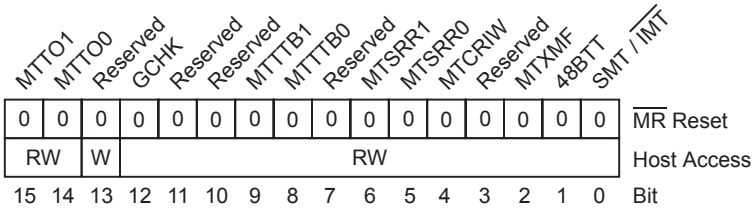
13. SIMPLE MONITOR TERMINAL (SMT) REGISTER DESCRIPTION

In addition to the registers described here, a HI-6131 SMT Bus Monitor also utilizes one or more Memory Address Pointer registers (described in Section 9.8) for managing SPI read/write operations. This comment does not apply for parallel bus interface HI-6130 designs.

13.1. SMT Configuration Register (0x0029)



Bit No.	Mnemonic	R/W	Reset	Function
15 − 14	MTTO1:0	R/W	0	MT Time Out Select. This 2-bit field selects the Monitor “no response” time-out delay from four available selections. Excluding RT-RT commands, the delay is measured from command word mid-parity bit to status word mid-sync.

Bit 15:14	***Bus Dead Time***	***Time Out (excludes RT-RT)***	***RT-RT Time Out***
00	16µs	18µs	61µs
01	21µs	23µs	66µs
10	80µs	82µs	122µs
11	138µs	140µs	180µs

For RT-RT commands, time out delay is measured per Figure 8 in the RT Validation Test Plan, SAE AS4111. That is, from mid-parity of the receive command to mid-sync of the first received data word. This adds 40µs for the embedded transmit command word and transmit-RT status word within this interval.

13	Reserved	W	0	Bit 13 is not used by the bus monitor operating in SMT mode. Initialize this bit to logic 0.
12	GCHK	R/W	0	Gap Check. When this bit equals 1, the monitor evaluates inter-message gaps and RT response times for a minimum preceding bus dead time of 2 µs. This dead time corresponds to an inter-message gap of 4µs, measured per MIL-STD-1553, from mid-parity zero crossing of the preceding word, to mid-sync zero crossing of the following word. A minimum gap time violation results in a Format Error in the Block Status Word for the message. When this bit equals 0 (recommended), the monitor does not check for short inter-message gap times.
11 − 10	Reserved	R/W	0	Bits 11-10 are not used by the bus monitor operating in SMT mode. Initialize these bits to logic 0.

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td rowspan="6">9 − 8</td><td rowspan="6">MTTTB1:0</td><td rowspan="6">R/W</td><td rowspan="6">0</td><td>Monitor Time Tag Message Bit Select.
This 2-bit field selects the bit within the MIL-STD-1553 message where time stamp occurs. Time stamp occurs at mid-bit transition:</td></tr>
<tr><td><table>
<tr><th>Bit 9:8</th><th>Time Tag Event</th></tr>
<tr><td>00</td><td>Last Bit of Last Word in Message</td></tr>
<tr><td>01</td><td>First Bit of First (Command) Word in Message</td></tr>
<tr><td>10</td><td>Last Bit of First (Command) Word in Message</td></tr>
<tr><td>11</td><td>time tag disabled, stores time tag = 0</td></tr>
</table></td></tr>
<tr><td>For options 00 and 10, the “Last Bit” precedes the word’s parity bit. For option 01, the “First Bit” occurs 0.5µs after command sync. While “First Word” generally denotes a command word, message recording can begin with a data word when register bit 5 equals 1.</td></tr>
<tr><td>7</td><td>Reserved</td><td>R/W</td><td>0</td><td>Bit 7 is not used by the bus monitor operating in SMT mode.
Initialize this bit to logic 0.</td></tr>
</table>

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Bit No.	Mnemonic	R/W	Reset	Function
6 – 5	MTSRR1:0	R/W	0	MT Start-Record Requirement 1:0. When register bits 6-5 equal 00, the MT starts recording a new MIL-STD-1553 message when a **properly encoded, complete MIL-STD-1553 word with command sync** is decoded: The command sync is followed by 16 properly encoded data bits plus a 17th parity bit expressing odd parity. No data is recorded until this condition is met. This is the usual setting. (default setting) When register bits 6-5 equal 01, the MT starts recording a new MIL-STD-1553 message when a **properly encoded, complete MIL-STD-1553 word with command sync or data sync** is decoded. The properly encoded command sync (or data sync) is followed by 16 properly encoded data bits plus a 17th parity bit expressing odd parity. If recording begins with data sync, the Sync Error flag will be set in the Block Status Word. When register bits 6-5 equal 10, the MT starts recording a new MIL-STD-1553 message upon detection of a **properly encoded command sync with two contiguous data bits**. If the properly encoded command sync with two contiguous data bits does not result in a valid command word, the Invalid Word Error is set in the Block Status Word. This selection begins recording for complete MIL-STD-1553 command words as well as for command word fragments, or command words with bad parity. Under some circumstances, this record option might be helpful for debugging MIL-STD-1553 communication failure. When register bits 6-5 equal 11, the MT starts recording new bus activity upon detection of **any properly encoded sync (command or data) with two contiguous data bits**. This selection begins recording for complete MIL-STD-1553 command or data words as well as for word fragments, or words with bad parity. If the properly encoded sync with two contiguous data bits does not result in a valid Manchester II word, the Invalid Word Error is set in the Block Status Word. If recording begins with data sync, the Sync Error flag will be set in the Block Status Word. Under some circumstances, this record option might be helpful for debugging MIL-STD-1553 communication failure.
4	MTCRIW	R/W	0	MT Continue Recording After Invalid Word. When bit 4 equals 0, the MT stops recording an incomplete message when an invalid MIL-STD-1553 word is decoded. The invalid word is not stored, and the MT awaits word detection per register bits 6-5 before the next MIL-STD-1553 message is recorded. (default) When bit 4 equals 1, the MT continues recording an incomplete message when an invalid MIL-STD-1553 word is decoded. The invalid word is stored and the MT continues monitoring the message until completion or time-out occurs.
3	Reserved	R/W	0	Bit 3 is not used by the bus monitor operating in SMT mode. Initialize this bit to logic 0.

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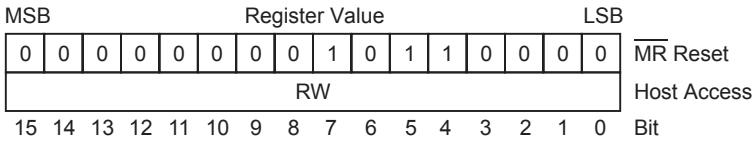
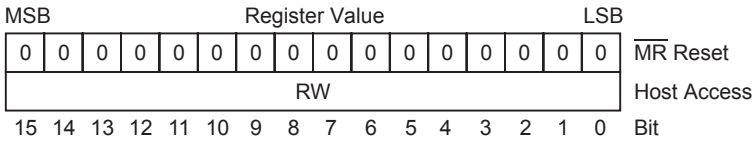
Bit No.	Mnemonic	R/W	Reset	Function
2	MTXMF	R/W	0	Extended Message Flag Enable. Usually register bit 2 is set to logic 1 to enable expanded status/error flags, occupying the “reserved” bit positions in the IRIG-106 Block Status Word. When register bit 2 equals 0, the recorded status/error flags are limited to the defined bits in the IRIG-106 Block Status Word. This is described in Section XX.
1	48BTT	R/W	0	48-Bit Time Tag / $\overline{\text{16-Bit Time Tag}}$ When register bit 1 equals 0, the SMT time tag counter operates with 16-bit resolution and the recorded entry for each MIL-STD-1553 message in the Command Stack is four 16-bit words. When register bit 1 equals 1, the SMT time tag counter operates with 48-bit resolution. To record the 48-bit time count, the entry for each MIL-STD-1553 message in the Command Stack is eight 16-bit words. Two of the words added are used for Response Time and Message Length words. See Section 13.5.
0	SMT / $\overline{\text{IMT}}$	R/W	0	Select Simple Monitor Terminal (SMT) or IRIG-106 Monitor Terminal (IMT). For SMT operation, this register bit must be logic 1.

13.2. SMT Bus Monitor Address List Start Address Register (0x002F)



This 16-bit register is Read-Write and is fully maintained by the host. After $\overline{\text{MR}}$ pin master reset, this register is initialized with 0x00B0, the default base address of the MT Address Table in device RAM. The host can overwrite the default base address. This register is not affected by MT soft reset, when the MTRESET bit is asserted in the Master Status and Reset Register, 0x0001. The Address List for SMT mode is explained in **Section XX**.

13.3. SMT Last Message Command Stack Pointer (0x0031)



This 16-bit register is read-only and is updated by the MT upon completion of a monitored MIL-STD-1553 message. This register is cleared after $\overline{\text{MR}}$ pin master reset or by MT soft reset, when the MTRESET bit is asserted in the Master Status and Reset Register, 0x0001.

This register contains the RAM address for the first word stored in the Command Stack for the last completed MIL-STD-1553 message.

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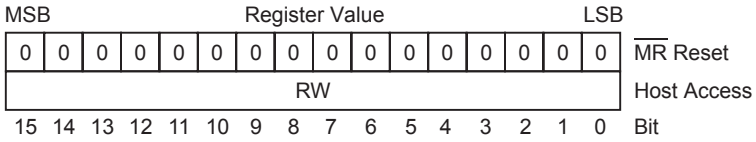
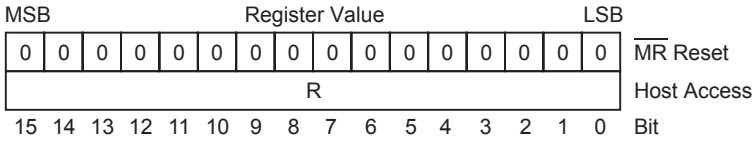
13.4. SMT Next Message Command Stack Pointer (0x0030)



This 16-bit register is read-only and is updated by the MT upon completion of a monitored MIL-STD-1553 message. This register is cleared after $\overline{MR}$ pin master reset or by MT soft reset, when the MTRESET bit is asserted in the Master Status and Reset Register, 0x0001. This register contains the address for the first word to be stored in MT Command Stack, for the next MIL-STD-1553 message. It mirrors the value contained in the MT Stack 1 Current Address Pointer, which is Word 1 in the MT Address List.

The MT logic only updates this “next message address” register after message completion. Therefore, after reset or after the host has changed the MT Address List Start Address Register 0x002F, this register does not contain a pointer address until processing for the next message is completed. If the read value equals zero, the “next message address” is the Command Stack starting address.

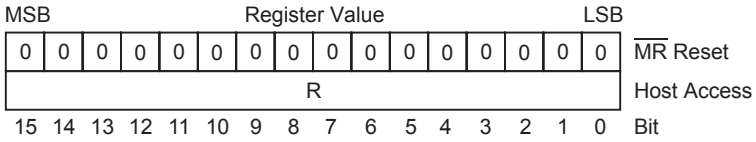
13.5. SMT Bus Monitor Time Tag Count Register (0x003A)



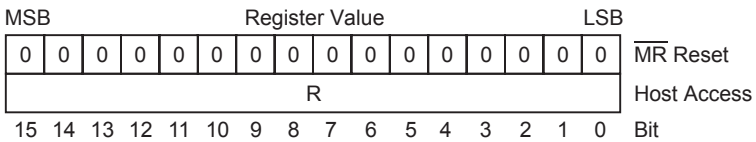
When MT Configuration Register bits 1-0 equal 11, the Simple Message Monitor operates with 16-bit Time Tag resolution and register 0x003A contains the full 16-bit Time Tag count.

When MT Configuration Register bits 1-0 equal 01, the Simple Message Monitor operates with 48-bit Time Tag resolution and the full Time Tag Count requires the above register plus two additional registers:

13.6. SMT Bus Monitor Time Tag Count Mid Register (0x003B)



13.7. SMT Bus Monitor Time Tag Count High Register (0x003C)



When configured for 48-bit time base operation, count bits 47-17 reside in register 0x003C, count bits 31-16 reside in

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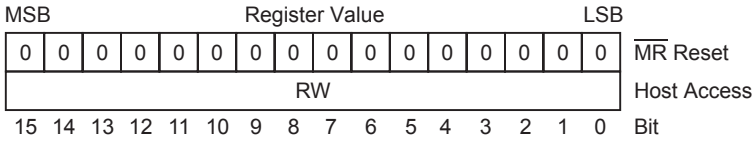
register 0x003B while register 0x003A contains bits 15-0.

The host cannot directly write these registers but uses other methods to control or read Time Tag count. By writing bits 15-14 in the Time Tag Counter Configuration Register 0x0039, the host can clear time tag count to zero, copy the current time count to the SMT Time Tag Utility Register(s), or load the current value contained in the SMT Time Tag Utility Register(s) into the SMT Time Tag counter(s). Finally, the SMT Time Tag Match Register(s) provide capability for host interrupts when the time tag count reaches any predetermined 16- or 48-bit value. For further information, refer to the description of the Time Tag Counter Configuration Register 0x0039.

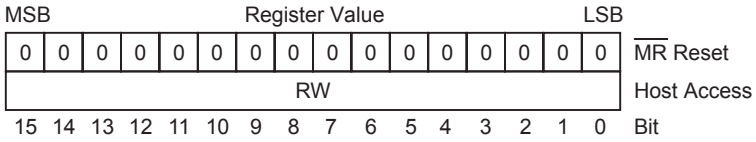
13.8. SMT Bus Monitor Time Tag Utility Register (0x003D)



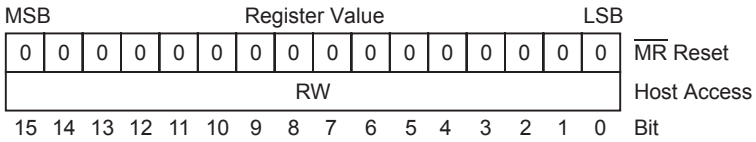
When MT Configuration Register bits 1-0 equal 11, the Simple Message Monitor operates with 16-bit Time Tag resolution and register 0x003D is the only Time Tag Utility register needed.

When MT Configuration Register bits 1-0 equal 01, the Simple Message Monitor operates with 48-bit Time Tag resolution and “utility” operations require the above register plus two additional registers:

13.9. SMT Bus Monitor Time Tag Utility Mid Register (0x003E)



13.10. SMT Bus Monitor Time Tag Utility High Register (0x003F)



These registers are read-write and are cleared after $\overline{MR}$ pin Master Reset. This utility register triplet is used for simultaneously loading or reading a 16- or 48-bit value into or from the SMT Time Tag Counter. Please refer to the description for bits 15-14 in the Time Tag Counter Configuration Register 0x0039 in Section 9.7.

Loading a 16-bit or 48-bit value into the SMT Time Tag Count Register(s)

When loading or clearing Time Tag count, the 16-bit value in Time Tag Utility Register 0x003D is copied into SMT Time Tag Count register 0x003A. If configured for 48-bit time stamp operation, count bits 47-17 and count bits 31-16 are simultaneously copied from Time Tag Utility Registers 0x003F and 0x003E into SMT Time Tag Count Registers 0x003C and 0x003B respectively.

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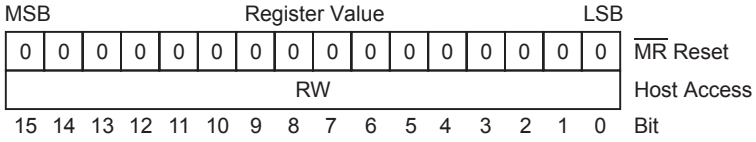
Capturing a 16-bit or 48-bit value from the SMT Time Tag Count Register(s)

When capturing Time Tag count, the 16-bit value in SMT Time Tag Count register 0x003A is copied into Time Tag Utility Register 0x003D. If configured for 48-bit time stamp operation, count bits 47-17 and count bits 31-16 in SMT Time Tag Count Registers 0x003C and 0x003B are simultaneously copied into Time Tag Utility Registers 0x003F and 0x003E respectively.

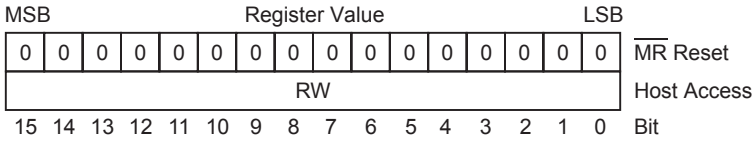
13.11. SMT Bus Monitor Time Tag Match Register (0x0040)



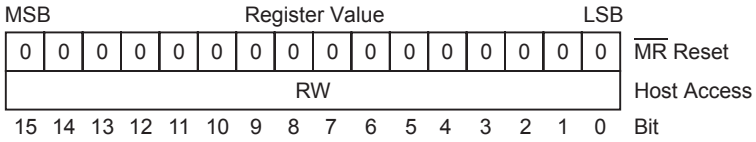
When MT Configuration Register bits 1-0 equal 11, the Simple Message Monitor operates with 16-bit Time Tag resolution and register 0x0040 is the only Time Tag Utility register needed.

When MT Configuration Register bits 1-0 equal 01, the Simple Message Monitor operates with 48-bit Time Tag resolution and time tag matching operations require the above register plus two additional registers:

13.12. SMT Bus Monitor Time Tag Match Mid Register (0x0041)



13.13. SMT Bus Monitor Time Tag Match High Register (0x0042)



These registers are read-write and are cleared after $\overline{MR}$ pin Master Reset. When the MTTTM bit 6 is logic 1 in the Hardware Interrupt Enable Register 0x000F, an interrupt occurs when the MT time tag count matches the value stored in this register triplet. If the MT is configured for 16-bit time tag, Time Tag Match Register 0x0040 is compared to Time Tag Count register 0x003A for match determination.

If configured for 48-bit time tag operation, count bits 47-17 and 31-16 in Time Tag Match Registers 0x0042 and 0x0041 are also compared to MT Time Tag Count Registers 0x003C and 0x003B for 48-bit match determination.

Please refer to the description for MTTTM bit 6 in the Hardware Interrupt Registers described in Section 9.5.

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13.14. SMT Bus Monitor Interrupt Registers and Their Use

Thirteen HI-613x registers are used for host interrupt management. In addition to the Interrupt Count & Log Address Register described in Section 9.4, there are four 3-register groups, separated by function. One register group is for Hardware interrupts, plus one register group each for Bus Controller, Bus Monitor and Remote Terminal interrupts. The Remote Terminal register set is shared between RT1 and RT2. Each group (BC, MT, RT or Hardware) has

- An Interrupt Enable Register to enable and disable interrupts
- A Pending Interrupt Register to capture the occurrence of enabled interrupts
- An Interrupt Output Enable Register to enable $\overline{\text{IRQ}}$ output to host, for pending enabled interrupts

Each individual bit in all three registers is mapped to the same interrupt-causing event when the corresponding interrupt condition is enabled. Numerous interrupt options are available for the SMT. At initialization, bits must be set in the SMT Interrupt Enable register to identify the interrupt-causing events for the SMT which are heeded by the HI-613x. Most Monitor applications use just a subset of available SMT interrupt options. Interrupt-causing events are ignored when their corresponding bits are reset in the SMT Interrupt Enable Register. Setting an Interrupt Enable register bit from 0 to 1 does not trigger interrupt recognition for events that occurred while the bit was zero.

Whenever an enabled monitor interrupt event occurs, the Interrupt Log Buffer is updated and a bit is set in the SMT Pending Interrupt Register. This action takes place only when the corresponding bit is already set in the SMT Interrupt Enable Register. The host can poll the SMT Pending Interrupt Register to detect the occurrence of Monitor interrupts, indicated by non-zero value. When the host reads the SMT Pending Interrupt Register, it automatically clears to 0x0000.

When an enabled interrupt condition occurs and the corresponding bit is also set in the SMT Interrupt Output Enable Register, the $\overline{\text{IRQ}}$ output is asserted to alert the host. Thus, the SMT Interrupt Output Enable Register establishes two interrupt priority levels for the Monitor: high priority interrupts generate an nIRQ signal output, while low priority interrupts do not. The host detects low priority interrupts by polling the SMT Pending Interrupt Register.

A single $\overline{\text{IRQ}}$ host interrupt output signal is shared by all enabled interrupt conditions having bits set in the four Interrupt Output Enable registers. Multiple interrupt-causing events can occur simultaneously, so each $\overline{\text{IRQ}}$ output assertion can result from one or several interrupt conditions.

When the host receives an $\overline{\text{IRQ}}$ signal from the device, it must identify the event (or events) that triggered the interrupt. A hardware-assisted interrupt-decoding scheme simplifies interrupt identification. This scheme uses the three low order bits in the Hardware Pending Interrupt Register.

Upon $\overline{\text{IRQ}}$ interrupt assertion, the host first reads the Hardware Pending Interrupt Register. Bits 15-3 in this register identify hardware interrupt conditions. The three low-order bits in the Hardware Pending Interrupt Register indicate zero vs. non-zero status for the BC, RT and MT Pending Interrupt Registers. If any of these bits is logic 1, the corresponding Pending Interrupt Register has one or more interrupt flags set. Any combination of these 3 bits may be set. Each of the four Pending Interrupt registers self-resets to 0x0000 after the host reads its value. Thus, the host should retain the value read from the Hardware Pending Interrupt Register when 2 or more bits are non-zero in the bit 2-0 range.

When MTIP (MT Interrupt Pending) bit 1 is set in the Hardware Pending Interrupt Register, the SMT Pending Interrupt Register contains a nonzero value, so should be read next to identify the specific SMT interrupt event.

When polling the Pending Interrupt registers to identify low priority interrupts that do not assert the $\overline{\text{IRQ}}$ output, the same method can be applied. At a single read of the Hardware Pending Interrupt Register reveals zero / non-zero status of all four Pending Interrupt registers.

To help the host process interrupts, the HI-613x device maintains information from the 32 most recent interrupts in a 64-word ring buffer in RAM, located at the fixed address range 0x0180 to 0x01BF. Each interrupt stores two information words: the Interrupt Identification Word (IIW) identifies the interrupt type(s) that occurred; the Interrupt Address Word (IAW) identifies the interrupt source. For SMT interrupts, the IAW contains the 16-bit Command Stack address, pointing to the Block Status Word of the message in which the interrupt event occurred.

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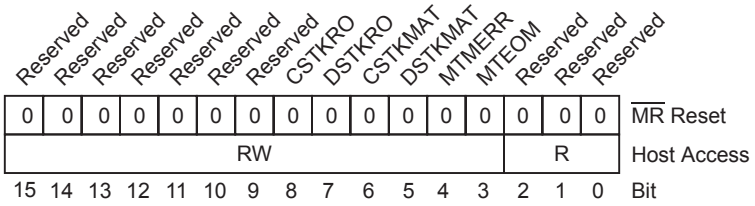
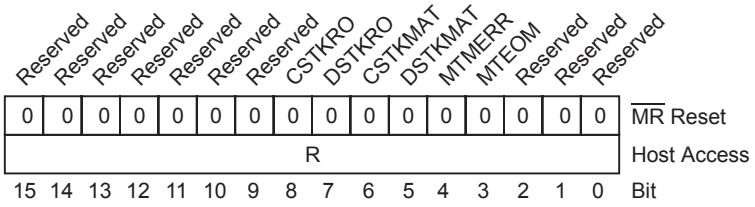
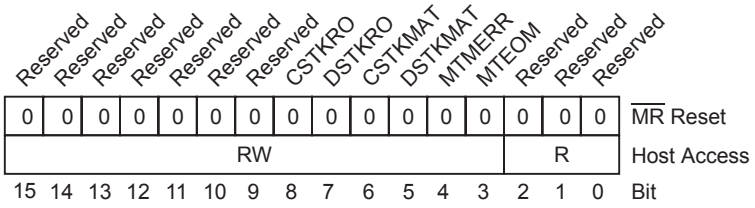
13.14.1. SMT Bus Monitor Interrupt Enable Register (0x0011)



13.14.2. SMT Bus Monitor Pending Interrupt Register (0x0008)



13.14.3. SMT Bus Monitor Interrupt Output Enable Register (0x0015)



Three registers govern SMT interrupt behavior: the SMT Interrupt Enable Register, the SMT Pending Interrupt Register and the SMT Interrupt Output Enable Register. When a bit is set in the SMT Interrupt Enable Register, the corresponding SMT interrupt is enabled. When a bit is reset in this register, the corresponding interrupt event is unconditionally disregarded. Setting a register bit from 0 to 1 does not trigger interrupt recognition for events that occurred while the bit was zero.

When an enabled SMT interrupt event occurs, the corresponding bit is set in the SMT Pending Interrupt Register and the Interrupt Log Buffer is updated. To simplify interrupt decoding, MTIP bit 1 in the Hardware Pending Interrupt Register is also set whenever one or more bits are set in the SMT Pending Interrupt Register.

If the corresponding bit is already set in the SMT Interrupt Output Enable Register, the nIRQ output pin is asserted at Pending Interrupt Register assertion. The SMT Interrupt Output Enable Register establishes two priority levels: high priority interrupts generate an $\overline{IRQ}$ output while low priority interrupts do not. Both priority levels update the SMT Pending Interrupt Register and the Interrupt Log Buffer. The host detects low priority (masked) interrupts by polling SMT Pending Interrupt Register.

The table below describes the bit descriptions shared by all three SMT interrupt registers.

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Bit No.	*Mnemonic*	*Function*
15 − 9	Reserved	These bits are not used in SMT monitor mode. They should be initialized logic 0 in the SMT Interrupt Enable Register. These bits will always read logic 0 in the SMT Pending Interrupt Register.
8	CSTKRO	Command Stack Rollover Interrupt. The Command Stack Pointer value (Word 1 in the SMT Address List) has rolled over to the Command Stack Start Address (Word 0 in the SMT Address List).
7	DSTKRO	Data Stack Rollover Interrupt. The Data Stack Pointer value (Word 5 in the SMT Address List) has rolled over to the Data Stack Start Address (Word 4 in the SMT Address List).
6	CSTKMAT	Command Stack Address Match Interrupt. The Command Stack Pointer value (Word 1 in the SMT Address List) has reached the Command Stack Address Match value in Word 3 of the SMT Address List.
5	DSTKMAT	Data Stack Address Match Interrupt. The Data Stack Pointer value (Word 5 in the SMT Address List) has reached the Data Stack Address Match value in Word 7 of the SMT Address List.
4	SMTMERR	SMT Message Error Interrupt. A non-broadcast MIL-STD-1553 message ended with an RT Status Word containing the ME Message Error status bit set.
3	SMTEOM	SMT End of Message Interrupt. Successful completion of a MIL-STD-1553 message, regardless of validity.
2 − 0	Reserved	Bits 2-0 cannot be written, and read back 000.

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14. IRIG-106 MONITOR TERMINAL (IMT)

The HI-613x can operate as an autonomous MIL-STD-1553 Bus Monitor, requiring minimal host support. Two fundamentally different monitor modes are offered. Each of these modes has a separate data sheet section describing registers used and operational details. Information regarding the alternative Simple Monitor Terminal (SMT) may be found in Section 12.

14.1. Overview

IRIG-106 Monitor Terminal (IMT) mode complies with IRIG-106, a comprehensive standard ensuring interoperability of aeronautical telemetry at United States Military RCC member ranges. The telemetry group of the Range Commanders Council maintains the IRIG-106 standard. Chapter 10 of the standard defines operation and interfaces for digital flight data recorders over a range of telemetry protocols, including MIL-STD-1553. Further information on the IRIG-106 standard can be found at http://irig106.org/

The HI-613x is configured for IMT operation when bit 0 in the MT Configuration Register 0x0029 is logic 0. The IMT always operates with 48-bit Time Tag resolution. In register 0x0000, MTENA bit 8 is logically ANDed with the MTENA input pin to enable the Bus Monitor. If the MTENA input pin or register bit equals logic 0, Bus Monitor operation is disabled. When the pin and MTENA register bit are both logic 1, the Bus Monitor is enabled. Operation commences when the receiver first decodes MIL-STD-1553 activity meeting the “start record” criteria selected by bits 6-5 in the MT Configuration Register. If monitor operation is underway when the MTENA register bit or input pin becomes logic 0, monitor operation stops and the open data packet is finalized after completion of any message already underway.

The Holt IRIG-106 Monitor Terminal (hereafter called IMT) uses a single storage stack in device RAM. Recorded message data, message results and characteristics are stored in multiple-message “data packets”. As they occur, MIL-STD-1553 messages are appended to the end of the open data packet and time stamped with a 48-bit Time Tag value. By default, the IMT records all MIL-STD-1553 messages, although it optionally records just selected messages, based on RT address, subaddress and transmit/receive status for each detected Command Word.

The IMT optionally generates a Packet Header and Packet Trailer consistent with IRIG-106 Chapter 10 specifications. The header contains various data including data packet size, time stamp and header checksum. The trailer is primarily comprised of a data checksum. While the IRIG-106 standard requires a header and trailer on each data packet, some applications will require data packet size exceeding the RAM capacity of the HI-613x device. In this case, the IMT may be configured to disable automatic header and trailer generation, so the entire RAM buffer is used for message storage. Upon receiving each end-of-packet interrupt, the host offloads the entire block of new message data, which may be appended to a large packet buffer RAM, accessible to the host microcontroller. At the appropriate time, the host then generates the required IRIG-106 packet header and packet trailer.

The IMT can be configured to automatically start a new data packet after finalization of each completed data packet, or the host microcontroller can command the start of the new data packet. In either case, the starting address for the new packet follows the last storage address of the previous packet (even when the last packet was finalized due to imminent buffer overrun). The device stores packet data in circular buffer fashion, automatically wrapping around to the buffer start address after the last buffer address is written. The host microcontroller is responsible for offloading each data packet in a timely manner to avoid data overwrite by the HI-613x device. One strategy: enable a “packet ready” interrupt, as well as an “N-word warning before full buffer” interrupt triggered halfway through the IMT RAM buffer capacity. The host microcontroller uses these alternating interrupts to pace data buffer offloading, reading a half buffer each time one of the two interrupts occurs.

The HI-613x IMT is highly flexible. According to the IRIG-106 standard, the Block Status Word stored for each MIL-STD-1553 message contains several reserved status bits which always read logic 0. The HI-613x device optionally uses these bits to convey additional status information to the host; the host then resets the reserved bits before including the Block Status Word in the IRIG-106 data packet.

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14.2. IRIG-106 Bus Monitor - Data Packet Format

When the HI-613x Bus Monitor is initialized for IMT operation, recorded bus message information is stored in device RAM using a “data packet“ format consistent with IRIG-106 Chapter 10. The IRIG-106 data packet is comprised of three parts: a Packet Header, a Packet Body (containing the monitored MIL-STD-1553 message information) and a Packet Trailer. The HI-613x IMT may be configured to generate complete data IRIG-106 packets, including Packet Header and Packet Trailer, or may be configured to generate only the Packet Body, without Packet Header and Packet Trailer.

The IRIG-106 data packet is shown in Figure 8. When the IMTHTD bit 3 in the IMT Configuration Register 0x0029 is logic 1, the HI-613x stores only the Packet Body. When the IMTHTD bit 3 is logic 0, the HI-613x stores a Packet Header and Packet Trailer, described on the next pages, in addition to the Packet Body.

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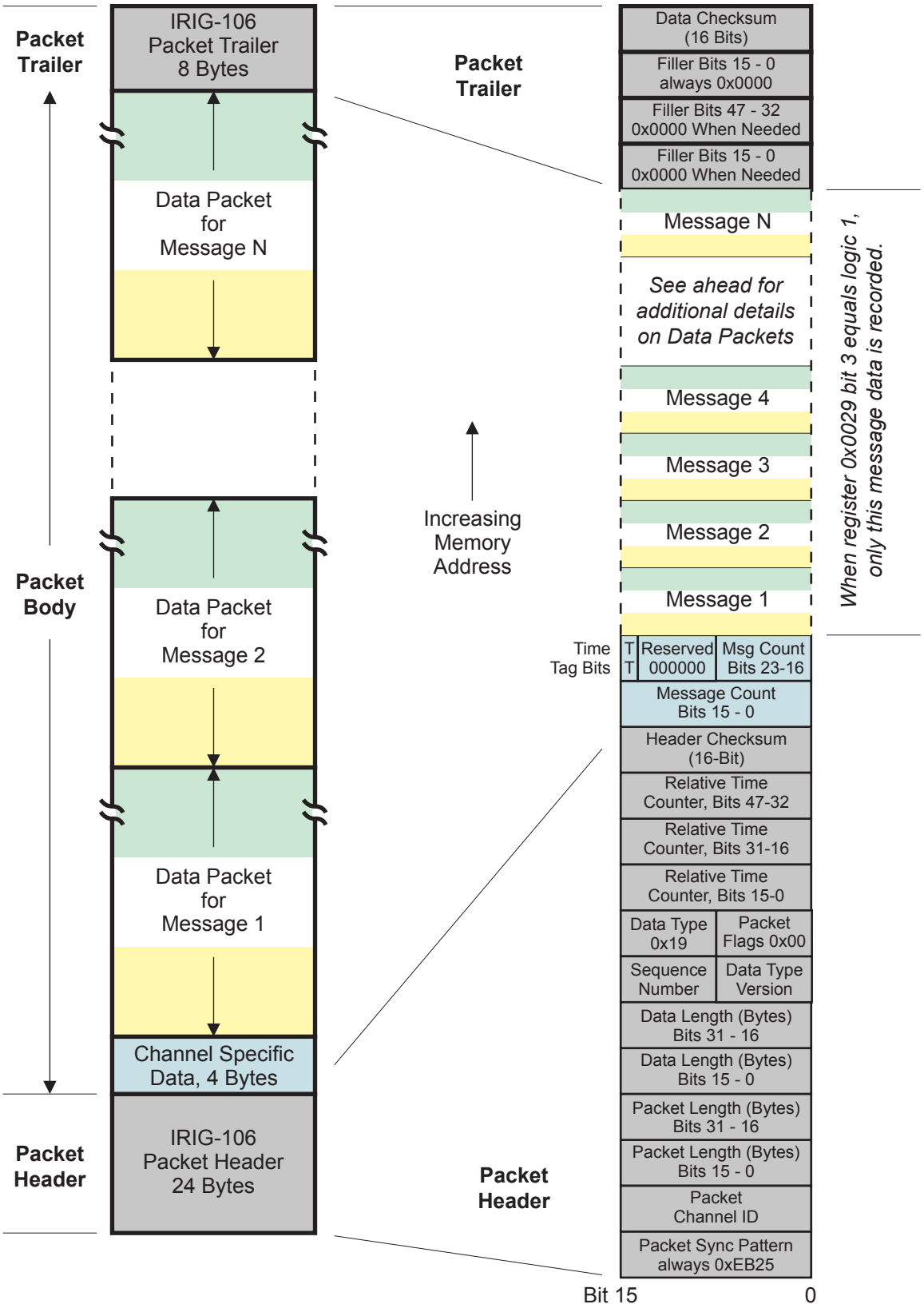

Figure 8. IRIG-106 Data Packet and Message Storage Summary

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14.3. IRIG-106 Packet Header Description

The length of the packet header is fixed at 24 bytes, shown in as twelve 16-bit words. The Packet Header consists of 10 contiguous fields in the following sequence:

14.3.1. Packet Sync Pattern.

A static sync value of 0xEB25 is used for every packet.

14.3.2. Channel ID.

This 2-byte field contains a value representing the Packet Channel ID. The Packet Header is generated using the value stored in register 0x002E.

14.3.3. Packet Length.

This 32-bit field contains a value representing the length of the entire packet. The value indicates the number of bytes in the packet, and is always a multiple of four (bits 1-0 are always 0-0). The Packet Length includes the Packet Header, Channel Specific Data, Intra-Packet Headers, Data, Filler, and Data Checksum. (The HI-613x IMT does not generate the optional Packet Secondary Header.)

14.3.4. Data Length.

This 32-bit field contains a value representing the valid data length within the packet, expressed in number of bytes. Valid data length includes Channel Specific Data, Intra-Packet Data Headers, Intra-Packet Time Stamp(s), and Data, but does not include the Packet Trailer Filler and Data Checksum.

14.3.5. Data Type Version.

This 8-bit field contains a value at or below the release version of the IRIG-106 standard applied to the data types in the table below. The Packet Header is generated using the value encoded by bits 11-10 in register 0x0029. The Data Type value is used in the Packet Header as shown below.

Register 0x0029 Bits 11-10	*Data Type*	*IRIG-106*
01	0x01	IRIG-106-04 (original release)
10	0x02	IRIG-106-05 (default
11	0x03	IRIG-106-07
00	0x04	IRIG-106-09

14.3.6. Sequence Number.

This 8-bit field contains a value representing the packet sequence number for each Channel ID. This is simply a counter that increments to a maximum count of 0xFF, incrementing once for every packet transferred. After master reset, the Sequence Number starts at 0x00. Upon reaching 0xFF, the Sequence Number rolls over to 0x00 and continues counting.

14.3.7. Packet Flags.

This 8-bit field equals either 0x00 or 0x02, depending on the checksum type selected by bit 1 in register 0x0029. If Data

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Checksum is disabled, this field equals 0x00. If 16-bit Data Checksum is enabled, this field equals 0x02. Although bits 7-2 in this field always equal logic 0, the encoded significance for all eight Packet Flags is explained here:

- Packet Secondary Header is not present (bit 7)
- Packet Header 48-bit Relative Time Count used for Intra-Packet Time Stamps (bit 6)
- Sync error did not occur for Relative Time Count (bit 5)
- Data Overflow error did not occur (bit 4)
- Optional IRIG-106 Packet Secondary Header is not used (bits 3-2)
- Data Checksum format: bits 1-0 always equal 00 or 10

  00 = data checksum disabled (automatic, when register 0x0029 bit 1 = logic 0)

  01 = 8-bit data checksum (option not available)

  10 = 16-bit data checksum (automatic, when register 0x0029 bit 1 = logic 1)

  11 = 32-bit data checksum (option not available)

14.3.8. Data Type.

This 8-bit field contains a value representing the type and format of the data. The HI-613x IMT always generates a fixed Data Type value of 0x19, which represents a MIL-STD-1553B Format 1 data packet.

14.3.9. Relative Time Counter.

This 48-bit (3-word) field contains a value representing the 10 MHz Relative Time Counter (RTC). The RTC is derived from an internal clock generator, and remains free running during each data packet recording. The 48-bit value applies to the first bit of message data in the packet body.

14.3.10. Header Checksum.

This 16-bit (1-word) field contains the 16-bit arithmetic sum of all 16-bit words in the header, excluding the Header Checksum word itself.

14.4. IRIG-106 Packet Trailer Description

IRIG-106 defines a Packet Trailer consisting of an optional Data Checksum, preceded by “filler words”. The standard requires the overall packet length to be an even number of 16-bit words. The HI-613x IMT inserts 0x0000 “filler” words to meet this requirement. Every packet generated by the HI-613x IMT has a Packet Trailer consisting of 2 or 3 filler words (0x0000) followed by the 16-bit Data Checksum word.

Bit 1 in register 0x0029 enables/disables automatic generation of a 16-bit Data Checksum. When auto checksum is disabled, the Packet Trailer simply consists of 3 or 4 filler words. When the configuration bit is logic 1, the 16-bit checksum is written into the last packet word at packet finalization. If an 8- or 32-bit data checksum is needed, the host must generate it. IRIG-106 defines the Data Checksum as the arithmetic sum of all of the bytes (8-bit checksum), words (16-bit checksum) or long words (32-bit checksum) in the entire packet, excluding the 24-byte Packet Header and the Data Checksum itself.

14.5. IRIG-106 Data Packet Trailer Description

The HI-613x IMT Packet Body consists of a 32-bit Channel Specific Data field, followed by one or more message data blocks, with separate message data blocks for each monitored MIL-STD-1553 message.

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14.5.1. Channel Specific Data.

This 32-bit field occurs once per packet and precedes the packet channel data. The Channel Specific Data is comprised of the following fields:

Bits 31-30	*Bits 29-24*	*Bits 23-0*
Time Tag Bits	Reserved, always 000000	Message Count

Bits 31-30 indicate the MIL-STD-1553 data bit at which Intra-Packet Header time stamp occurs for each message:

00 = time stamp occurs at the last bit of the last word in the message

01 = time stamp occurs at the first bit of the first word in the message

10 = time stamp occurs at the last bit of the first word in the message

11 = reserved, not used

Bits 23-0 indicate the binary count for the number of MIL-STD-1553 messages included in the packet. An integral number of complete transaction messages will be in each packet

For each monitored MIL-STD-1553 message, three data fields are stored in the Packet Body. These are shown in Figure 10, and explained here:

14.5.2. IRIG-106 Intra-Packet Time Stamp.

This 64-bit field contains a 48-bit Relative Time Counter value that marks the relative reception time for the MIL-STD-1553 message. The high order 16 bits always equal 0x0000. Time stamping occurs at the message bit indicated in the Channel Specific Data.

14.5.3. IRIG-106 Intra-Packet Data Header.

This 48-bit field is comprised of the following sub fields:

Block Status Word (BSW). This 16-bit word indicates status for the following MIL-STD-1553 message and indicates MIL-STD-1553 bus protocol errors.

Response Time Word. This 16-bit word contains two 8-bit fields. For all messages except RT-to-RT, the GAP1 byte indicates the RT response time. For RT-to-RT messages, the GAP1 byte indicates the Transmit RT response time, and the GAP2 byte indicates the Receive RT response time:

Bits 15-8	*Bits 7-0*
GAP2	GAP1

For both gap measurements, response time is measured consistently with MIL-STD-1553 definition, from the mid-parity zero crossing of the preceding word, to the mid-sync zero crossing of the RT Status Word. For both, the resolution is 100 ns per LSB, with a maximum time value of 25.5 µs.

Message Length Word. This 16-bit word indicates the number of bytes in the following message data block, ranging from 2 to 72 bytes, for 1 to 36 stored 16-bit words.

14.5.4. IRIG-106 Message Data.

This variable length block stores all MIL-STD-1553 message words in the order received. The number of words stored depends on the MIL-STD-1553 message type, ranging from 1 word stored (for a broadcast mode code command without data), to 36 words stored for an RT-to-RT message. Refer to Figure 10. An IRIG-106 packet typically contains numerous MIL-STD-1553 messages, although the standard states the packet must contain at least one message (no

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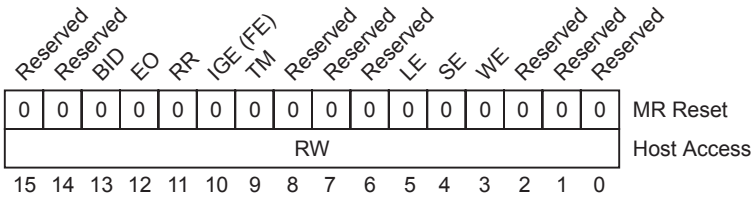
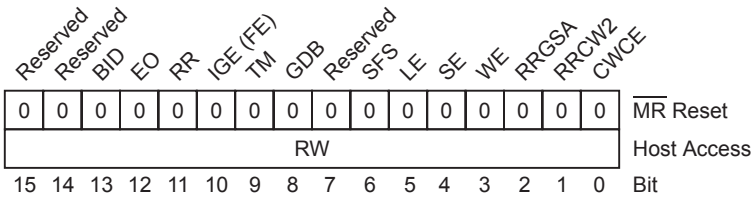
empty packets).

14.6. IMT Block Status Word (BSW) Description

The IRIG-106 standard describes a Block Status Word stored within the Intra-Packet Data Header for each monitored MIL-STD-1553 message. This word provides information regarding message status, the bus on which the message occurred, whether errors occurred during the message, and the type of occurring errors. The IRIG-106 Chapter 10 compliant Block Status Word contains eight reserved bits, which the HI-613x IMT writes as logic 0:



The HI-613x IMT offers an Extended Status reporting option, enabled when bit 2 in register 0x0029 is logic 1. When this option is enabled, all but one of the Reserved status bits are used to convey additional status information. Although the extended status bits do not comply with the IRIG-106 Chapter 10 standard, the host can reset the 7 normally reserved bits after reading the BSW. If using the IMT-generated 16-bit Data Checksum (enabled when register 0x0029 bits 1:0 equal 1-0), be advised that the tallied checksum value is based on the BSW value that was written into the data packet by the device, at individual MIL-STD-1553 message completion. The Block Status Word with Extended Status is defined:



IMT Block Status Word
with Extended Status Bits Enabled
(Not IRIG-106 Chapter 10 Compliant)

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	Reserved	R/W	0	Bit 15 is not used in IMT mode, always reads logic 0.
14	Reserved	R/W	0	Bit 14 is not used in IMT mode, always reads logic 0.
13	BID	R/W	0	Bus ID (Bus B / $\overline{\text{Bus A}}$). Bit 13 indicates the bus ID for the message. This bit is logic 0 for a message occurring on Bus A. This bit is logic 1 for a message occurring on Bus B.

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Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
12	EO	R/W	0	Error Occurred Flag. This bit indicates a message error was encountered. This bit is set when one or more of the following conditions are true (logical-OR): • an unfinished message is superseded by another valid command • Bit 10 Illegal Gap Error is set • Bit 9 Response Timeout is set • Bit 5 Length (Word Count) Error is set • Bit 4 Sync Type Error is set • Bit 3 Invalid Word Error is set • Bit 2 RT-RT Gap / Sync / Address Error is set • Bit 1 RT-RT Command Word 2 Error is set (except as noted) • Bit 0 Command Word Content Error is set (except as noted) Three exceptions where register bit 0 or 1 is set without affecting bit 12 state: **Bit 1 RT-RT Command Word 2 Errors that do not assert bit 12** • RT-RT Transmit Command Word 2 subaddress field equals 00000 or 11111 (mode code command indicated) • RT-RT Transmit Command Word 2 has the same RT Address as Receive Command Word 1 **Bit 0 Command Word Content Error that does not assert bit 12** • Undefined receive mode code 0~15 decimal.
11	RR	R/W	0	RT-to-RT Transfer When logic 1, bit 11 indicates an RT-to-RT message, beginning with two contiguous Command Words.
10	IGE	R/W	0	Illegal Gap Error When logic 1, bit 10 indicates an illegal gap occurred on the bus, other than Response Timeout. The IRIG-106 Standard refers to this bit as Format Error, having the same definition.
9	TM	R/W	0	Response Timeout. When logic 1, bit 9 indicates a response timeout occurred. This bit is set if an RT Status Word associated with this message failed to arrive within the response time interval specified by bits 15-14 in the MT Configuration Register 0x0029. For IRIG-106 compatibility, bits 15-14 in register 0x0029 should be initialized to 00, corresponding to a 14µs response time, as defined by MIL-STD-1553B (12µs bus dead time).

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Bit No.	Mnemonic	R/W	Reset	Function
8	GDB	R/W	0	Good Data Block Transfer. ***only if Extended Status is enabled*** Bit 8 is set to logic 1 following completion of a valid, error-free message. This bit is reset to logic 0 following completion of a message in which error occurred. If an RT responds to a transmit command with Busy status without transmitting the commanded data word(s), this message does not reset the GDB bit.
7	Reserved	R/W	0	Bit 7 is not used in IMT mode, always reads logic 0.
6	SFS	R/W	0	Status Flag Set ***only if Extended Status is enabled*** Bit 6 is logic 1 when a status bit was set in an RT Status Word response.
5	LE	R/W	0	Length (Word Count) Error Bit 5 indicates that the number of data words transmitted by the BC or RT differs from the Word Count specified in the Command Word. An RT Status Word with the Busy bit set will not cause Word Count Error. A transmit command with Response Timeout will not cause Word Count Error.
4	SE	R/W	0	Sync Type Error Bit 4 is logic 1 to indicate that a BC transmitted data sync with a Command Word, or a command / status sync occurred with Data Word, or an RT responded with data sync in its Status Word and/or command/ status sync in a Data Word.
3	WE	R/W	0	Invalid Word Error (WE) Bit 3 is logic 1 when invalid word error occurred. This includes Manchester decoding errors in the sync pattern or word bits, or the wrong number of bits in the word, or parity error.
2	RRGSA	R/W	0	RT-to-RT Gap/Sync/Address Error (RRGSA) ***only if Extended Status is enabled*** Bit 2 is logic 1 if one or more of these RT-RT message conditions occur: • MT Gap Check is enabled (bit 12 equals 1 in register 0x0029) and an RT Status Word is received having a response time less than 4µs, per MIL-STD-1553B (mid-parity to mid-sync). In other words, the bus “dead time” was less than 2µs. • One of the RTs responds with an invalid Status Word, having a sync error, a Manchester encoding error, bit count error and/or parity error • One of the RT Status Words contains an RT Address that differs from the RT Address in the corresponding Command Word.

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Bit No.	Mnemonic	R/W	Reset	Function
1	RRCW2	R/W	0	RT-to-RT Command Word 2 Error (RRCW2) ***only if Extended Status is enabled*** Bit 1 is logic 1 if an RT-to-RT message occurs (two contiguous Command Words) with one or more of the following illogical conditions: • Transmit Command Word 2 T/$\overline{R}$ bit equals 0 (receive) • Transmit Command Word 2 subaddress field equals 00000 or 11111 (mode command indicated) • Transmit Command Word 2 has the same RT Address as Receive Command Word 1
0	CWCE	R/W	0	Command Word Content Error (CWCE) ***only if Extended Status is enabled*** Bit 0 is logic 1 if a received Command Word violates one or more MIL-STD-1553B requirements: • A non-mode broadcast transmit Command Word occurred. (non-mode has 5-bit subaddress field equal to decimal 1~30) • A receive mode code Command Word was received with mode code in the range of 0~15 decimal (undefined) • A broadcast transmit mode code command occurred having a mode code value for which broadcast is not allowed (mode code = decimal 0, 2, 16, 18 or 19)

14.7. IMT Message Filter Table

The IRIG-106 Message Monitor can select messages for monitoring through the use of a 128-word MT Filter Table, located at fixed RAM address 0x0100. When the table bit corresponding to a new message Command Word is logic 1, that message is ignored by the monitor. If the table bit is logic 0, that message is recorded.

After nMR master reset, all MIL-STD-1553 messages are monitored because the entire table ranging from 0x0100 to 0x017F inclusive is 0x0000. Thus every valid Command Word received on an idle bus marks the start of a new MIL-STD-1553 message recorded by the monitor. When the table bit corresponding to a new message Command Word is logic 1, that message is ignored by the monitor. The Message Filter Table is addressed using three fields in the received Command Word: the 5-bit RT Address field, the T/$\overline{R}$ Transmit/Receive bit and the MSB of the 5-bit Subaddress field. This is illustrated in Figure 9.

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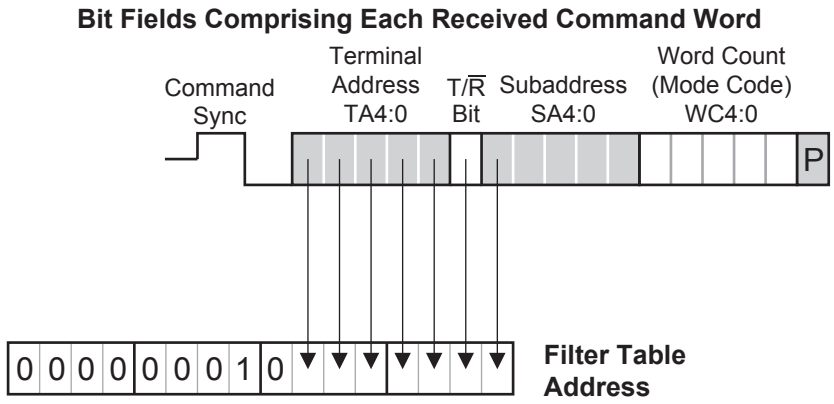

Figure 9. Deriving the Monitor Filter Table Address from the Received Command Word

Each RT Address from 0 to 31 decimal has four 16-bit table words: two words enable/disable individual Receive Subaddresses, two more words enable/disable individual Transmit Subaddresses. The first four table words apply to Subaddress 0 and are illustrated in Table 12. This 4-word pattern repeats for all 32 Subaddresses, 0-31 decimal.

Table 12. IMT Message Filter Table (RT Address 0 example)

A subaddress message is monitored when the corresponding word bit equals logic 0. The message is not monitored when the bit equals 1.																
Table address 0x0103								**RT Address 0, Transmit Subaddresses 31 to 16**								
Word Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Transmit SA	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Table address 0x0102								**RT Address 0, Receive Subaddresses 31 to 16**								
Word Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Transmit SA	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Table address 0x0101								**RT Address 0, Transmit Subaddresses 15 to 0**								
Word Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Transmit SA	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Table address 0x0100								**RT Address 0, Receive Subaddresses 15 to 0**								
Word Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Transmit SA	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

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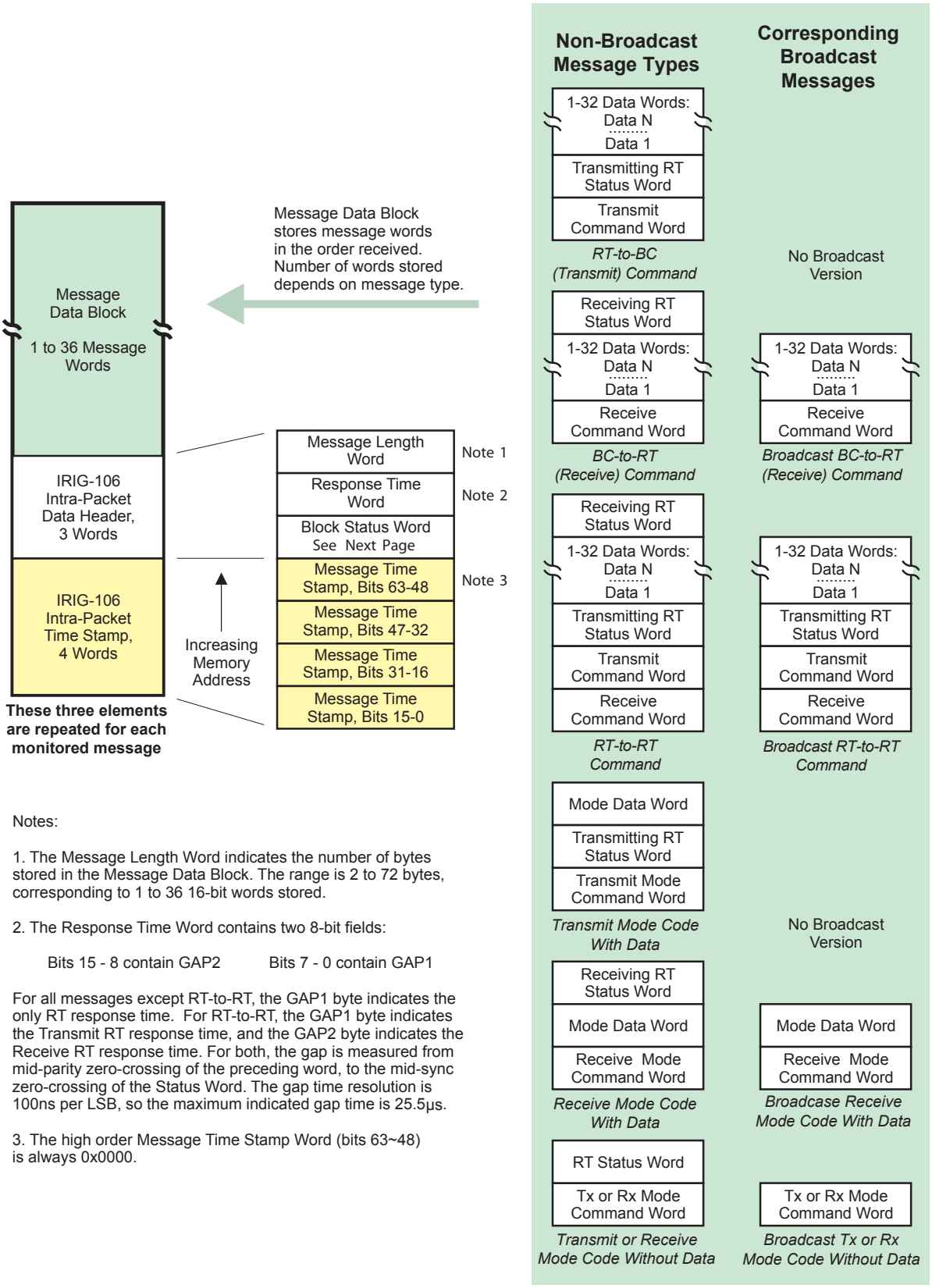

Notes:

1. The Message Length Word indicates the number of bytes stored in the Message Data Block. The range is 2 to 72 bytes, corresponding to 1 to 36 16-bit words stored.

2. The Response Time Word contains two 8-bit fields:

Bits 15 - 8 contain GAP2 Bits 7 - 0 contain GAP1

For all messages except RT-to-RT, the GAP1 byte indicates the only RT response time. For RT-to-RT, the GAP1 byte indicates the Transmit RT response time, and the GAP2 byte indicates the Receive RT response time. For both, the gap is measured from mid-parity zero-crossing of the preceding word, to the mid-sync zero-crossing of the Status Word. The gap time resolution is 100ns per LSB, so the maximum indicated gap time is 25.5µs.

3. The high order Message Time Stamp Word (bits 63~48) is always 0x0000.

Figure 10. IRIG-106 Data Fields and Message Storage

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15. IRIG-106 BUS MONITOR (IMT) CONFIGURATION AND OPERATION

The HI-613x is initialized for IRIG-106 Chapter 10 operation (IMT) by resetting bit 0 in the Bus Monitor Configuration Register 0x0029 to logic 0. The MIL-STD-1553 bus monitors that comply with IRIG-106 produce “data packets” in a format defined by the IRIG-106 standard. Figure 8 shows the overall data packet structure, comprised of three parts: a Packet Header, a Packet Body (containing the monitored MIL-STD-1553 message information) and a Packet Trailer. The HI-613x IMT may be configured to generate complete data IRIG-106 packets, including Packet Header and Packet Trailer, or may be configured to generate only the Packet Body, without header or trailer. A range of options is offered for configuring the Packet Header and Packet Trailer.

15.1. Generating complete IRIG-106 Data Packets

IMTHTD bit 3 in the MT Configuration Register 0x0029 is logic 0

The IMT generates the Packet Header and Packet Trailer after the first MIL-STD-1553 message is recorded when starting a new packet. When each new message data packet is added to the Packet Body, the device updates the Packet Header and generates a new Packet Trailer. Refer to Figure 8. When one data packet is finalized and the next data packet begins, the device adjusts the Address List pointers so the new Packet Header starts at the last unwritten Stack address.

15.2. Generating only IRIG-106 Packet Body (no header or trailer)

IMTHTD bit 3 in the MT Configuration Register 0x0029 is logic 1

The IMT devotes the entire RAM stack for message data packets. For each monitored message, only the Intra-Packet Timestamp, Intra-Packet Data Header, and Message Data Block are stored, per Figure 10 and the note in Figure 8. When operated in this mode, the RAM stack is fully utilized for message data; the first Intra-Packet Timestamp occurs at the stack Start Address initialized in the IMT Address List. The host assumes responsibility for generating the IRIG-106 Packet Header, Channel Specific Data and Packet Trailer. Otherwise, there may be situations when IMT packet body structure is simply preferred over SMT storage format, in a non-IRIG application that does not need the header or trailer overhead.

When operating in IMT mode, MIL-STD-1553 message data is added to the unfinished data packet until the packet is “finalized.” The host can initiate packet finalization by setting the PKTSTOP bit in the MT Configuration Register. Criteria for automatic packet finalization can be specified using customized limits. These host-initialized limits for packet completion are optional, enabled or disabled by configuring limit registers 0x002A through 0x002D. When the applicable limit register contains zero, that criteria for packet finalization is disabled. The practical maximum value for each of these limits is actually much smaller than limits shown below, as explained in the descriptions for registers 0x002A through 0x002D.

- host-specified maximum MIL-STD-1553 message count (1 to 65,535) in register 0x002A
- host-specified maximum word count (1 to 65,535 words) in register 0x002B
- host-specified maximum recording time (655.35 ms max, 10 µs resolution) in register 0x002C
- host-specified maximum intermessage gap (655.35 ms max, 10 µs resolution) in register 0x002D

The data packet ends and packet generation encapsulates the recorded data when the first of the set data packet limits is reached.

An open IRIG-106 data packet is also finalized when written packet data first crosses within 64 words of overrunning buffer space. This criteria, imminent buffer overrun, is mandatory and cannot be disabled. The current data packet is terminated when written packet length is within 64 words of overwriting the Current Packet Start Address (maintained

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in Address List Word 1 by the device).

The host initializes a Monitor Address List in RAM to reserve address space for the IMT storage stack and define buffer utilization interrupt behavior. For IMT mode, the 8-word Monitor Address List is defined as shown in Table XX.

Table 13. Monitor Address List for IMT Mode

Addr. List	*Name*	*Function*
Word 7	Packet Fill Warning Interrupt	These bits are not used in SMT monitor mode. They should be initialized logic 0 in the SMT Interrupt Enable Register. These bits will always read logic 0 in the SMT Pending Interrupt Register.
Words 6 − 5	Not Used	Command Stack Rollover Interrupt. The Command Stack Pointer value (Word 1 in the SMT Address List) has rolled over to the Command Stack Start Address (Word 0 in the SMT Address List).
Word 4	Last Written Block Status Word Address	Data Stack Rollover Interrupt. The Data Stack Pointer value (Word 5 in the SMT Address List) has rolled over to the Data Stack Start Address (Word 4 in the SMT Address List).
Word 3	Stack Address Interrupt	Command Stack Address Match Interrupt. The Command Stack Pointer value (Word 1 in the SMT Address List) has reached the Command Stack Address Match value in Word 3 of the SMT Address List.
Word 2	Stack Address Interrupt	Data Stack Address Match Interrupt. The Data Stack Pointer value (Word 5 in the SMT Address List) has reached the Data Stack Address Match value in Word 7 of the SMT Address List.
Word 1	Current Packet Start Address	SMT Message Error Interrupt. A non-broadcast MIL-STD-1553 message ended with an RT Status Word containing the ME Message Error status bit set.
Word 0	Stack Start Address	SMT End of Message Interrupt. Successful completion of a MIL-STD-1553 message, regardless of validity.

For purposes of this discussion, it is important to make a distinction between Stack Addresses and Packet Addresses. The Stack address range is fixed and initialized when the host writes Address List Words 0 and 2. The Packet address range is dynamic. The Current Packet Start Address must be initialized by the host for the first data packet; however this value is maintained by the device each time a new packet it started.

- Stack Start Address and Stack End Address define the Stack Start and End Address boundaries. These limits usually do not coincide with stored data packet boundaries, except the first data packet following device $\overline{MR}$ reset typically begins at the Stack Start Address.
- Packet Start Address and Packet End Address express a smaller address range for storing an IMT data packet. Because successive data packets are written in circular buffer fashion, there are times when Packet Start Address approaches the Stack End Address. The packet fills the remaining stack address range and wraps around to continue storing the packet at the Stack Start Address and beyond. In this case, Packet Start Address is greater than Packet End Address, but both packet addresses occur between the Stack Start and End Addresses.
- Current Packet Start Address is initialized by the host (typically equal to Stack Start Address) but is updated by the device each time a data packet is finalized, and the next data packet has started at the following memory address.

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- Initialized values for registers 0x002A – 0x002D may result in multiple small packets occurring within the Stack address range. If registers 0x002A through 0x002D all contain zero, data packet finalization defaults to “imminent buffer overrun” mode. Each data packet created will be slightly less than the allocated Stack address range. Successive IRIG-106 data packets are written in circular buffer fashion. Each new data packet starts one word after the final word in the previously finalized data packet.
- If the first data packet after reset begins at the Stack Start Address, it will be finalized and the second data packet will begin before reaching the Stack End Address boundary.
- Last-Written Block Status Word Address is updated by the device each time a Block Status Word is added to the end of the packet for a newly received MIL-STD-1553 message.
- Two optional stack interrupts are offered. When enabled, the Stack Address Interrupt occurs whenever the matching RAM address in the Stack is written. This address is fixed with respect to the Stack Start and End Addresses.
- When enabled, the Packet Fill Warning Interrupt is generated when the packet length reaches a specified number of words before Packet Start Address overwrite occurs. Because Packet Start Address “walks” through the stack address range for successive packets, the interrupt logic adjusts the Packet Fill Warning Interrupt address automatically. The fill warning number can be any value, i.e. half-way, 8,192 for a 16,384-word buffer. Used in conjunction with the Packet Ready interrupt, this packet “half full” setting produces alternating interrupts at the “half full” and “full” packet conditions. To prevent packet start address overwrite, these two interrupts tell the host when to offload data, a half packet at a time. In the event that the host is unable to immediately service a Packet Ready interrupt, no data is lost when the IMT is configured to immediately start a new packet upon completion of the prior packet (i.e., when PKTMR bit 7 equals logic 1 in the IMT Configuration Register 0x0029).

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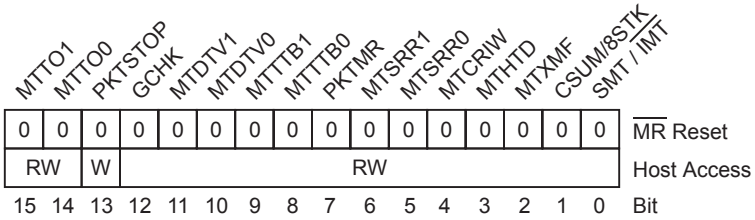
16. REGISTERS USED BY THE IMT BUS MONITOR

In addition to the registers described here, a HI-6131 IMT Bus Monitor also utilizes one or more Memory Address Pointer registers (described in Section 9.8) for managing SPI read/write operations. This comment does not apply for parallel bus interface HI-6130 designs.

16.1. IMT Bus Monitor MT Configuration Register (0x0029)



Bit No.	Mnemonic	R/W	Reset	Function
15 − 14	MTTO1:0	R/W	0	MT Time Out Select. This 2-bit field selects the Monitor “no response” time-out delay from four available selections. Excluding RT-RT commands, the delay is measured from command word mid-parity bit to status word mid-sync.

Bit 15:14	***Bus Dead Time***	***Time Out (excludes RT-RT)***	***RT-RT Time Out***
00	16µs	18µs	61µs
01	21µs	23µs	66µs
10	80µs	82µs	122µs
11	138µs	140µs	180µs

For RT-RT commands, time out delay is measured per Figure 8 in the RT Validation Test Plan, SAE AS4111. That is, from mid-parity of the receive command to mid-sync of the first received data word. This adds 40µs for the embedded transmit command word and transmit-RT status word within this interval.

Bit No.	Mnemonic	R/W	Reset	Function
13	PKTSTOP	W	0	MT Packet Stop. If packet recording is underway when the PKTSTOP bit is set, the IMT stops recording then post-processes the packet. If a MIL-STD-1553 message is underway when PKTSTOP is set, recording continues to message completion. The IMT immediately begins recording a new packet. If packet recording is not underway, setting PKTSTOP has no effect. This bit self-resets when written to logic 1. Writing logic 0 to this bit has no effect.

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>12</td><td>GCHK</td><td>R/W</td><td>0</td><td>Gap Check.
When this bit equals 1, the IMT monitor evaluates inter-message gaps and RT response times for a minimum preceding bus dead time of 2 µs. This dead time corresponds to an inter-message gap of 4µs, measured per MIL-STD-1553, from mid-parity zero crossing of the preceding word, to mid-sync zero crossing of the following word. A minimum gap time violation results in a Format Error in the Block Status Word for the message.
When this bit equals 0 (recommended), the monitor does not check for short inter-message gap times.</td></tr>
<tr><td>11 – 10</td><td>MTDTV1:0</td><td>R/W</td><td>0</td><td>IMT Packet Header “Data Type Version”.
This IMT setting is only meaningful when MTHTD (register bit 3) equals 0, enabling automatic generation of IRIG-106 data packet header and packet trailer.
The IRIG-106 Chapter 10 packet header contains an 8-bit field “Data Type” field corresponding to the IRIG-106 version applied to the data. Register bits 15-14 specify one of four Data Type values (0x01 – 0x04) for insertion into the generated packet header:
<table>
<tr><th>Bit 11:10</th><th>Header Data Type</th><th>IRIG Release</th></tr>
<tr><td>00</td><td>0x04</td><td>IRIG-106-09</td></tr>
<tr><td>01</td><td>0x01</td><td>IRIG-106-04</td></tr>
<tr><td>10</td><td>0x02</td><td>IRIG-106-05 (default)</td></tr>
<tr><td>11</td><td>0x03</td><td>IRIG-106-07</td></tr>
</table>
This selection does not affect data encoding, only the 8-bit Data Type code inserted into the IRIG-106 packet header.</td></tr>
<tr><td>9 – 8</td><td>MTTTB1:0</td><td>R/W</td><td>0</td><td>Monitor Time Tag Message Bit Select.
This 2-bit field selects the bit within the MIL-STD-1553 message where time stamp occurs. Time stamp occurs at mid-bit transition:
<table>
<tr><th>Bit 9:8</th><th>Time Tag Event</th></tr>
<tr><td>00</td><td>Last Bit of Last Word in Message</td></tr>
<tr><td>01</td><td>First Bit of First (Command) Word in Message</td></tr>
<tr><td>10</td><td>Last Bit of First (Command) Word in Message</td></tr>
<tr><td>11</td><td>time tag disabled, stores time tag = 0</td></tr>
</table>
For options 00 and 10, the “Last Bit” precedes the word’s parity bit. For option 01, the “First Bit” occurs 0.5µs after command sync. While “First Word” generally denotes a command word, message recording can begin with a data word when register bit 5 equals 1.</td></tr>
</table>

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Bit No.	Mnemonic	R/W	Reset	Function
7	PKTMR	R/W	0	IMT Packet Timer Mode. When the PKTMR bit is logic 0, the packet timer resets when the IMT is enabled. The packet timer then starts counting when the next MIL-STD-1553 message begins, at detection of the first valid command word (or alternate Start-Record Requirement selected by bits 6-5 below.) If the PKTMR bit is logic 1 when the IMT is enabled, the packet timer resets then immediately starts when the IMT is enabled. In this mode, whenever a data packet is finalized, the packet timer resets then restarts, and new packet recording is immediately started. If enabled, a PKTRDY (packet-ready) interrupt is generated for the host, at packet completion.
6 − 5	MTSRR1:0	R/W	0	IMT Start-Record Requirement 1:0. When register bits 6-5 equal 00, the IMT starts recording a new MIL-STD-1553 message when a **properly encoded, complete MIL-STD-1553 word with command sync** is decoded: The command sync is followed by 16 properly encoded data bits plus a 17th parity bit expressing odd parity. No data is recorded until this condition is met. **This is the usual setting.** (default setting) When register bits 6-5 equal 01, the IMT starts recording a new MIL-STD-1553 message when a **properly encoded, complete MIL-STD-1553 word with command sync or data sync** is decoded. The properly encoded command sync (or data sync) is followed by 16 properly encoded data bits plus a 17th parity bit expressing odd parity. If recording begins with data sync, the Sync Error flag will be set in the Block Status Word. When register bits 6-5 equal 10, the IMT starts recording a new MIL-STD-1553 message upon detection of a **properly encoded command sync with two contiguous data bits**. If the properly encoded command sync with two contiguous data bits does not result in a valid command word, the Invalid Word Error is set in the Block Status Word. This selection begins recording for complete MIL-STD-1553 command words as well as for command word fragments, or command words with bad parity. Under some circumstances, this record option might be helpful for debugging MIL-STD-1553 communication failure. When register bits 6-5 equal 11, the IMT starts recording new bus activity upon detection of **any properly encoded sync (command or data) with two contiguous data bits**. This selection begins recording for complete MIL-STD-1553 command or data words as well as for word fragments, or words with bad parity. If the properly encoded sync with two contiguous data bits does not result in a valid Manchester II word, the Invalid Word Error is set in the Block Status Word. If recording begins with data sync, the Sync Error flag will be set in the Block Status Word. Under some circumstances, this record option might be helpful for debugging MIL-STD-1553 communication failure.

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Bit No.	Mnemonic	R/W	Reset	Function
4	MTCRIW	R/W	0	IMT Continue Recording After Invalid Word. When bit 4 equals 0, the IMT stops recording an incomplete message when an invalid MIL-STD-1553 word is decoded. The invalid word is not stored, and the IMT awaits word detection per register bits 6-5 before the next MIL-STD-1553 message is recorded. (default) When bit 4 equals 1, the MT continues recording an incomplete message when an invalid MIL-STD-1553 word is decoded. The invalid word is stored and the IMT continues monitoring the message until completion or time-out occurs.
3	IMTHTD	R/W	0	IMT (Data Packet) Header and Trailer Disabled. When bit 3 equals 0, the IMT reserves space for an IRIG-106 packet header and packet trailer in the RAM stack assigned in the MT Address List. The Packet Header and Packet Trailer are automatically generated by the device at packet finalization and stored in the assigned stack. (default) When bit 3 equals 1, the IMT generates only the IRIG-106 Packet Body, stored in the assigned stack. The full stack address range is used for message storage.
2	MTXMF	R/W	0	IMT Extended Message Flag Enable. When register bit 2 equals 0, the recorded status/error flags are limited to the defined bits in the IRIG-106 Block Status Word. See Section 14.6. When register bit 2 equals 1, expanded status/error flags are enabled, occupying “reserved” bit positions in the IRIG-106 Block Status Word.
1	IMTCKSM	R/W	0	IMT Checksum Enable This IMT setting is only meaningful when IMTHTD (register bit 3) equals 0, enabling automatic generation of IRIG-106 data packet header and packet trailer. When register bit 1 equals 1, a 16-bit checksum is tallied for the data packet body, and stored in the packet trailer at packet finalization. When register bit 1 equals 0, no checksum is tallied for the data packet body.
0	SMT / $\overline{\text{IMT}}$	R/W	0	Select Simple Monitor Terminal (SMT) or IRIG-106 Monitor Terminal (IMT). This register bit must equal logic 0 for IMT operation. When this bit is zero, the bus monitor operates in IMT IRIG-106 mode with 48-bit time tag counter resolution.

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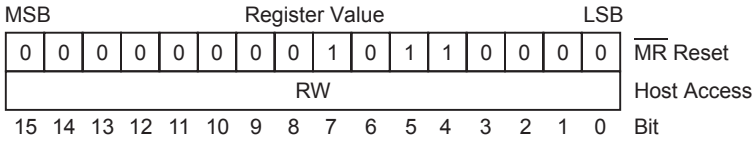
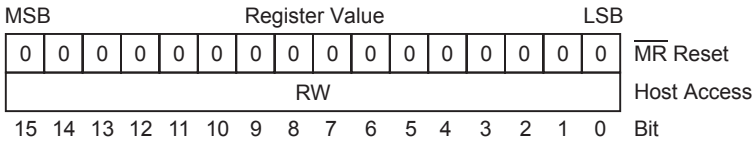
16.2. IMT Bus Monitor Address List Start Address Register (0x002F)



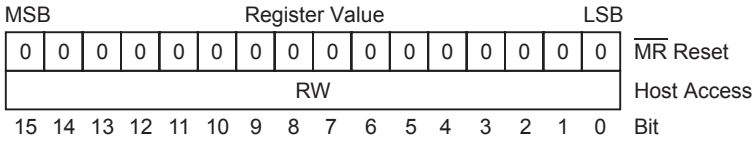
This 16-bit register is Read-Write and is fully maintained by the host. After $\overline{MR}$ pin master reset, this register is initialized with 0x00B0, the default base address of the Monitor Address Table in device RAM. The host can overwrite the default base address. This register is not affected by MT soft reset, when the MTRESET bit is asserted in the Master Status and Reset Register, 0x0001. The Address List for IMT monitor is explained on **page TBD**.

16.3. IMT Bus Monitor Last Message Stack Register (0x0031)



This 16-bit register is read-only **(diagram wrong)** and is updated by the IMT upon completion of a monitored MIL-STD-1553 message. This register is cleared after nMR pin master reset or by MT soft reset, when the MTRESET bit is asserted in the Master Status and Reset Register, 0x0001. This register contains the Block Status Word address in RAM for the last completed MIL-STD-1553 message.

16.4. IMT Bus Monitor Next Message Stack Pointer (0x0030)



This 16-bit register is read-only **(diagram wrong)** and is updated by the IMT after completion of a monitored MIL-STD-1553 message. This register is cleared after nMR pin master reset or by MT soft reset, when the MTRESET bit is asserted in the Master Status and Reset Register, 0x0001. This register contains the RAM address for the next-written Block Status Word, for the next MIL-STD-1553 message. It mirrors the value contained in the Current Address Pointer, word 2 in the Monitor Address List.

The IMT logic only updates this “next message address” register after message completion. Therefore, after reset, this register does not contain a valid pointer address until the next valid message is completed. If the read value equals zero, the “next message address” equals the stack start address.

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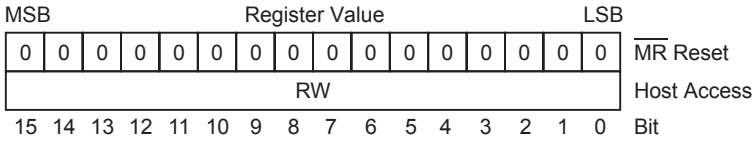
16.5. IMT Packet Maximum Message Count Register (0x002A)



This 16-bit register is read-write and is maintained by the host. This register is cleared after $\overline{MR}$ pin master reset but is not affected by MT soft reset, when the MTRESET bit is asserted in the Master Status and Reset Register, 0x0001.

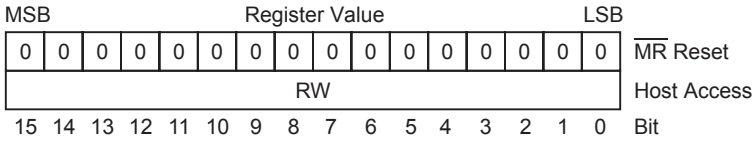
This register only applies when the monitor is configured for IRIG-106 Chapter 10 operational mode, which is when $\overline{IMT}$ bit 0 is initialized to logic 0 in the MT Configuration Register 0x0029. In this mode, monitored message data is stored in "data packets" in the monitor stack. The HI-613x IMT finalizes the unfinished packet when the number of MIL-STD-1553 messages in the packet reaches the value in this register. If register value is zero, this criteria is not used for determination of end-of-packet.

16.5.1. Practical IRIG-106 packet message count considerations

IRIG-106 Chapter 10 stipulates a maximum allowable time interval of 100 ms for any data packet. The maximum number of packet messages occurs when the BC continuously transmits back-to-back broadcast mode code commands without data, each with the minimal allowable intermessage gap of 4 µs, yielding 2 µs dead time between commands. This results in repeating message transmission every 22 µs. Therefore the maximum packet message count is (100 ms / 22 µs) or 4,545 messages occurring in the maximum allowed 100 ms packet interval. Therefore, for strict compliance with IRIG-106, the maximum attainable packet message count is 4,545 decimal.

The HI-613x device can be configured to record packet times exceeding the IRIG-106 limit. Without regard for maximum packet time allowed by IRIG-106, the maximum message count governed by HI-613x RAM capacity is a lower value. If the HI-613x is configured as IMT only, the maximum contiguous RAM space is 0x7FFF – 0x01BF = 0x7E40 = 32,320 words. Maximum message storage space occurs when the HI-613x IMT is configured to provide the data Packet Body, without packet header or trailer. 14 words are used for packet header, leaving 32,306 words for messages. If the BC continuously transmits back-to-back broadcast mode code commands without data, each message consumes 8 words of buffer space. This unlikely repeating message sequence yields the highest packet possible message count for a RAM-limited HI-613x monitor, which is 32,306 / 8 = 4,038 messages. Transmit and receive subaddress commands typically require far more than 8 stored words per MIL-STD-1553 message, so normal bus traffic will probably fill the IMT Stack far in advance of 4,000 messages.

16.6. IMT Packet Maximum 1553 Word Count Register (0x002B)



This 16-bit register is read-write and is maintained by the host. This register is cleared after $\overline{MR}$ pin master reset but is not affected by MT soft reset, when the MTRESET bit is asserted in the Master Status and Reset Register, 0x0001.

This register only applies when the monitor is configured for IRIG-106 Chapter 10 operational mode, which is when $\overline{IMT}$ bit 0 is initialized to logic 0 in the MT Configuration Register 0x0029. In this mode, monitored message data is stored in "data packets" in the monitor stack. The HI-613x IMT finalizes the unfinished packet when the number of 16-bit MIL-STD-1553 message words in the packet reaches the value in this register. This word count is comprised of BC command, RT status and message data words. It excludes IRIG-106 header and trailer (if used) and message block data words and time stamp words. If the register value is zero, this register is not used for determination of end-

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of-packet.

16.6.1. Practical IRIG-106 packet word count considerations

IRIG-106 Chapter 10 stipulates a maximum allowable time interval of 100 ms for any data packet. The maximum number of MIL-STD-1553 packet words occurs when the BC continuously transmits back-to-back 32 data word broadcast receive with 32 data words, each with the minimal allowable intermessage gap of 4 µs, yielding 2 µs dead time between commands. This results in repeating message transmission every 662 µs. Therefore (100 ms / 662 µs) or 151.1 such messages occur in the maximum allowed 100 ms packet interval. Therefore, for strict compliance with IRIG-106, the maximum number of MIL-STD-1553 words in a maximum duration 100 ms IRIG-106 packet is 151.1 messages x 33 words/message = 4,985 words.

The HI-613x permits longer packet recording times than 100 ms. The maximum contiguous RAM space in the device RAM for an IMT Stack buffer is about 32,200 words, achievable when the device is configured as IMT only (no concurrent BC or RTs). To achieve even larger packets, the host can accumulate Packet Body increments read from HI-613x RAM in a separate, larger RAM. The HI-613x would probably be configured without automatic packet header and trailer generation, to record message data in the format shown in Figure 7 “IRIG-106 Message Data Storage” on page 67. Upon completion of each large packet (accumulated from multiple HI-613x “sub-packets”), the host generates the packet header, channel specific data and packet trailer for the accumulated packet data body.

16.7. IMT Maximum Packet Time Register (0x002C)

MSB								Register Value							LSB	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\overline{\text{MR}}$ Reset
RW																Host Access
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit

This 16-bit register is read-write and is maintained by the host. This register is cleared after $\overline{\text{MR}}$ pin master reset but is not affected by MT soft reset, when the MTRESET bit is asserted in the Master Status and Reset Register, 0x0001.

This register only applies when the monitor is configured for IRIG-106 Chapter 10 operational mode, which is when $\overline{\text{IMT}}$ bit 0 is initialized to logic 0 in the MT Configuration Register 0x0029. In this mode, monitored message data is stored in “data packets” in the monitor stack. The HI-613x IMT finalizes the unfinished packet if the packet data recording time (measured in 10 µs increments) reaches the value in this register. If register value is zero, the register is not used for determination of end-of-packet.

16.7.1. Practical IRIG-106 packet time considerations

IRIG-106 Chapter 10 stipulates a maximum packet time of 100 ms. Therefore, for strict compliance with the standard, the maximum count contained in this register would be (100 ms / 10 µs) = 10,000 decimal. The HI-613x device logic allows a maximum packet time greater than 100 ms. If the register contains 0xFFFF, the maximum packet time is 655.35 ms.

16.8. IMT Packet Maximum Gap Time Register (0x002D)

MSB								Register Value							LSB	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\overline{\text{MR}}$ Reset
RW																Host Access
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit

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This 16-bit register is read-write and is maintained by the host. This register is cleared after $\overline{MR}$ pin master reset but is not affected by MT soft reset, when the MTRESET bit is asserted in the Master Status and Reset Register, 0x0001.

This register only applies when the monitor is configured for IRIG-106 Chapter 10 operational mode, which is when $\overline{IMT}$ bit 0 is initialized to logic 0 in the MT Configuration Register 0x0029. In this mode, monitored message data is stored in "data packets" in the monitor stack. If the elapsed time between successive MIL-STD-1553 words (measured in 10 µs increments) reaches the value in this register, the HI-613x IMT finalizes an unfinished packet. The maximum time interval is 655.35ms. The measured interval restarts after each Manchester word, and ends with gap time-out, or detection of the next-occurring valid Manchester word on either bus. Under normal circumstances, this register is used for determination of gaps between MIL-STD-1553 messages, however message fragments containing valid Manchester words also preempt time-out and restart the timer.

16.8.1. Practical IRIG-106 maximum gap time considerations

Word validation occurs about 3us after Manchester word completion. When the programmed value in this register is N, the in-process packet will finalize at (10N + 3) µs, unless a valid Manchester word started before the maximum bus "dead time" of (N-2) x 10 µs. When the stored register value is zero, this register is not used for end-of-packet determination.

Example: This register contains 20 decimal. The resultant maximum allowed bus "dead time" between Manchester words is 180 µs. When gap time exceeds this limit, packet finalization occurs at 203 µs, and (if enabled) MT interrupts occur for Packet Ready and Maximum Gap Time. *A valid Manchester word starting after 180 µs is not included the finalized packet, but may be the first word in the following packet when bits 6-5 in the MT Configuration Register equal 0-0 or 0-1.*

16.9. IMT Packet Header Channel ID Register (0x002E)

MSB							Register Value								LSB	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\overline{MR}$ Reset
RW																Host Access
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit

This 16-bit register is read-write and is maintained by the host. This register is cleared after $\overline{MR}$ pin master reset but is not affected by MT soft reset, when the MTRESET bit is asserted in the Master Status and Reset Register, 0x0001.

This register is only used when the MT is configured for IRIG-106 Chapter 10 operational mode, with automatic packet header and packet trailer generation. That is, when $\overline{IMT}$ bit 0 is initialized to logic 0, and IMTHTD bit 3 is initialized to logic 1 in the MT Configuration Register 0x0029.

The IRIG-106 Chapter 10 packet header includes a 16-bit Channel ID. The value contained in this register is used for the Channel ID field, when generating the packet header. The host must load a nonzero value into this register during initialization because Channel ID of 0x0000 is reserved for computer-generated data packets.

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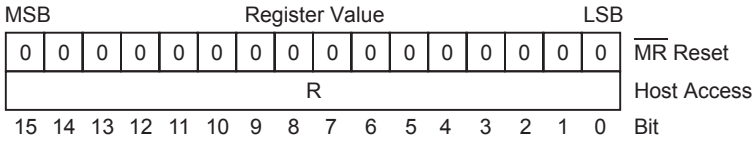
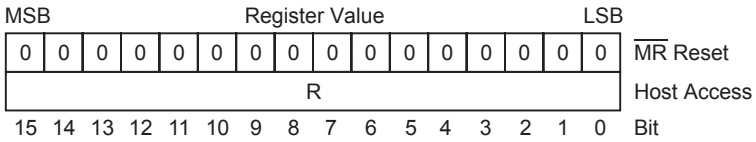
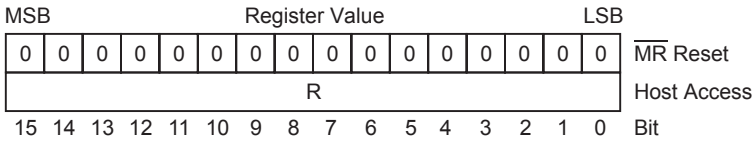
16.10. IMT Monitor Time Tag Count Low Register (0x003A)



16.11. IMT Monitor Time Tag Count Mid Register (0x003B)



16.12. IMT Monitor Time Tag Count High Register (0x003C)



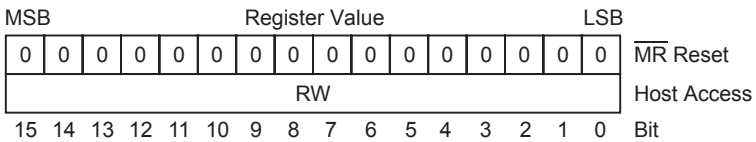
The IMT Bus Monitor always uses a 48-bit time base. The current time base value is reflected in these three 16-bit registers. These registers are read-only and are cleared after $\overline{MR}$ pin Master Reset. Count bits 47-32 reside in register 0x003C, count bits 31-16 reside in register 0x003B while register 0x003A contains bits 15-0.

The host cannot directly write into these registers, but can otherwise control the MT Time Tag count. By writing bits 15-14 in the Time Tag Counter Configuration Register 0x0039, the host can:

- clear the 48-bit time tag count to zero (by loading three 0x0000 values)
- simultaneously copy the 3-register time value into the three IMT Time Tag Utility Registers
- simultaneously load the value contained in the three IMT Time Tag Utility Registers into the IMT Time Tag count registers.

Finally, three IMT Time Tag Match Registers provide capability for generating a host interrupt when the time tag count reaches any predetermined 48-bit value. For further information, refer to the description of the Time Tag Counter Configuration Register 0x0039.

16.13. IMT Time Tag Utility Low Register (0x003D)



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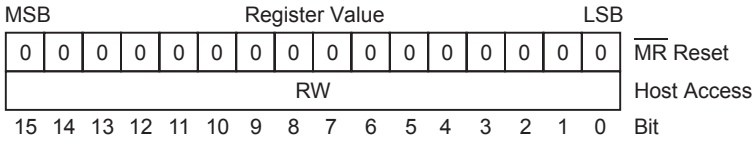
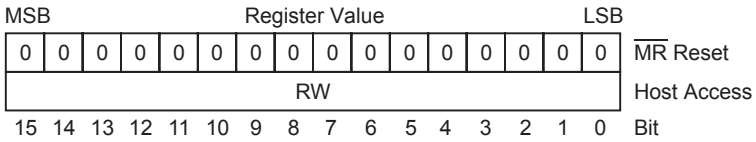
16.14. IMT Time Tag Utility Mid Register (0x003E)



16.15. IMT Time Tag Utility High Register (0x003F)



These multifunction registers are read-write and are cleared after $\overline{MR}$ pin Master Reset. This utility register triplet is used for simultaneously copying a 48-bit value into the three corresponding IMT Time Tag Count Registers. These registers are also used for simultaneously capturing the 48-bit value from the IMT Time Tag Count Registers. Please refer to the description for bits 15-14 in the Time Tag Counter Configuration Register 0x0039 in Section 9.7.

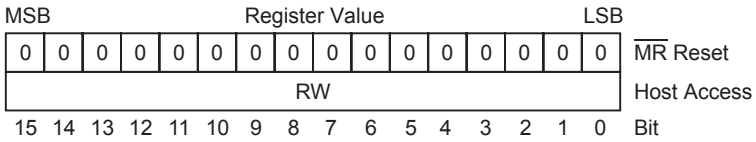
16.15.1. Loading a 48-bit value into the three 16-bit SMT Time Tag Count Registers

When loading or clearing Time Tag count, the 16-bit value in utility register 0x003D is copied into SMT Time Tag Counter register 0x003A. Simultaneously, count bits 47-17 and count bits 31-16 are copied from Time Tag Utility registers 0x003F and 0x003E into SMT Time Tag Counter registers 0x003C and 0x003B.

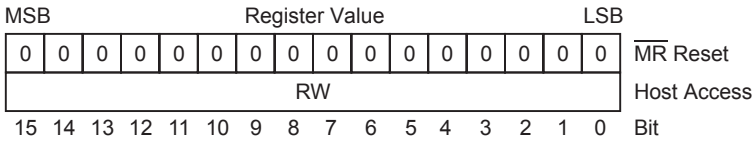
16.15.2. Capturing a 48-bit value from the three 16-bit SMT Time Tag Count Registers

When capturing Time Tag count, the 16-bit value in SMT Time Tag Count register 0x003A is copied into Time Tag Utility Register 0x003D. Simultaneously, count bits 47-17 and count bits 31-16 in SMT Time Tag Count registers 0x003C and 0x003B are copied into Time Tag Utility registers 0x003F and 0x003E respectively.

16.16. IMT Time Tag Match Low Register (0x0040)



16.17. IMT Time Tag Match Mid Register (0x0041)



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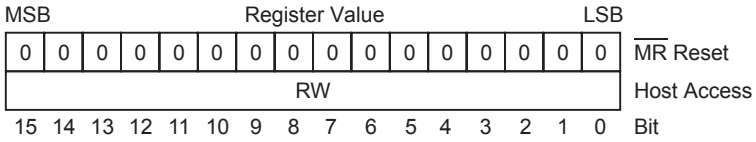
16.18. IMT Time Tag Match High Register (0x0042)



These registers are read-write and are cleared after $\overline{MR}$ pin Master Reset. When the MTTTM bit 6 is logic 1 in the Hardware Interrupt Enable Register 0x000F, an interrupt occurs when the value stored in this register triplet matches the 48-bit value in the IMT Time Tag Count Registers.

Please refer to the description for MTTTM bit 6 in the Hardware Interrupt Registers described in Section 9.5.

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16.19. IMT Bus Monitor Interrupt Registers and Their Use

Thirteen HI-613x registers are used for host interrupt management. In addition to the Interrupt Count & Log Address Register described in Section 9.4, there are four 3-register groups, separated by function. One register group is for Hardware interrupts, plus one register group each for Bus Controller, Bus Monitor and Remote Terminal interrupts. The Remote Terminal register set is shared between RT1 and RT2. Each group (BC, MT, RT or Hardware) has

- An Interrupt Enable Register to enable and disable interrupts
- A Pending Interrupt Register to capture the occurrence of enabled interrupts
- An Interrupt Output Enable Register to enable $\overline{IRQ}$ output to host, for pending enabled interrupts

Each individual bit in all three registers is mapped to the same interrupt-causing event when the corresponding interrupt condition is enabled. Numerous interrupt options are available for the IMT. At initialization, bits must be set in the IMT Interrupt Enable register to identify the interrupt-causing events for the IMT which are heeded by the HI-613x. Most Monitor applications only use A subset of available IMT interrupt options. Interrupt-causing events are ignored when their corresponding bits are reset in the IMT Interrupt Enable Register. Setting an Interrupt Enable register bit from 0 to 1 does not trigger interrupt recognition for events that occurred while the bit was zero.

Whenever an enabled monitor interrupt event occurs, the Interrupt Log Buffer is updated and a bit is set in the IMT Pending Interrupt Register. This action takes place only when the corresponding bit is already set in the IMT Interrupt Enable Register. The host can poll the IMT Pending Interrupt Register to detect the occurrence of Monitor interrupts, indicated by non-zero value. When the host reads the IMT Pending Interrupt Register, it automatically clears to 0x0000.

When an enabled interrupt condition occurs and the corresponding bit is also set in the IMT Interrupt Output Enable Register, the $\overline{IRQ}$ output is asserted to alert the host. Thus, the IMT Interrupt Output Enable Register establishes two interrupt priority levels for the Monitor: high priority interrupts generate an nIRQ signal output, while low priority interrupts do not. The host detects low priority interrupts by polling the IMT Pending Interrupt Register.

A single $\overline{IRQ}$ host interrupt output signal is shared by all enabled interrupt conditions having bits set in the four Interrupt Output Enable registers. Multiple interrupt-causing events can occur simultaneously, so each nIRQ output assertion can result from one or several interrupt conditions.

When the host receives an $\overline{IRQ}$ signal from the device, it must identify the event (or events) that triggered the interrupt. A hardware-assisted interrupt-decoding scheme simplifies interrupt identification. This scheme uses the three low order bits in the Hardware Pending Interrupt Register.

Upon $\overline{IRQ}$ interrupt assertion, the host first reads the Hardware Pending Interrupt Register. Bits 15-3 in this register identify hardware interrupt conditions. The three low-order bits the Hardware Pending Interrupt Register indicate zero vs. non-zero status for the RT, MT and BC Pending Interrupt Registers. If any of these bits is logic 1, the corresponding Pending Interrupt Register has one or more interrupt flags set. Any combination of these 3 bits may be set. Each of the four Pending Interrupt registers self-resets to 0x0000 after the host reads its value. Thus, the host should retain the value read from the Hardware Pending Interrupt Register when 2 or more bits are non-zero in the bit 2-0 range.

When MTIP (MT Interrupt Pending) bit 1 is set in the Hardware Pending Interrupt Register, the IMT Pending Interrupt Register contains a nonzero value, so should be read next to identify the specific IMT interrupt event.

When polling the Pending Interrupt registers to identify low priority interrupts that do not assert the nIRQ output, the same method can be applied. At a single read of the Hardware Pending Interrupt Register reveals zero / non-zero status of all four Pending Interrupt registers.

To help the host process interrupts, the HI-613x device maintains information from the 32 most recent interrupts in a 64-word ring buffer in RAM, located at the fixed address range 0x0180 to 0x01BF. Each interrupt stores two information words: the Interrupt Identification Word (IIW) identifies the interrupt type(s) that occurred; the Interrupt Address Word (IAW) identifies the interrupt source. For IMT interrupts, the IAW contains the 16-bit Stack address, pointing to the Block Status Word of the message in which the interrupt event occurred.

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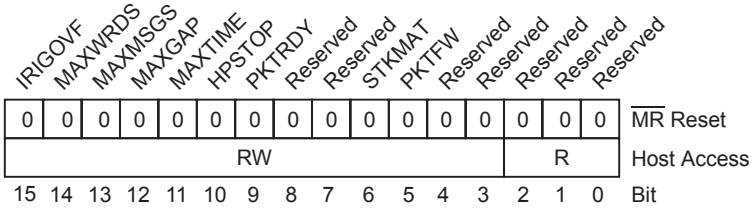
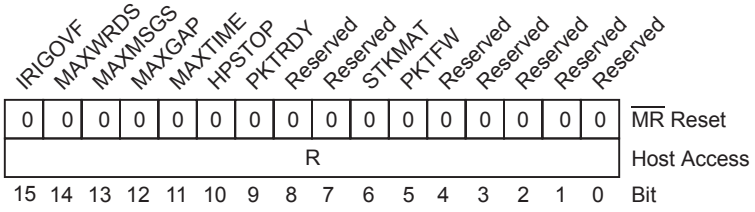
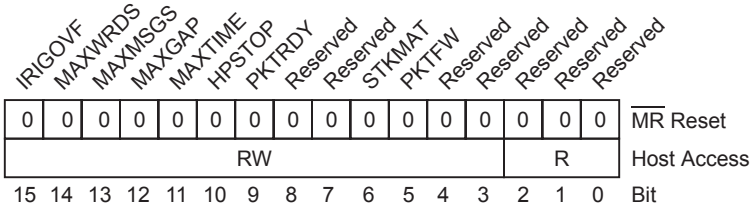
16.19.1. IMT Bus Monitor Interrupt Enable Register (0x0011)



16.19.2. IMT Bus Monitor Pending Interrupt Register (0x0008)



16.19.3. IMT Bus Monitor Interrupt Output Enable Register (0x0015)



These three registers govern IMT interrupt behavior: the IMT Interrupt Enable Register, the IMT Pending Interrupt Register and the IMT Interrupt Output Enable Register. When a bit is set in the IMT Interrupt Enable Register, the corresponding IMT interrupt is enabled. When a bit is reset in this register, the corresponding interrupt event is unconditionally disregarded. Setting a register bit from 0 to 1 does not trigger interrupt recognition for events that occurred while the bit was zero.

When an enabled IMT interrupt event occurs, the corresponding bit is set in the IMT Pending Interrupt Register and the Interrupt Log Buffer is updated. To simplify interrupt decoding, MTIP bit 1 in the Hardware Pending Interrupt Register is also set whenever one or more bits are set in the IMT Pending Interrupt Register.

If the corresponding bit is already set in the IMT Interrupt Output Enable Register, the nIRQ output pin is asserted at Pending Interrupt Register assertion. The IMT Interrupt Output Enable Register establishes two priority levels: high priority interrupts generate an nIRQ output while low priority interrupts do not. Both priority levels update the IMT Pending Interrupt Register and the Interrupt Log Buffer. The host detects low priority (masked) interrupts by polling IMT Pending Interrupt Register.

The table below first describes the common bits 15-3 in all three IMT interrupt registers and then describes register-to-register differences for bits 2-0.

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Bit No.	Mnemonic	Function
15	IRIGOVF	IRIG-106 Stack Overflow. Since start-of-packet, data recording got within 64 words of overwriting the Packet Start Address. The in-process packet terminated at end-of-message. Next message begins next packet.
14	MAXWRDS	IRIG-106 Maximum MIL-STD-1553 Word Count Interrupt. The in-process packet terminated at end-of-message when the number of MIL-STD-1553 message words recorded in the packet attained the maximum word count stored in the MT Packet Maximum MIL-STD-1553 Word Count Register at address 0x002B.
13	MAXMSGS	IRIG-106 Maximum Message Count Interrupt. The in-process packet terminated at end-of-message when the number of recorded MIL-STD-1553 messages equals the maximum message count stored in the IMT Packet Maximum Message Count Register at address 0x002A.
12	MAXGAP	IRIG-106 Maximum Gap Time Exceeded Interrupt. The in-process packet terminated when the bus monitor encountered a MIL-STD-1553 message gap interval exceeding the maximum gap time stored in the MT Packet Maximum Gap Time Register at address 0x002D.
11	MAXTIME	IRIG-106 Maximum Recording Time Exceeded Interrupt. The in-process packet terminated when the bus monitor reached the maximum packet time stored in the MT Maximum Packet Time Register at address 0x002C. When timeout occurs, packet finalization occurs after completion of an unfinished message.
10	HPSTOP	Host Packet Stop Interrupt. The host asserted the PKSTOP bit in the MT Configuration Register to stop the bus monitor. Recording stopped after in-process message completion.
9	PKTRDY	Packet Ready Interrupt. Above register bits 15-10 are logically ORed to derive the state of this bit.
8	Reserved	This bit is not used in IMT monitor mode. It should be initialized logic 0 in the IMT Interrupt Enable Register.
7	Reserved	This bit is not used in IMT monitor mode. It should be initialized logic 0 in the IMT Interrupt Enable Register.
6	STKMAT	Stack Address Match Interrupt. The stack pointer value has reached the interrupt address in Word 3 of the IMT Address List.
5	PKTFW	Packet Fill Warning Interrupt. Host previously initialized Word 7 in the IMT Address List with a word count value, N. The current stack pointer address has reached N words before overwriting the Current Packet Start Address stored in Word 1 of the IMT Address List.
4	Reserved	This bit is not used in IMT monitor mode. It should be initialized logic 0 in the IMT Interrupt Enable Register.
3	Reserved	This bit is not used in IMT monitor mode. It should be initialized logic 0 in the IMT Interrupt Enable Register.

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Bit No.	*Mnemonic*	*Function*
2 − 0	Reserved	Bits 2-0 cannot be written, and read back 000.

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17. SINGLE OR DUAL REMOTE TERMINAL(S) − OVERVIEW

The HI-613x can operate as one or two autonomous MIL-STD-1553 Remote Terminals, requiring minimal host support. When a single Remote Terminal (RT) is enabled, its configuration and operation is nearly identical to the Holt HI-612x integrated circuit. When two RTs are enabled, they operate simultaneously and independently, with the full flexibility of the Holt HI-612x remote terminal architecture. Designated as RT1 and RT2, the configuration registers for the two terminals are completely duplicated, although certain (i.e., interrupt management) registers are shared between the two RTs. Each terminal has its own Descriptor Table, command Illegalization Table and host interrupt configuration.

The discrete input / output pins for the two Remote Terminals are completely duplicated. The following signal pins are provided for Remote Terminals RT1 and RT2:

- RT1 and RT2 Terminal Address 4 - 0 input pins
- RT1 and RT2 Terminal Address Parity input pins
- RT1 and RT2 (Address) Lock input pins
- RT1 and RT2 Enable input pins
- RT1 and RT2 Subsystem Fail input pins
- RT1 and RT2 Mode Code 8 (Reset Remote Terminal) output pins

By writing the Master Status and Reset Register, Remote Terminals RT1 and RT2 can be independently reset using “soft reset”. Either or both RTs can be configured to automatically assert soft reset when a valid “Reset Remote Terminal” mode code command is received. In this configuration, the serial auto-initialization EEPROM should already be programmed with the desired attributes for the two terminals. When a broadcast “Reset Remote Terminal” mode command is received, RT1 and RT2 perform soft reset independently, although the read-from-EEPROM time interval is doubled.

In this section of the data sheet, the Remote Terminal registers are described first, followed by the details for configuring and operating one or both RTs.

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18. REGISTERS USED BY REMOTE TERMINALS RT1 AND RT2

In addition to the registers described here, HI-6131 Remote Terminals RT1 and RT2 also utilize one or more Memory Address Pointer registers (described in Section 9.8) for managing SPI read/write operations. This comment does not apply for parallel bus interface HI-6130 designs.

18.1. Remote Terminal 1 (RT1) Configuration Register (0x0017)
Remote Terminal 2 (RT2) Configuration Register (0x0020)

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td rowspan="4">15 − 14</td><td rowspan="4">RTTO1:0</td><td rowspan="4">R/W</td><td rowspan="4">0</td><td>RT-RT Time Out Select.
This 2-bit field selects the “no response” time-out delay for RT-to-RT receive commands from four available selections:</td></tr>
<tr><td>
<table>
<tr><th>Bit 15:14</th><th>Bus Dead Time</th><th>RT-RT Time Out</th></tr>
<tr><td>00
01
10
11</td><td>15µs
20µs
58µs
138µs</td><td>57µs
62µs
100µs
180µs</td></tr>
</table>
</td></tr>
<tr><td>For RT-RT commands, time out delay is measured per Figure 8 in the RT Validation Test Plan, SAE AS4111. That is, from mid-parity of the receive command to mid-sync of the first received data word. This interval includes 20µs each for the embedded transmit command word and transmit-RT status word within this span.</td></tr>
<tr><td></td></tr>
<tr><td>13</td><td>RTINHA</td><td>R/W</td><td>0</td><td>RT Bus A Inhibit.
If this bit is logic 1, Bus A for this RT is inhibited, as defined by the BSDTXO bit in register 0. The BSDTXO bit offers two options: inhibit transmit and receive, or inhibit only transmit. Setting the RTINHA bit inhibits Bus A for just this RT, while allowing normal Bus A operation by the BC or the other RT.
Note: If this bit is logic 0, Bus A is not inhibited here but its operation may otherwise be globally inhibited by logic 1 at the TXINHA pin, or logic 1 at the TXINHA bit in the Master Status & Reset Register.</td></tr>
<tr><td>12</td><td>RTINHB</td><td>R/W</td><td>0</td><td>RT1 Bus B Inhibit.
If this bit is logic 1, Bus B for this RT is inhibited, as defined by the BSDTXO bit in register 0. The BSDTXO bit offers two options: inhibit transmit and receive, or inhibit only transmit. Setting the RTINHB bit inhibits Bus B for just this RT, while allowing normal Bus B operation by the BC or the other RT.
Note: If this bit is logic 0, Bus B is not inhibited here for this RT but its operation may otherwise be globally inhibited by logic 1 at the TXINHB pin, or logic 1 at the TXINHB bit in the Master Status & Reset Register.</td></tr>
</table>

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Bit No.	Mnemonic	R/W	Reset	Function
11	BCSTINV	R/W	0	Broadcast Commands Invalid. If this bit is high, commands addressed to RT address 31 are treated as invalid: There is no terminal recognition of commands to RT address 31; there is no RT command response, and no status updating for the benefit of following “transmit status” or “transmit last command” mode commands. If this bit is low, commands addressed to RT address 31 are treated as valid broadcast commands.
10	DBCENA	R/W	0	Dynamic Bus Control Enable. When this bit is logic 1, this RT accepts bus control after receiving a valid legal “dynamic bus control” mode command. The RT STEX bit in the Master Configuration Register resets to 0 and the BCSTRT bit in the Master Configuration Register is set to logic 1. If dynamic bus control is allowed, the BCENA input pin and register bit in the Master Configuration Register must both be logic 1, and the bus controller should be fully initialized in advance to permit immediate operation. When this bit is logic 0, the host must perform all actions necessary to change from RT to Bus Controller mode. Typically the RT Descriptor Table is configured to generate an IWA interrupt to alert the host upon receiving a valid legal Dynamic Bus Control mode code command, MC0.
9	UMCINV	R/W	0	Undefined Mode Codes Invalid. This bit determines whether the RT treats undefined mode code commands as valid (default) or invalid commands. This bit applies only to the following undefined mode code commands: • Mode Codes 0 through 15 with T/R bit = 0 • Mode Codes16, 18 and19 with T/R bit = 0 • Mode Codes 17, 20 and 21 with T/R bit = 1 If this bit is low (default state after nMR pin reset) undefined mode code commands are considered valid, and RT response is based on individual mode command settings in the Illegalization Table: If mode command is legal, the RT “responds in form” and updates status. If a mode command is illegal, the RT asserts Message Error status and (if non-broadcast) transmits only its Status Word without associated data word. If this bit is high, undefined mode code commands are treated as invalid: There is no RT recognition of an invalid command, no RT command response, and no status updating for the benefit of following “transmit status” or “transmit last command” mode commands.
8	NOTICE2	R/W	0	Notice 2 Broadcast Data Storage. If this bit is high, the terminal stores data associated with broadcast commands separately from data associated with non-broadcast commands to meet the requirements of MIL-STD-1553B Notice 2. If this bit is low, broadcast command data is stored in the same buffer with data from non-broadcast commands.

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Bit No.	Mnemonic	R/W	Reset	Function
7	SMCP	R/W	0	IMT Extended Message Flag Enable. When register bit 2 equals 0, the recorded status/error flags are limited to the defined bits in the IRIG-106 Block Status Word. See Section 14.6. When register bit 2 equals 1, expanded status/error flags are enabled, occupying “reserved” bit positions in the IRIG-106 Block Status Word.
6	TRXDB	R/W	0	IMT Checksum Enable This IMT setting is only meaningful when IMTHTD (register bit 3) equals 0, enabling automatic generation of IRIG-106 data packet header and packet trailer. When register bit 1 equals 1, a 16-bit checksum is tallied for the data packet body, and stored in the packet trailer at packet finalization. When register bit 1 equals 0, no checksum is tallied for the data packet body.
5	ALTBITW	R/W	0	Select Simple Monitor Terminal (SMT) or IRIG-106 Monitor Terminal (IMT). This register bit must equal logic 0 for IMT operation. When this bit is zero, the bus monitor operates in IMT IRIG-106 mode with 48-bit time tag counter resolution.
4	AUTOBSD	R/W	0	Automatic Bus Shutdown Enable. This bit affects bus shutdown and shutdown override for mode code commands MC20 and MC21. When the AUTOBSD bit is logic 0, the host is responsible for implementing “bus shutdown” when mode code command MC20 is received, as well as implementing “bus shutdown override” when mode code command MC21 is received. See the Master Configuration Register BSDTXO bit for other considerations.
3 − 2	MC17OP1:0	R/W	0	MC17 Sync Option Bits 1:0 If register bits 3-2 equal 11, the data word received with a valid “synchronize” mode command (MC17) is unconditionally loaded into the Time-Tag counter, at address 0x0047 for RT1 or 0x0049 for RT2. For non-broadcast MC17 commands, the counter load occurs before status word transmission. If register bits 3-2 equal 00, the external host assumes responsibility for actions needed to perform “synchronize” duties upon reception of the valid MC17 “synchronize” mode code command, but status transmission automatically occurs. The binary 01 and 10 combinations of register bits 3-2 support certain extended subaddress schemes. If bits 3-2 equal 01, the received data word is automatically loaded into the Time-Tag counter if bit 0 of the received data word equals 0. The counter resides at address 0x0047 for RT1 or 0x0049 for RT2. If bits 3-2 equal 10, the received data word is automatically loaded into the Time-Tag counter if bit 0 of the received data word equals 1. For non-broadcast MC17 commands, the counter load occurs before status word transmission.

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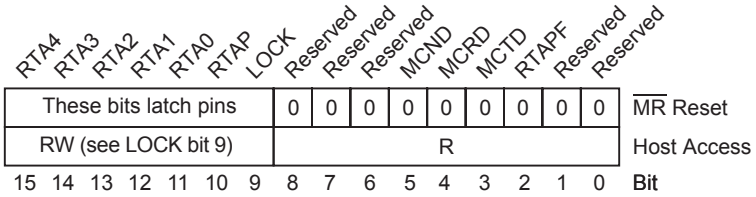
Bit No.	Mnemonic	R/W	Reset	Function
1	MC16OPT	R/W	0	Host reset of “service request” status bit for mode code 16. If this bit is logic 0, reception of a “transmit vector word” mode command (MC16) causes automatic reset of the Service Request status bit. The Service Request bit is reset in the Status Word Bits register before status word transmission begins. If the MCOPT1 bit is logic 1, the external host assumes responsibility for resetting the Service Request bit in the Status Word Bits register.
0	MC8OPT	R/W	0	Automatic soft reset for mode code 8. If this bit is logic 0, reception of a “reset remote terminal” mode command (MC8) causes automatic assertion of SRESET software reset. If non-broadcast mode command, reset occurs after status word transmission is complete. If this bit is logic 1, the external host assumes responsibility for actions needed to perform terminal reset.

18.2. Remote Terminal 1 (RT1) Operational Status Register (0x0018)
Remote Terminal 2 (RT2) Operational Status Register (0x0021)



At rising edge on the $\overline{MR}$ Master Reset input pin, register bits 15-9 capture the logic states (0 or 1) of the corresponding input pins having like names. After reset, register bits 15-9 can be overwritten only if LOCK bit 9 is logic 0. If the register LOCK bit is logic 1, these bits are read-only.

Bits 8-0 are read-only; these bits are cleared after $\overline{MR}$ pin master reset, but are unaffected by assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001).

Bit No.	Mnemonic	R/W	Reset	Function
15 − 11 10	RTA4:0 RTAP	R/W	0	Remote Terminal Address bits 4-0. Remote Terminal Address Parity. These bits reflect the active remote terminal address. They reflect the state of the input pins RTA4 through RTA0 that applied at the rising edge of the $\overline{MR}$ master reset input signal. The RTAP bit, when appended to the remote terminal address bits, provides odd parity. If the register LOCK bit is high, bits 15-10 are read-only. If the register LOCK bit is low, the host can overwrite these bits change the terminal address and parity.

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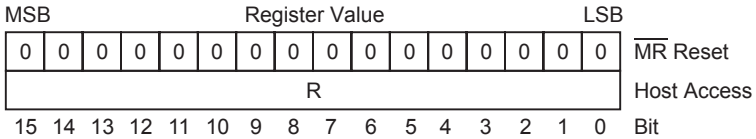
<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>9</td><td>LOCK</td><td>R/W</td><td>0</td><td>Remote Terminal Address Lock.
This bit reflects the state of the LOCK input pin that applied at the rising edge of the $\overline{MR}$ master reset input signal. After reset, the host can overwrite bits 15-9 only if register LOCK bit 9 is logic 0. When the LOCK bit is high, the host cannot overwrite register bits 15-9. To restore host write capability for these bits, the $\overline{MR}$ master reset input signal must first be asserted with the LOCK input pin held low to restore register LOCK bit 9 to logic 0.</td></tr>
<tr><td>8 − 6</td><td>Reserved</td><td>R</td><td>0</td><td>These bits are not used.</td></tr>
<tr><td>5
4
3</td><td>MCND
MCRD
MCTD</td><td>R</td><td>0</td><td>No Data Mode Command Flag.
Receive Data Mode Command Flag.
Transmit Data Mode Command Flag.
These three bits reflect the type of command stored in the RT Current Command Register:
<table>
<tr><th>Current Command Type</th><th>Bits 5-4-3</th><th>Current Command Word</th></tr>
<tr><td>Subaddress, not mode code</td><td>000</td><td>Subaddress, transmit or receive</td></tr>
<tr><td>Mode code, no data word</td><td>100</td><td>MC0 to MC15, T/$\overline{R}$ bit = 1</td></tr>
<tr><td>Mode code, received word</td><td>010</td><td>MC16 to MC31, T/$\overline{R}$ bit = 0</td></tr>
<tr><td>Mode code, transmit word</td><td>001</td><td>MC16 to MC31, T/$\overline{R}$ bit = 1</td></tr>
<tr><td>Mode code, undefined</td><td>111</td><td>MC0 to MC15, T/$\overline{R}$ bit = 0</td></tr>
</table></td></tr>
<tr><td>2</td><td>RTAPF</td><td>R</td><td>0</td><td>Remote Terminal Address Parity Fail.
This bit is set when RT address parity error occurs for the value contained in register bits 15-10. It is low when correct odd parity applies for bits 15-10.</td></tr>
<tr><td>1 − 0</td><td>Reserved</td><td>R</td><td>0</td><td>These bits are not used.</td></tr>
</table>

18.3. Remote Terminal 1 (RT1) Current Command Register (0x0002)
Remote Terminal 2 (RT2) Current Command Register (0x0004)



These 16-bit registers are read-only and are fully maintained by the device. These registers are cleared after $\overline{MR}$ pin master reset, but are unaffected by assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001).

This register contains the last valid command word received by the Remote Terminal over either MIL-STD-1553 bus. This register is updated 5µs after the ACTIVE output is asserted.

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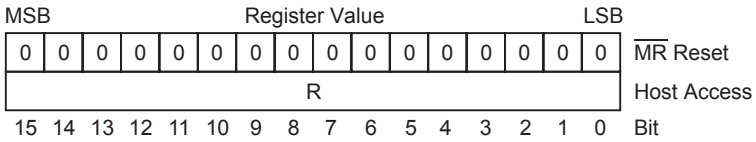
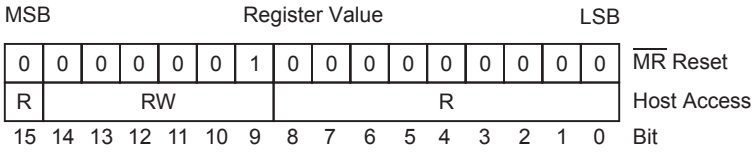
18.4. Remote Terminal 1 (RT1) Current Control Word Address Register (0x0003) Remote Terminal 2 (RT2) Current Control Word Address Register (0x0005)



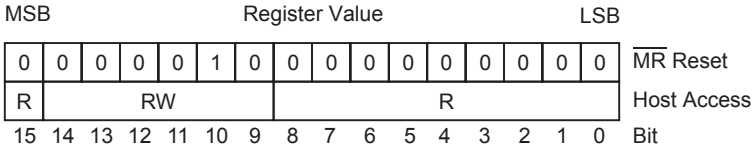
These 16-bit registers are read-only and are fully maintained by the device. These registers are cleared after $\overline{MR}$ pin master reset, but are unaffected by assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001).

These registers contain the address for the descriptor table Control Word corresponding to the current command stored in the Current Command Register, above. These registers are updated 5 µs after the ACTIVE output is asserted for recognition of a valid command for the RT. Also see description for the “Current Message Information Word Address” register.

18.5. Remote Terminal 1 (RT1) Descriptor Table Base Address Register (0x0019) Remote Terminal 2 (RT2) Descriptor Table Base Address Register (0x0022)



Register Address 0x0019 (RT1)



Register Address 0x0019 (RT1)

These 16-bit registers are Read-Write and contain the starting address for the Remote Terminal’s Descriptor Table. These registers are initialized with default values after $\overline{MR}$ pin master reset, or by assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001). For RT1, the post-reset register value is 0x0200. For RT2, the post-reset register value is 0x0400. After initialization, these registers are fully maintained by the host. Bit 15 and bits 8:0 cannot be set and will always read logic 0.

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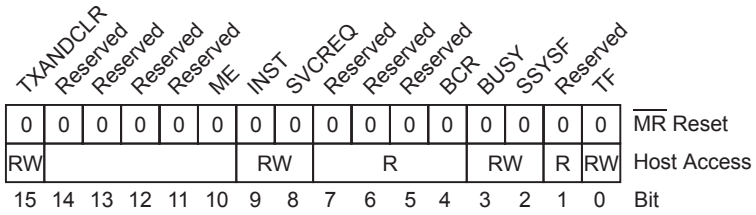
18.6. Remote Terminal 1 (RT1) MIL-STD-1553 Status Word Bits Register (0x001A)
Remote Terminal 2 (RT2) MIL-STD-1553 Status Word Bits Register (0x0023)



These 16-bit registers are Read-Write. With the exception of bits 4 and 10, these registers are maintained by the host. These registers are cleared after $\overline{MR}$ pin master reset, or by assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001).

Register bits 14-10 and 7-4 are read-only. Most of these bits read back zero, except for bits 4 and 10, which are maintained by the device. The remaining bits in the register are Read-Write and are maintained by the host. All bits are active high. Register bits 10-0 are reflected in the outgoing MIL-STD-1553 RT status word. The RT status word reflects the state of host-written register bits until overwritten by the host, unless the Transmit and Clear function (bit 15) is enabled. When set, the Transmit and Clear bit resets itself and bits 9-5 and 3-0 after the next transmitted status word.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	TXANDCLR	R/W	0	Transmit and Clear. When this bit is set, it resets itself and bits 9-5 and 3-0 after the next transmitted status word. This bit does not affect operation of the Transmit Status Word and Transmit Last Command mode codes. Example: Transaction of a valid legal command with the INST and TXANDCLR bits asserted results in status word transmission with the Instrumentation bit set. If the following command is Transmit Status or Transmit Last Command mode code, the Instrumentation bit remains set.
14 − 11	Reserved	R	0	These bits are not used, cannot be written, always read back 000.
10	ME	R	0	Message Error status bit. The device maintains this read-only bit, based on prior message results.
9	INST	R/W	0	Instrumentation status bit. The host maintains this read-write bit.
8	SVCREQ	R/W	0	Service Request status bit. The host maintains this read-write bit.
7 − 5	Reserved	R	0	These bits are not used, cannot be written, always read back 000.
4	BCR	R	0	Broadcast Command Received status bit. The device maintains this read-only bit, based on prior message results.

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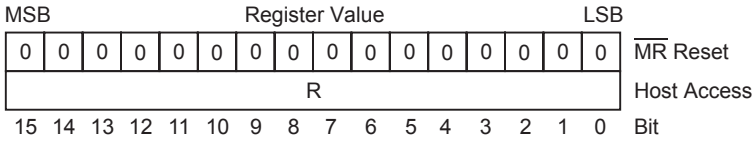
Bit No.	Mnemonic	R/W	Reset	Function
3	BUSY	R/W	0	Busy status bit. The host maintains this read-write bit. When set, the RT asserts its Busy bit in status response for all valid commands. Instead of enabling Busy for all commands, the host can assert Busy status for selected commands by asserting the Busy bit in descriptor table Control Words for the individual commands. When response to a command conveys Busy status, the RT suppresses transmission of data words that would normally accompany status for transmit commands. For messages transacted with Busy status, the WASBUSY flag is asserted in the stored Message Information Word.
2	SSYSF	R/W	0	Subsystem Fail status bit. The host maintains this read-write bit. This register bit is logically ORed with the RT's SSYSF input pin. If either SSYSF register bit or SSYSF pin is asserted, the SSYSF Subsystem Flag status bit is set. If the RT's Configuration Register MCOPT1 bit equals 0, reception of a "transmit vector word" mode command (MC16) causes automatic reset of the SSYSF status bit in this register; when this occurs, the register bit is reset before status word transmission begins.
1	DBC	R	0	Dynamic Bus Control status bit. The host maintains this read-write bit.
0	TF	R/W	0	Terminal Flag status bit. The host maintains this read-write bit. When this bit is asserted, the Terminal Flag status bit is set. If the Terminal Flag bit is set while responding to subaddress transmit commands or mode code commands 16-31 that normally transmit a data word, all data word transmission is suppressed.

18.7. Remote Terminal 1 (RT1) Current Message Information Word Register (0x001B) Remote Terminal 2 (RT2) Current Message Information Word Register (0x0024)



These 16-bit registers are Read-Write and are fully maintained by the device. These registers are cleared after $\overline{MR}$ pin master reset, but are unaffected by assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001). This register contains the data buffer address (assigned in the terminal's Descriptor Table) corresponding to the last decoded valid command' for the Remote Terminal. This register is updated 5µs after the ACTIVE output is asserted.

The value in this register points to the command's Message Information Word (or MIW) in the Descriptor Table, The value of the current command word itself is stored in the Current Command Register for the Remote Terminal, RT1 or RT2.

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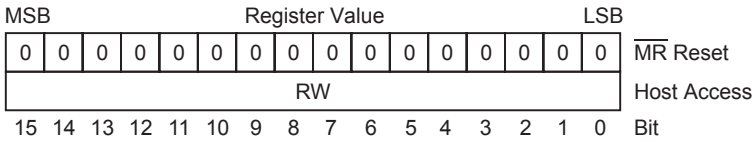
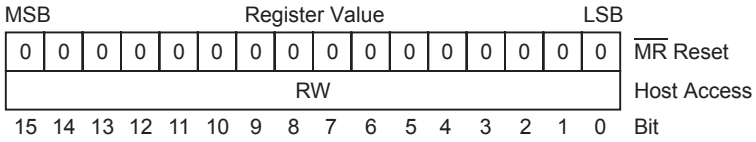
18.8. Remote Terminal 1 (RT1) Bus A Select Register (0x001C)
Remote Terminal 2 (RT2) Bus A Select Register (0x0025)



These 16-bit registers are Read-Write and are fully maintained by the host. These registers are cleared after $\overline{MR}$ pin master reset, but are unaffected by assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001).

The Bus A Select register is only used when the AUTOBSD bit in the RT Configuration Register equals 1. This AUTOBSD setting means the device automatically fulfills mode commands MC20 (decimal) “selected transmitter shutdown” or MC21 “override selected transmitter shutdown”. “Transmitter shutdown” or “shutdown override” can only occur for the inactive bus. If either mode command is received on Bus B, the inactive bus is Bus A. The device compares the received mode data word to the contents of the Bus A Select register to determine whether inactive Bus A is selected for “transmitter shutdown” or “transmitter shutdown override”. (Bus shutdown or shutdown override can only occur for the inactive bus.) If the data word matches the value stored in the Bus A Select register and AUTOBSD equals 1, the device automatically fulfills MC20 “transmitter shutdown” or MC21 “shutdown override” without host assistance: If the mode command received was MC20 (bus shutdown), the Transmit Shutdown A bit in the RT’s BIT (built-in test) Word Register is asserted. If mode command MC21 (override bus shutdown) was received, the Transmit Shutdown A bit in the BIT Word Register is negated.

18.9. Remote Terminal 1 (RT1) Bus B Select Register (0x001D)
Remote Terminal 2 (RT2) Bus B Select Register (0x0026)



These 16-bit registers are Read-Write and are fully maintained by the host. These registers are cleared after $\overline{MR}$ pin master reset, but are unaffected by assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001).

The Bus B Select register is only used when the AUTOBSD bit in the RT Configuration Register equals 1. This AUTOBSD setting means the device automatically fulfills mode commands MC20 (decimal) “selected transmitter shutdown” or MC21 “override selected transmitter shutdown”. “Transmitter shutdown” or “shutdown override” can only occur for the inactive bus. If either mode command is received on Bus A, the inactive bus is Bus B. The device compares the received mode data word to the contents of the Bus B Select register to determine whether inactive Bus B is selected for “transmitter shutdown” or “transmitter shutdown override”. (Bus shutdown or shutdown override can only occur for the inactive bus.) If the data word matches the value stored in the Bus B Select register and AUTOBSD equals 1, the device automatically fulfills MC20 “transmitter shutdown” or MC21 “shutdown override” without host assistance: If the mode command received was MC20 (bus shutdown), the Transmit Shutdown B bit in the RT’s BIT (built-in test) Word Register is asserted. If mode command MC21 (override bus shutdown) was received, the Transmit Shutdown B bit in the BIT Word Register is negated.

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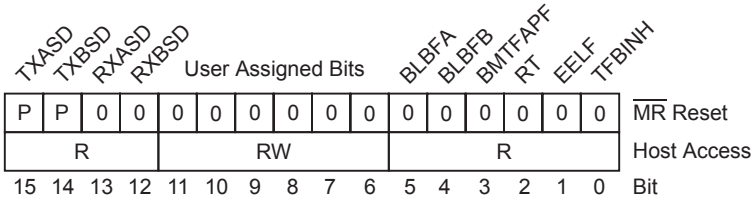
18.10. Remote Terminal 1 (RT1) Built-In Test (BIT) Word Register (0x001E)
Remote Terminal 2 (RT2) Built-In Test (BIT) Word Register (0x0027)



Bits 11-6 in these 16-bit registers are read-write; the remaining bits are read-only. The ten assigned bits are written by the device when predetermined events occur. The host may overwrite the device-written bits 5 and 4. After $\overline{MR}$ pin master reset, bits 13-12, 5-4 and 0 are reset. Bits 15-14 will be set if the corresponding TXINHA or TXINHB input pins are high. Bits 3-1 will be set if RT address parity error, or post-MR memory test failure or auto-initialization failure occurred. These registers are not affected by assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001). Remote terminals RT1 and RT2 use independent BIT Word registers.

If the ALTBITW option bit in the RT Configuration Register is zero when a valid “transmit BIT word” mode command (MC19) is received, the current value in this register is transmitted as the mode data word in the terminal response. The value is also copied to the Remote Terminal’s assigned data buffer for MC19, after mode command fulfillment.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15 14	TXASD TXBSD	R	0	Transmit Bus A Shutdown. Transmit Bus B Shutdown. These read-only bits are set when the corresponding bus transmitter was disabled by assertion of the bus TXINHA or TXINHB input pin, or by fulfillment of a “transmitter shutdown” mode command, either MC4 or MC20. Refer to the description for the BSDTXO bit in the Master Configuration Register (pg xx) and the description for the AUTOBSD bit in the RT Configuration Register for further information.
13 12	RXASD RXBSD	R	0	Receive Bus A Shutdown. Receive Bus B Shutdown. These read-only bits are set when the corresponding bus receiver was disabled concurrently with a bus transmitter by a “transmitter shutdown” mode command MC4 or MC20. Refer to the description for the BSDTXO bit in the Master Configuration Register (Section 9.1) and the description for the AUTOBSD bit in the RT Configuration Register for further information.
11 − 6	----------	R/W	0	User assigned bits.
5 4	BLBFA BLBFB	R	0	Bus A Loopback Fail. Bus B Loopback Fail. These read-only bits are set if Bus A or Bus B loopback failure occurs during self-test.
3	BMTF	R	0	BIST Memory Test Fail. This bit is set if error occurs during built-in self-test for device Random Access Memory (RAM).

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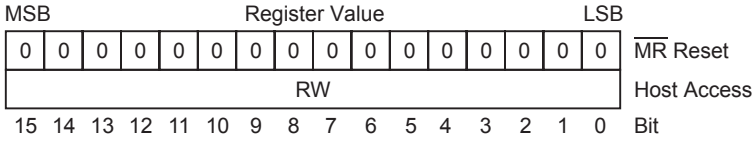
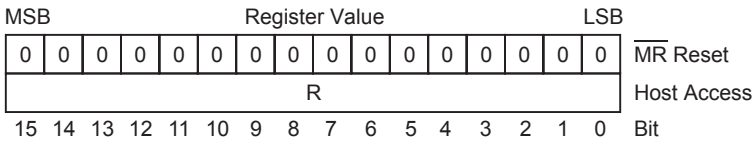
Bit No.	Mnemonic	R/W	Reset	Function
2	RTAPF	R	0	RT Address Parity Fail. This bit is asserted when an RT1 or RT2 Operational Status Register bits 15:10 reflect parity error. After $\overline{MR}$ master reset, bits 15:10 in the RT's Operational Status Register reflect input pin states, but will be overwritten if subsequent auto-initialization is performed (if AUTOEN pin is high) and the initialization EEPROM contains different data for RT Operational Status Register bits 15:10.
1	EELF	R	0	Auto-Initialization EEPROM Load Fail. This bit only applies when auto-initialization is enabled (AUTOEN input pin state equals 1). This bit is set if, after $\overline{MR}$ master reset, failure occurs when copying serial EEPROM to registers and RAM. When this occurs, bit 0 or bit 1 will be set in the RT's Operational Status Register (0x0002) to indicate type of failure.
0	TFBINH	R	0	This bit is set when the Terminal Flag status bit is disabled while fulfilling an "inhibit terminal flag bit" mode code command (MC6). This bit is reset if terminal flag status bit disablement is cancelled later by an "override inhibit terminal flag bit" mode code command (MC7).

18.11. Remote Terminal 1 (RT1) Alternate Built-In Test (BIT) Word Register (0x001F)
Remote Terminal 2 (RT2) Alternate Built-In Test (BIT) Word Register (0x0028)



This 16-bit register is Read-Write and is fully maintained by the host. This register is cleared after $\overline{MR}$ pin master reset. It is not affected by assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001). If the ALTBITW option bit in the RT Configuration Register equals one when a valid "transmit BIT word" mode command (MC19) is received, the current value in this register is transmitted as the mode data word in the terminal response. The value is also copied to the assigned data buffer for MC19, after mode command fulfillment.

18.12. Remote Terminal 1 (RT1) Time Tag Counter Register (0x0049)
Remote Terminal 2 (RT2) Time Tag Counter Register (0x004B)



This register is read-only and is cleared after $\overline{MR}$ pin Master Reset or assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001). Reads to this register address return the current value of the free running 16-bit Time Tag counter. Counter resolution is programmed by the TTCK2:0 bits in the Time Tag Configuration Register. Options are: 2, 4, 8, 16, 32 and 64µs, or externally provided clock. The same clock source is shared by RT1, RT2 and the BC.

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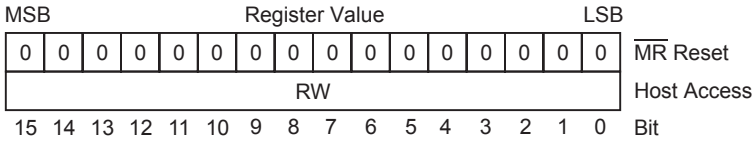
The device automatically resets the Time-Tag Counter when a “synchronize” mode command without data (MC1) is received. In addition, the host can reset, load or capture the Time Tag count at any time by asserting action bits in the Time Tag Configuration Register. Load and capture operations utilize the RT Time Tag Utility Registers, described below.

The MC17OP1:0 bits in the Remote Terminal Configuration Registers allow automatic loading of Time-Tag count using the data word received with a “synchronize with data” mode command, MC17. If both of these bits equal one, the data word received with a valid “synchronize” mode command (MC17) is unconditionally loaded into the Time-Tag counter. For non-broadcast MC17 commands, the counter load occurs before status word transmission. If both MC17OP1 and MC17OP0 bits equal 0, the external host assumes responsibility for actions needed to perform “synchronize” duties upon reception of the valid MC17 “synchronize” command, but status transmission occurs automatically.

The binary 01 and 10 combinations of these bits support certain extended subaddressing schemes. If the MC17OP1:0 bits equal 01, the received data word is automatically loaded into the Time-Tag counter if the low order bit of the received data word (bit 0) equals 0. If the MC17OP1:0 bits equal 10, the received data word is automatically loaded into the Time-Tag counter if the low order bit of the received data word (bit 0) equals 1. For non-broadcast MC17 commands, the counter is loaded before status word transmission.

18.13. Remote Terminal 1 (RT1) Time Tag Utility Register (0x004A) Remote Terminal 2 (RT2) Time Tag Utility Register (0x004C)



These 16-bit registers are Read-Write and are fully maintained by the host. These registers are cleared after $\overline{MR}$ pin master reset, but are not affected by assertion of RTxRESET remote terminal software reset in the Master Status and Reset Register (0x0001). These registers have two functions associated with the two free-running Remote Terminal Time Tag Counters:

18.13.1. RT Time Tag Counter Loading

When the RT1TTA1-0 bits 9-8 in Time Tag Counter Configuration Register 0x0039 are written to 1-0, the value contained in the RT1 Time Tag Utility Register (0x0048) is loaded into the RT1 Time Tag Counter (0x0047).

When the RT2TTA1-0 bits 11-10 in Time Tag Counter Configuration Register 0x0039 are written to 1-0, the value contained in the RT2 Time Tag Utility Register (0x0049) is loaded into the RT2 Time Tag Counter (0x004A).

18.13.2. RT Time Tag Count Match Interrupts

If the RT1TTM or RT2TTM interrupts are enabled in the Hardware Interrupt Enable Register (0x000F), then time tag “count match” interrupts are enabled. When enabled for RT1, the hardware RT1TTM interrupt occurs when the free running RT1 Time Tag Counter (0x0047) matches the value contained in the RT1 Time Tag Utility Register (0x0048).

When enabled for RT2, the hardware RT2TTM interrupt occurs when the free running RT2 Time Tag Counter (0x0049) matches the value contained in the RT2 Time Tag Utility Register (0x004A).

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18.14. RT1 and RT2 Remote Terminal Interrupt Registers and Their Use

Thirteen HI-613x registers are used for host interrupt management. In addition to the Interrupt Count & Log Address Register described in Section 9.4, there are four 3-register groups, separated by function. One register group is for Hardware interrupts, plus one register group each for Bus Controller, Bus Monitor and Remote Terminal interrupts. The Remote Terminal register set is shared between RT1 and RT2. Each group (Hardware, BC, MT or RT) has

- An Interrupt Enable Register to enable and disable interrupts
- A Pending Interrupt Register to capture the occurrence of enabled interrupts
- An Interrupt Output Enable Register to enable $\overline{\text{IRQ}}$ output to host, for pending enabled interrupts

Each individual bit in all three registers is mapped to the same interrupt-causing event when the corresponding interrupt condition is enabled. Numerous interrupt options are available for the RT. At initialization, bits must be set in the RT Interrupt Enable register to identify the interrupt-causing events for the RT which are heeded by the HI-613x. Most Monitor applications only use A subset of available RT interrupt options. Interrupt-causing events are ignored when their corresponding bits are reset in the RT Interrupt Enable Register. Setting an Interrupt Enable register bit from 0 to 1 does not trigger interrupt recognition for events that occurred while the bit was zero.

Whenever an enabled monitor interrupt event occurs, the Interrupt Log Buffer is updated and a bit is set in the RT Pending Interrupt Register. This action takes place only when the corresponding bit is already set in the RT Interrupt Enable Register. The host can poll the RT Pending Interrupt Register to detect the occurrence of Monitor interrupts, indicated by non-zero value. When the host reads the RT Pending Interrupt Register, it automatically clears to 0x0000.

When an enabled interrupt condition occurs and the corresponding bit is also set in the RT Interrupt Output Enable Register, the $\overline{\text{IRQ}}$ output is asserted to alert the host. Thus, the RT Interrupt Output Enable Register establishes two interrupt priority levels for the Monitor: high priority interrupts generate an $\overline{\text{IRQ}}$ signal output, while low priority interrupts do not. The host detects low priority interrupts by polling the RT Pending Interrupt Register.

A single $\overline{\text{IRQ}}$ host interrupt output signal is shared by all enabled interrupt conditions having bits set in the four Interrupt Output Enable registers. Multiple interrupt-causing events can occur simultaneously, so each $\overline{\text{IRQ}}$ output assertion can result from one or several interrupt conditions.

When the host receives an $\overline{\text{IRQ}}$ signal from the device, it must identify the event (or events) that triggered the interrupt. A hardware-assisted interrupt-decoding scheme simplifies interrupt identification. This scheme uses the three low order bits in the Hardware Pending Interrupt Register.

Upon $\overline{\text{IRQ}}$ interrupt assertion, the host first reads the Hardware Pending Interrupt Register. Bits 15-3 in this register identify hardware interrupt conditions. The three low-order bits the Hardware Pending Interrupt Register indicate zero vs. non-zero status for the RT, MT and BC Pending Interrupt Registers. If any of these bits is logic 1, the corresponding Pending Interrupt Register has one or more interrupt flags set. Any combination of these 3 bits may be set. Each of the four Pending Interrupt registers self-resets to 0x0000 after the host reads its value. Thus, the host should retain the value read from the Hardware Pending Interrupt Register when 2 or more bits are non-zero in the bit 2-0 range.

When MTIP (MT Interrupt Pending) bit 1 is set in the Hardware Pending Interrupt Register, the RT Pending Interrupt Register contains a nonzero value, so should be read next to identify the specific RT interrupt event.

When polling the Pending Interrupt registers to identify low priority interrupts that do not assert the $\overline{\text{IRQ}}$ output, the same method can be applied. At a single read of the Hardware Pending Interrupt Register reveals zero / non-zero status of all four Pending Interrupt registers.

To help the host process interrupts, the HI-613x device maintains information from the 32 most recent interrupts in a 64-word ring buffer in RAM, located at the fixed address range 0x0180 to 0x01BF. Each interrupt stores two information words: the Interrupt Identification Word (IIW) identifies the interrupt type(s) that occurred; the Interrupt Address Word (IAW) identifies the interrupt source. For RT interrupts, the IAW contains a 16-bit address in the RT1 or RT2 Descriptor Table, pointing to the Command Word used in the message in which the interrupt occurred.

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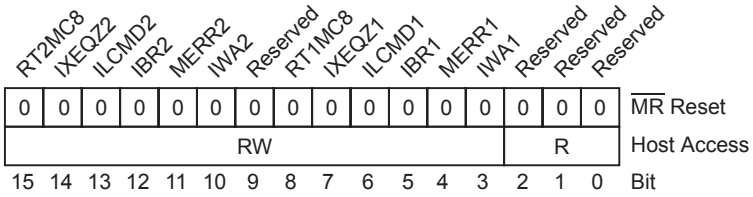
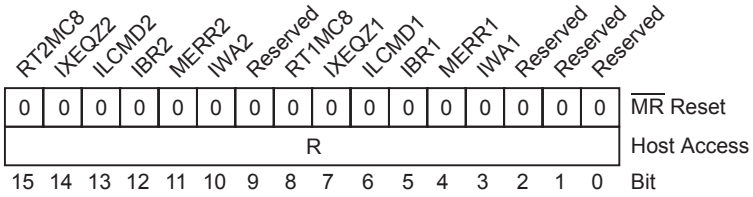
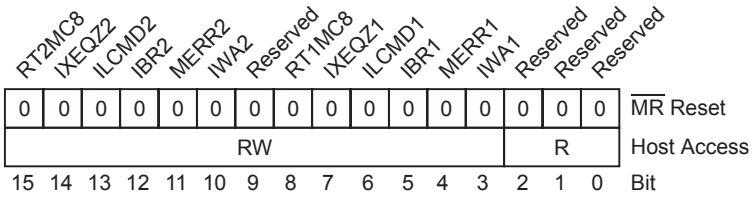
18.14.1. Remote Terminal (RT) Interrupt Enable Register (0x0012)



18.14.2. Remote Terminal (RT) Pending Interrupt Register (0x0009)



18.14.3. Remote Terminal (RT) Interrupt Output Enable Register (0x0016)



Three registers govern RT interrupt behavior: the RT Interrupt Enable Register, the RT Pending Interrupt Register and the RT Interrupt Output Enable Register. When a bit is set in the RT Pending Interrupt Enable Register, the corresponding RT interrupt is enabled. When a bit is reset in this register, the corresponding interrupt event is unconditionally disregarded. Setting a register bit from 0 to 1 does not trigger interrupt recognition for events that occurred while the bit was zero.

When an enabled RT interrupt event occurs, the corresponding bit is set in the Pending RT Interrupt Register and the Interrupt Log Buffer is updated. To simplify interrupt decoding, RTIP bit 2 in the Hardware Pending Interrupt Register is also set whenever a message sets at least one bit in the RT Pending Interrupt Register.

If the corresponding bit is set in the RT Interrupt Output Enable Register, the $\overline{IRQ}$ output is asserted at message completion. The RT Interrupt Output Enable Register establishes two priority levels: high priority interrupts generate an nIRQ output while low priority interrupts do not. Both priority levels update the Pending Interrupt Register and Interrupt Log Buffer. The host can detect low priority (masked) interrupts by polling Pending Interrupt registers.

The following table describes the shared bit descriptions used by all three RT interrupt registers.

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Bit No.	*Mnemonic*	*Function*
15	RT2MC8	RT2 Mode Code 8 Command Interrupt. Remote terminal RT2 processed a valid MIL-STD-1553 “reset remote terminal” mode code command. An RTxMC8 interrupt notifies the host when the Bus Controller commands remote terminal reset. The state of bit 0 in the RT2 Remote Terminal Configuration Register 0x0020 determines whether the mode code response is automatic or handled by the host. If the RT2MC8 bit is reset in the RT Interrupt Enable register when RT2 decodes a valid “reset remote terminal” mode command, bit 0 in the RT2 Remote Terminal Configuration Register dictates whether the reset response is automatic, or host controlled. The event does not affect the RT Pending Interrupt Register, the Interrupt Log or the nIRQ output, but the nRT2MC8 output pin is asserted to indicate that RT2 needs reset. In the case of a broadcast command to RT31, both MC8 pins will be asserted.
14	IXEQZ2	RT2 Index Equals Zero Interrupt. The “index equals zero” (IXEQZ) interrupt for RT2. Index counts are used in multi-message bulk data transfers. “Index equals zero” occurs when the last expected message was transacted. Defined IXEQZ interrupt events comprise: (a) subaddresses using indexed buffer mode when the index decrements from 1 to 0, or (b) subaddresses using circular buffer modes when the pre-determined number of messages has been transacted.
13	ILCMD2	RT2 Illegal Command Interrupt. The Remote Terminal 2 encountered a valid illegal message, as defined in the RT2 Illegal Command Table. Illegal commands are detected when a new valid command word is decoded and the RT2 Illegalization Table bit corresponding to the received command is logic 1. (Table bits are logic 0 for legal commands.) The RT2 Illegalization Table contains nonzero values only when “illegal command detection” is being applied. When illegal commands are received, RT2 responds by transmitting a status word with ME “message error” flag set; no data words are transmitted. If the ILCMD2 bit is reset in the RT Interrupt Enable Register when a valid illegal command is decoded, the event does not affect the RT Pending Interrupt Register, the Interrupt Log or the $\overline{\text{IRQ}}$ output.
12	IBR2	RT2 Broadcast Command Received Interrupt. Broadcast commands are enabled for Remote Terminal 2 and the terminal encountered a valid command addressed to RT31, the broadcast command address.
11	MERR2	RT2 Message Error Status Interrupt. The Remote Terminal 2 set its Message Error status flag while processing a valid MIL-STD-1553 message. Message errors are caused by Manchester encoding problems or protocol errors.
10	IWA2	RT2 Interrupt When Accessed. The Remote Terminal 2 processed a valid MIL-STD-1553 command having the IWA interrupt enabled in its RT2 Descriptor Table entry. IWA interrupts are used to notify the host each time certain command words are encountered.
9	Reserved	Bit 9 cannot be written and reads back logic 0.

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Bit No.	*Mnemonic*	*Function*
8	RT1MC8	RT1 Mode Code 8 Command Interrupt. Remote terminal RT1 processed a valid MIL-STD-1553 “reset remote terminal” mode code command. An RTxMC8 interrupt notifies the host when the Bus Controller commands remote terminal reset. The state of bit 0 in the RT1 Remote Terminal Configuration Register 0x0017 determines whether the mode code response is automatic or handled by the host. If the RT1MC8 bit is reset in the RT Interrupt Enable register when RT1 decodes a valid “reset remote terminal” mode command, bit 0 in the RT1 Remote Terminal Configuration Register dictates whether the reset response is automatic, or host controlled. The event does not affect the RT Pending Interrupt Register, the Interrupt Log or the nIRQ output, but the nRT1MC8 output pin is asserted to indicate that RT1 needs reset. In the case of a broadcast command to RT31, both MC8 pins will be asserted.
7	IXEQZ1	RT1 Index Equals Zero Interrupt. The “index equals zero” (IXEQZ) interrupt for RT1. Index counts are used in multi-message bulk data transfers. “Index equals zero” occurs when the last expected message was transacted. Defined IXEQZ interrupt events comprise: (a) subaddresses using indexed buffer mode when the index decrements from 1 to 0, or (b) subaddresses using circular buffer modes when the pre-determined number of messages has been transacted.
6	ILCMD1	RT1 Illegal Command Interrupt. The Remote Terminal 2 encountered a valid illegal message, as defined in the RT1 Illegal Command Table. Illegal commands are detected when a new valid command word is decoded and the RT1 Illegalization Table bit corresponding to the received command is logic 1. (Table bits are logic 0 for legal commands.) The RT1 Illegalization Table contains nonzero values only when “illegal command detection” is being applied. When illegal commands are received, RT1 responds by transmitting a status word with ME “message error” flag set; no data words are transmitted. If the ILCMD2 bit is reset in the RT Interrupt Enable Register when a valid illegal command is decoded, the event does not affect the RT Pending Interrupt Register, the Interrupt Log or the $\overline{\text{IRQ}}$ output.
5	IBR1	RT1 Broadcast Command Received Interrupt. Broadcast commands are enabled for Remote Terminal 1 and the terminal encountered a valid command addressed to RT31, the broadcast command address.
4	MERR1	RT1 Message Error Status Interrupt. The Remote Terminal 1 set its Message Error status flag while processing a valid MIL-STD-1553 message. Message errors are caused by Manchester encoding problems or protocol errors.
3	IWA1	RT1 Interrupt When Accessed. The Remote Terminal 1 processed a valid MIL-STD-1553 command having the IWA interrupt enabled in its RT1 Descriptor Table entry. IWA interrupts are used to notify the host each time certain command words are encountered.
2 − 0	Reserved	Bits 2-0 cannot be written, and read back 000.

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19. REMOTE TERMINAL RT1 AND RT2 CONFIGURATION AND OPERATION

19.1. Command Responses

A brief review of MIL-STD-1553 commands and responses is appropriate here to establish terminology used in the rest of this data sheet. Shown in Figure 11, each command word is comprised of a sync field, three 5-bit data fields, a single bit denoting Transmit / Receive direction and ends with a parity bit. The hardware decoder uses the sync field to determine word type (command vs. data). Word validity is based on proper sync encoding, Manchester II encoding, correct bit count and correct odd parity for the 16 data bits. Once a valid word with command sync is found, the sync and parity are stripped before the command's 16 data bits are stored for further processing.

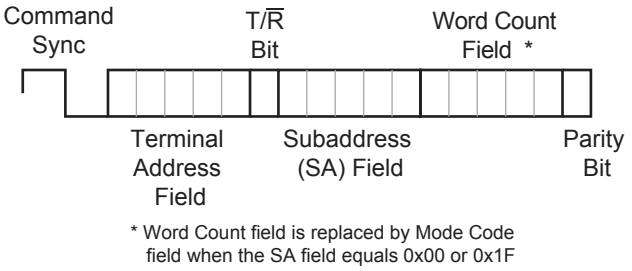

Figure 11. MIL-STD-1553 Command Word Structure

A "valid command" can be specifically addressed to the individual HI-6130 terminal (the command word's embedded Terminal Address field matches the terminal address latched in the Operational Status register) or can be a "broadcast command" addressed to all terminals. Broadcast commands are always addressed to RT address 31 (0x1F). In systems where broadcast commands are disallowed, RT31 is not used as a conventional terminal address. When set, the BCSTINV bit in Configuration Register 1 renders RT31 commands as "invalid": broadcast commands are indistinguishable from commands addressed to other terminals. Invalid commands are simply disregarded.

When the command word's 5-bit SA (subaddress) field is in the range of 1 to 30 (0x01 to 0x1E) the command is considered a "subaddress command". The terminal will either receive or transmit data words, and "direction" is specified by the command's T/$\overline{R}$ bit. The number of data words transacted is specified in the 5-bit word count field, ranging from 1 to 32 words. Thirty-two data words is represented when the word count field equals 0x00.

When the command's 5-bit subaddress field equals 0 or 31 (0x1F) a "mode code" command is indicated; the low order five bits no longer specify a word count, instead they convey a mode code value. This data sheet refers to mode code commands by the mode code number. For example, a mode command with 5-bit mode code field of 0x10 is called MC16, and the full range of mode code values is MC0 through MC31 (decimal).

Mode codes MC16 through MC31 (0x10 through 0x1F) have a single associated data word. When the command T/$\overline{R}$ bit equals 0, the data word is contiguous with the command word and received by the RT. When the command's T/$\overline{R}$ bit equals 1, the data word is transmitted by the RT, following the terminal's transmitted status word.

Mode codes MC0 through MC15 (0x0F) do not have associated data words. For these 16 commands, the command T/$\overline{R}$ bit does not specify "direction". These commands must be transmitted with T/$\overline{R}$ bit equal to 1. If the T/$\overline{R}$ bit is 0, the mode command is "undefined".

Twenty-two mode commands are "undefined mode commands " in MIL-STD-1553B:

Mode Codes 0 through 15 with T/R bit = 0
Mode Codes16, 18 and19 with T/R bit = 0
Mode Codes 17, 20 and 21 with T/R bit = 1

The UMCINV bit in Configuration Register 1 determines how these undefined mode commands are handled by the HI-6130/31. If the UMCINV configuration bit equals 1, the undefined mode commands are treated as invalid. They are not recognized by the device. There is no terminal response and status is not updated. If the UMCINV configuration bit equals 0, the 22 undefined mode commands are considered valid; this is the default condition following reset. For this case, terminal response depends on whether or not the application uses "illegal command detection."

If illegal command detection is not used, all Illegalization Table entries should be logic 0, including the 22 entries for these undefined commands. (The Illegalization Table is fully described in Section 19.2 on page 160. After $\overline{MR}$ reset, all entries equal logic 0.) The terminal responds "in form", transmitting clear status (and a single mode data word if the command is MC17, MC20 or MC21 with T/$\overline{R}$ bit = 1). Terminal status is updated.

If illegal command detection applies, the Illegalization Table entries for these 22 undefined commands should be initialized to logic 1. In this case, the terminal will respond with status word only, with Message Error bit set.

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No mode data word is transmitted. Terminal status is updated.

Twenty-seven mode codes are considered “reserved” in MIL-STD-1553B:

Mode Codes 9 through 15 with T/R bit = 1
Mode Codes 22 through 31 with T/R bit = 1
Mode Codes 22 through 31 with T/R bit = 0

Treatment of these reserved mode commands depends on their respective Illegalization Table entries. As described above for undefined mode commands, response depends on whether or not illegal command detection applies.

Any mode commands not implemented in the HI-6130/31 terminal should be treated the same as reserved mode commands. For example, command MC0 (with T/$\overline{R}$ = 1) is probably unimplemented because the HI-6130 does not have provisions for accepting “dynamic bus control”.

The important point is that “illegal command detection” should be universally applied (or not applied) when setting up a HI-6130/31 Remote Terminal application. Here are the two options:

Not using Illegal command detection. The HI-6130/31 Illegalization Table is left in its default state (all locations equal to $\overline{MR}$ post-reset 0x0000). The terminal responds “in form” to all valid commands, whether legal or illegal.

Using illegal command detection. The HI-6130/31 Illegalization Table is initialized by the host to implement “illegal command detection”. The host sets bits for all illegal commands. This generally includes the reserved and unimplemented mode commands, unimplemented subaddresses (or specific word counts, T/$\overline{R}$ bit states, and/or broadcast vs. non-broadcast status within subaddresses). Treatment for the undefined mode commands depends on UMCINV bit.

The host defines terminal response for all individual commands by initializing the Descriptor Table, fully described later. At this point, a few comments about the Descriptor Table are appropriate.

The command SA (subaddress) field has a range of 0 to 31 (0x1F). When SA is in the range 1 to 30 (0x1E), the command is a transmit or receive “subaddress command”. The number of data words transmitted or received is expressed in the low order 5 bits. When SA equals 0 or 31 (0x1F) the command is a mode command and the mode code value is expressed in the low order 5 bits.

For each subaddress, separate table “descriptor blocks” for transmit and receive commands permit different data buffering to be applied. The host initializes the table so each transmit-subaddress and each receive-subaddress uses one of four methods for storing message data. During table initialization, memory is allocated in shared RAM for storing message data according to the application requirements. Each transmit-subaddress and receive-subaddress has one or more data pointers (depending on buffer method) addressing its reserved data buffer(s).

Each mode command also has its own table “descriptor block”. Mode commands have either one data word or no associated data words. Descriptor words used as data pointers by “subaddress commands” are instead used for direct storage of transacted mode data words. Mode commands that transmit or receive mode data words have a dedicated storage address range in shared RAM, eliminating the need for descriptor table data pointers.

Each mode command with mode data word has its own fixed address for data storage. This includes reserved mode codes with data word. Thus the HI-6130/31 can respond consistently for all mode commands; transmitted data values for “in form” responses (when “illegal command detection” is not used) can be predetermined, even for the reserved mode commands.

19.1.1. RT to RT Commands.

The MIL-STD-1553 standard allows for data word transmission from a specified transmitting terminal to a different receiving terminal. When broadcast commands are allowed, data transmission can be addressed to the broadcast terminal address, RT31. If broadcast is allowed, the host should initialize the BCSTINV (broadcast invalid) bit in Configuration Register 1 to logic 0.

All RT to RT commands are characterized by a pair of contiguous command words: Command Word 1 is a receive command addressed to the intended receiving terminal, then Command Word 2 is a transmit command addressed to a single transmitting terminal. Command Word 2 cannot be broadcast address RT31. The HI-6130 automatically detects and handles RT to RT commands, except when either command word contains a subaddress field equal to 0x0 or 0x1F. Either subaddress value indicates a mode code command; the device treats RT to RT commands with mode code as invalid. If either RT-RT command word is addressed to the HI-6130/31 terminal but contains subaddress 0x0 or 0x1F, the command is not recognized; there is no RT command response, and no status updating for the benefit of follow-

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ing “transmit status” or “transmit last command” mode commands.

When either RT-RT command word (with subaddress field not equal to 0x0 or 0x1F) is addressed to the HI-6130/21 terminal, but the other command word contains subaddress 0x0 or 0x1F, the RT-RT command is not recognized as valid. There is no RT command response, and no status updating for the benefit of following “transmit status” or “transmit last command” mode commands.

An RT-RT command pair where Command Word 1 is addressed to the HI-6130/21 terminal and Command Word 2 is addressed to a different terminal is considered an “RT-RT receive” command. When the message is transacted, the device sets the RTRT bit in the Receive Subaddress Message Information Word in the subaddress data buffer.

An RT-RT command pair where Command Word 2 is solely addressed to the HI-6130/21 terminal (not RT31) is considered an “RT-RT transmit” command. The Message Information Word does not distinguish the RT to RT transmit message from an ordinary RT to BC transmit command.

19.2. Command Illegalization Table

The following pages describe various structures residing in the RAM shared between the host and HI-6130 or HI-6131 command processing logic. The host initializes these structures to control the terminal’s response to received commands. The first structure described is the command Illegalization Table used for “illegal command detection”.

Illegal command detection is an optional process. When illegal command detection is not used, the terminal “responds in form” to all valid commands: it sends Clear Status and transacts the number of data words defined in the received command. When illegal command detection is not used, the bus controller cannot tell whether the command is legal or illegal, from the terminal’s transmitted response.

If illegal command detection is used, the terminal responds differently when an illegal command is detected. The terminal responds to illegal commands with “message error” status, transmitting only status word. Data word transmission is suppressed if the command type inherently includes transmitted data words. The terminal responds to each legal command with clear status and transacts the number of data words defined in the type of command received.

For consistency, apply illegal command detection to all illegal and unimplemented commands, and to all reserved or undefined mode code commands, or “respond in form” to all of these commands (illegal command detection disabled) by leaving the Illegalization Table in the all-cleared default state after $\overline{MR}$ master reset

The device uses a 256-word “Illegalization Table” in shared RAM to distinguish between legal and illegal commands. After the ($\overline{MR}$) master reset input is negated, HI-6130/21 performs internal self test including a shared RAM test which leaves all memory locations fully reset. Once self test is complete, the HI-6130/21 READY output goes high to indicate HI-6130/21 readiness for host initialization. At this point, all entries in the Illegalization Table read logic 0, so by default, illegal command detection is not applied.

To apply illegal command detection, the host (or auto-initialization) writes the Illegalization Table to set bits for all illegal command combinations. This typically includes any unimplemented subaddresses and/or word counts, undefined mode commands, reserved mode commands and any mode commands not implemented in the terminal design. Host initialization of the table can be replaced by auto-initialization.

Once STEX is set in Configuration Register 1, terminal execution begins. Each time a valid command is received, a 1-bit entry (indexed using command word data bits) is fetched from the Illegalization Table:

If fetched Illegalization Table bit equals logic 0, the command is “legal”; the terminal responds “in form”, transmitting clear status and transacting the number of data words defined for the message type. Terminal status is updated.

If fetched Illegalization Table bit equals logic 1, the command is “illegal”; the terminal responds with status word only, with Message Error bit set. No data words are transmitted. Terminal status is updated.

When illegal command detection is not applied, all table entries should read logic 0; the terminal responds “in form” to all valid commands.

The illegalization scheme allows any subset of command T/$\overline{R}$ bit, broadcast vs. non-broadcast status, subaddress and word count (or mode code number), for a total of 4,096 legal/illegal command combinations. Commands may be illegalized down to the word count level. For example, 10-word receive commands to a given subaddress may be legal, while 9-word receive commands to the same subaddress are illegal.

Broadcast receive commands are illegalized separately

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from non-broadcast receive commands. Transmit and receive commands for the same subaddress are illegalized separately. For mode commands, any combination of mode code number, T/$\overline{R}$ bit and broadcast/non-broadcast status can be legal or illegal.

The Illegalization Table is located in shared RAM within the fixed address range of 0x0100 to 0x01FF. See Figure 12. The table is comprised of 256 16-bit words. To cover the full range of 1 to 32 data words, each subaddress uses a pair of illegalization registers. The lower register (even memory address) covers word counts 0 to 15, using one bit per word count. As in command encoding, “0” denotes 32 data words. Bit 0 corresponds to 32 data words, bit 1 corresponds to 1 data word and bit 15 corresponds to 15 data words. The upper register (odd memory address) similarly covers word counts 16 to 31, using one bit per word count. Bit 0 corresponds to 16 data words, while bit 15 corresponds to 31 data words.

When a command’s subaddress field equals 0 or 31 (0x1F), the command is a mode command. Table entries for mode commands use bits to represent mode code numbers, not word counts. The lower register (even memory address) covers mode codes 0 to 15, using one bit per mode code. Bit 0 corresponds to mode code 0, bit 15 corresponds to mode code 15. The upper register (odd memory address) similarly covers mode codes 16 to 31, using one bit per mode code. Bit 0 corresponds to mode code 16, bit 15 corresponds to mode code 31. There is no functional difference between SA0 mode commands and SA31 mode commands. Since either subaddress indicates a mode command, the subaddress 0 table words should match the subaddress 31 table words in each quadrant.

Table entries from 0x0142 to 0x017D do not have to be programmed. These correspond to broadcast transmit subaddress commands (undefined by MIL-STD-1553B) and are always invalid. There is no terminal response.

Addressing for the Illegalization Table is derived from the command word T/$\overline{R}$ bit, subaddress field, MSB of the Word Count (Mode Code) field and the command’s broadcast vs. non-broadcast status as shown below in Figure 12.

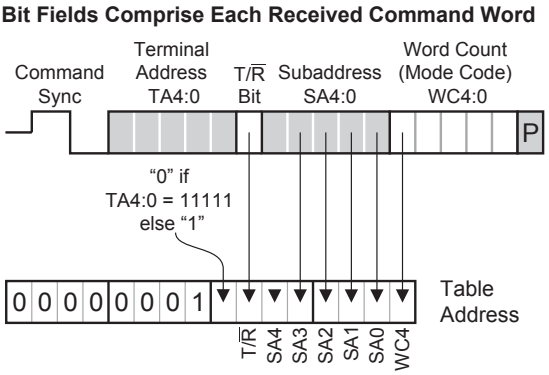

Figure 12. Deriving the Illegalization Table Address From the Received Command Word

Figure 14 on page 164 shows individual bit locations in the Illegalization Table for broadcast and non-broadcast variants of all mode commands defined by MIL-STD-1553B. Locations are also identified for reserved mode codes and undefined mode code commands.

The following examples illustrate how the Illegalization Table is initialized to distinguish between legal and illegal commands when “illegal command detection” is being used. Remember: If the terminal does not use illegal command detection, the table is left in its post-$\overline{MR}$ reset state, with all table locations reset to 0x0000. In this case, all command responses are “in form”.

For “subaddress commands” (ordinary receive commands or transmit commands) individual table bits correspond to word counts specified in the received command word. If a bit is 0, the corresponding word count is legal. If a bit is 1, the corresponding word count is illegal.

For example, transmit commands to subaddress 1 are controlled by the words at 0x01C2 and 0x01C3. In Figure 13 on page 163, these words are located in the “RT Address Transmit” block. The word stored at 0x01C3 controls subaddress 1 transmit commands having word counts 16 to 31. The word stored at 0x01C2 controls subaddress 1 transmit commands having word counts 1 to 15 or 32. (Reminder: In MIL-STD-1553B, zero corresponds to 32 words.)

```
Word at 0x01C3 (Tx Subaddr 1) 31 to 16 words
Bit      15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
Words    31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

Word at 0x01C2 (Tx Subaddr 1) 15 to 1 & 32 words
Bit      15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
Words    15 14 13 12 11 10  9  8  7  6  5  4  3  2  1 32
```

If the word stored at 0x01C3 = 0xFFFF and the word stored at 0x01C2 = 0xFF0F, then commands with 4, 5, 6, or 7 data words are the only legal transmit commands

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for subaddress 1 and all other word counts are illegal. Receive commands and broadcast receive commands for Subaddresses1 through 30 are encoded similarly.

For "mode code commands" (characterized by command word subaddress field equal to 00000 or 11111 binary) individual table bits correspond to individual mode code values. Here "transmit" and "receive" simply indicate the state of the command word T/$\overline{R}$ bit. (For mode codes 0-15, the T/$\overline{R}$ bit does not indicate data direction since data is not transacted when fulfilling these commands).

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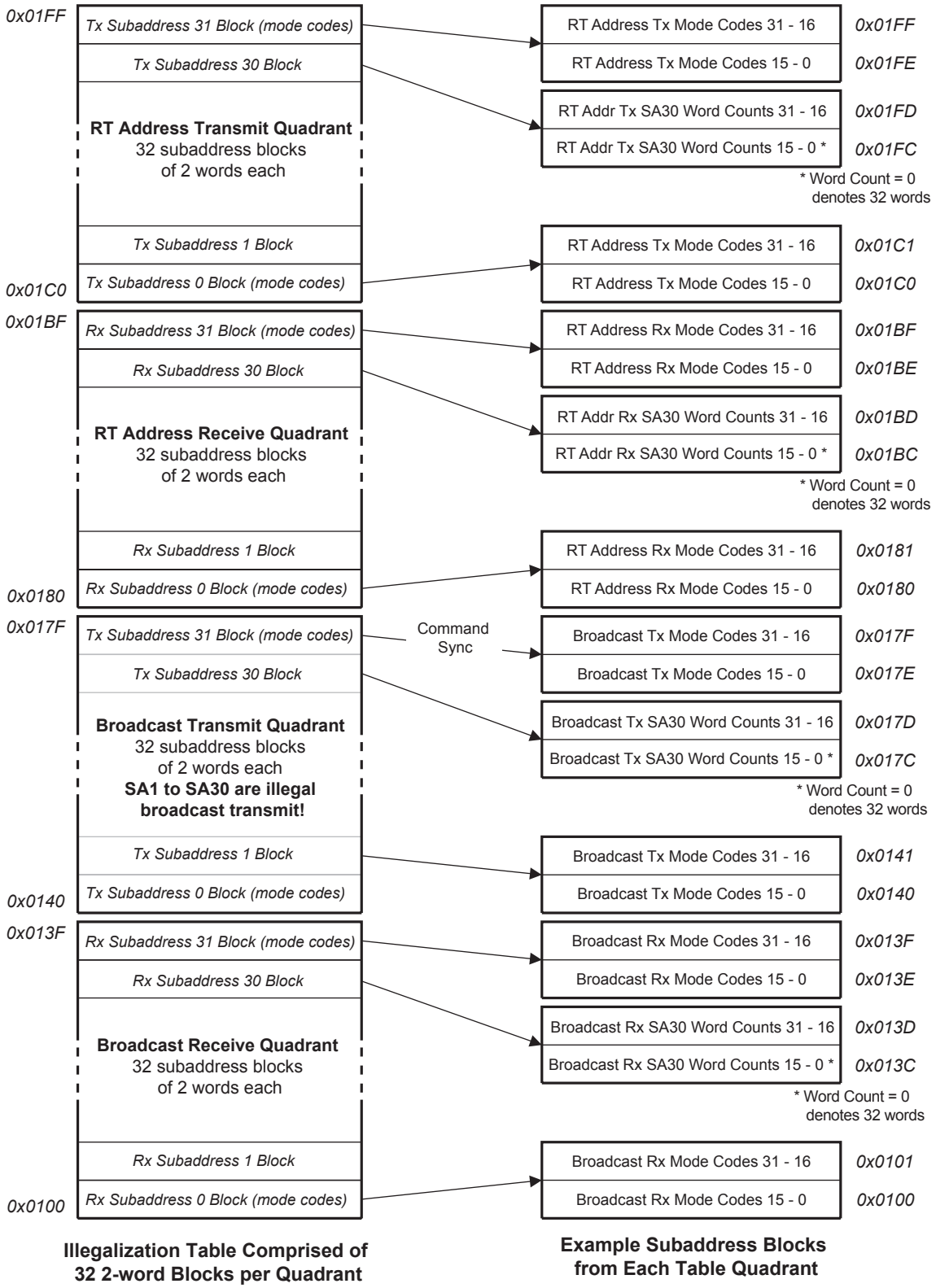

Figure 13. Fixed Address Mapping for Illegalization Table

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Figure 14 summarizes the 16 Illegalization Table locations for mode commands. These locations are scattered throughout the overall Illegalization Table shown in Figure 13. Remember: the host must initialize all table locations corresponding to both subaddress 0 and subaddress 31 (11111 binary).

Consider an example in which all reserved and all undefined mode commands are illegal. If all defined transmit mode commands are legal except MC0 (”dynamic bus control”) the eight table entries for transmit mode commands would be:

0x01FF and 0x01C1 = 1111 1111 1111 0010 = 0xFFF2
0x01FE and 0x01C0 = 1111 1110 0000 0001 = 0xFE01
0x017F and 0x0141 = 1111 1111 1111 1111 = 0xFFFF
0x017E and 0x0140 = 1111 1110 0000 0101 = 0xFE05

The receive mode command words are encoded similarly. Continuing the same example where all reserved and all undefined mode commands are illegal: If all defined receive mode commands are legal, the eight table entries for receive mode commands would be:

0x01BF and 0x0181 = 1111 1111 1100 1101 = 0xFFCD
0x01BE and 0x0180 = 1111 1111 1111 1111 = 0xFFFF
0x013F and 0x0101 = 1111 1111 1100 1101 = 0xFFCD
0x013E and 0x0100 = 1111 1111 1111 1111 = 0xFFFF

RAM Address			Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x01FF and 0x01C1	Tx MC31 - MC16	Transmit Mode Commands With Data	**MC #**	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			Status	R	R	R	R	R	R	R	R	R	R	U	U	D	D	U	D
0x01FE and 0x01C0	Tx MC15 - MC0	Transmit Mode Commands Without Data	**MC #**	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			Status	R	R	R	R	R	R	R	D	D	D	D	D	D	D	D	D
0x01BF and 0x0181	Rx MC31 - MC16	Receive Mode Commands With Data	**MC #**	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			Status	R	R	R	R	R	R	R	R	R	R	D	D	U	U	D	U
0x01BE and 0x0180	Rx MC15 - MC0	Receive Mode Commands Without Data	**MC #**	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			Status	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
0x017F and 0x0141	Br.Tx MC31 - MC16	Broadcast Transmit Mode Commands With Data	**MC #**	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			Status	R	R	R	R	R	R	R	R	R	R	U	U	NB	NB	U	NB
0x017E and 0x0140	Br.Tx MC15 - MC0	Broadcast Transmit Mode Commands Without Data	**MC #**	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			Status	R	R	R	R	R	R	R	D	D	D	D	D	D	NB	D	NB
0x013F and 0x0101	Br.Rx MC31 - MC16	Broadcast Receive Mode Commands With Data	**MC #**	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			Status	R	R	R	R	R	R	R	R	R	R	D	D	U	U	D	U
0x013E and 0x0100	Br.Rx MC15 - MC0	Broadcast Receive Mode Commands Without Data	**MC #**	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			Status	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

LEGEND

D = Defined Mode Command
U = Undefined Mode Command
R = Reserved Mode Code
NB = Defined Code, But Broadcast Not Allowed

Figure 14. Summary of Illegalization Table Addresses for Mode Code Commands

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19.3. Temporary Receive Data Buffer

The 32-word temporary receive data buffer resides in shared RAM in address space 0x0020 to 0x003F. The device optionally uses this buffer for temporary storage of receive data words until successful message completion. To enable the buffer, the host asserts the TRXDC bit in Configuration Register 2.

When enabled, the terminal stores received data words in the 32-word buffer during message processing. Upon error-free message completion, all buffered words are written in a burst to the data buffer memory assigned to the specific subaddress in the Descriptor Table.

When the TRXDB bit in Configuration Register 2 is negated, the temporary receive data buffer is disabled. At 20us intervals, the terminal writes received data words to assigned subaddress data buffer memory as each word is received. If message error occurs during data reception, data integrity is lost; valid data from the prior receive message may be partially overwritten by data from a message ending in error. MIL-STD-1553 states that all received data from messages ending in error **should be disregarded.**

In a typical application, the temporary buffer is not directly accessed by the host, although there is no restriction preventing host data access. The host should never write data into the temporary buffer space.

19.4. Interrupt Log Buffer

Two interrupt output pins notify the host upon occurrence of pre-determined interrupt-causing events. The interrupt types are listed below. Each interrupt type only occurs when the corresponding interrupt type bit is asserted in the Interrupt Enable Register. To manage host interrupts, the device architecture uses an Interrupt Log buffer, three control registers, two interrupt output pins and two interrupt acknowledge input pins. The data sheet section entitled “Interrupt Management” provides additional details.

Shown in Figure 15, the Interrupt Log Buffer is a 32-word ring buffer located in shared RAM, at address range 0x0040 to 0x005F. To help the host process interrupts, the device interrupt manager maintains information from the 16 most recent interrupts in this buffer. The buffer contains two information words for each occurring interrupt: the Interrupt Identification Word and Interrupt Address Word.

The Interrupt Identification Word (IIW) identifies the occurring interrupt type using a word format identical to the Pending Interrupt Register. Upon update, all bits except the occurring interrupt type bit(s) are reset.

Table 14. Interrupt Information Word Bits Summary

IIW - Interrupt Information Word			**IAW - Interrupt Address Word**
Bit	*Interrupt*	*Origin*	
15	IXEQZ	Message	IAW contains the Command Word Descriptor Table Address
14	IWA	Message	
13	IBR	Message	
12		-----	
11		-----	
10	MERR	Message	
9		-----	
8	ILCMD	Message	
7	SPIFAIL	Hardware	IAW contains 0x0000
6	LBFA	Hardware	
5	LBFB	Hardware	
4	TTINT1	Hardware	
3	TTINT0	Hardware	
2	RTAPF	Hardware	
1	EECKF	Hardware	
0	RAMIF	Hardware	

More than one bit may be asserted in an Interrupt Identification Word. For example, IBR (interrupt broadcast received) and MERR (interrupt message error) can occur for the same message. One assertion of the $\overline{\text{INTMES}}$ output pin alerts the host when concurrent message interrupts occur.

The Interrupt Address Word (IAW) identifies the originating command for message-based interrupts. When interrupts originate from message processing, the Interrupt Address Word (IAW) identifies the interrupt source using the 16-bit address of the command’s Control Word in the Descriptor Table. Hardware interrupts are not linked with command processing. These interrupts write an Interrupt Address Word value of 0x0000.

After $\overline{\text{MR}}$ reset or SRST software reset, the device automatically initializes bits 7:0 in the Interrupt Log Address

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register to the buffer's base address, 0x0040. The bit 7:0 value read will always be even, ranging from 0x0040 to 0x005E. Once terminal operation begins, the current value of the Interrupt Log Address indicates where the Interrupt Information Word (IIW) for the next occurring interrupt will be stored.

On the first interrupt occurring after reset, the device writes the IIW and IAW to offset locations 00000 and 00001 respectively. The device increments the ring buffer pointer after each word is stored, storing interrupt information sequentially in the ring buffer. Information words for the sixteenth interrupt are stored in offset locations 0x1E and 0x1F (buffer addresses 0x005E and 0x005F) and the Interrupt Log Address "rolls over" to again point to offset location 0 (buffer address 0x0040) where the Interrupt Information Word for the seventeenth interrupt will be stored.

Bits 15:8 in the Interrupt Log Address register maintain a count of interrupt events since the register was last read. The interrupt count stops at 255 decimal. Counts greater than 16 indicate buffer overrun, but the extended count capacity is provided as a diagnostic aid.

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0x005F	INTERRUPT 16	Interrupt Address Word
0x005E	INTERRUPT 16	Interrupt Information Word
0x005D	INTERRUPT 15	Interrupt Address Word
0x005C	INTERRUPT 15	Interrupt Information Word
0x005B	INTERRUPT 14	Interrupt Address Word
0x005A	INTERRUPT 14	Interrupt Information Word
0x0059	INTERRUPT 13	Interrupt Address Word
0x0058	INTERRUPT 13	Interrupt Information Word
0x0057	INTERRUPT 12	Interrupt Address Word
0x0056	INTERRUPT 12	Interrupt Information Word
0x0055	INTERRUPT 11	Interrupt Address Word
0x0054	INTERRUPT 11	Interrupt Information Word
0x0053	INTERRUPT 10	Interrupt Address Word
0x0052	INTERRUPT 10	Interrupt Information Word
0x0051	INTERRUPT 9	Interrupt Address Word
0x0050	INTERRUPT 9	Interrupt Information Word
0x004F	INTERRUPT 8	Interrupt Address Word
0x004E	INTERRUPT 8	Interrupt Information Word
0x004D	INTERRUPT 7	Interrupt Address Word
0x004C	INTERRUPT 7	Interrupt Information Word
0x004B	INTERRUPT 6	Interrupt Address Word
0x004A	INTERRUPT 6	Interrupt Information Word
0x0049	INTERRUPT 5	Interrupt Address Word
0x0048	INTERRUPT 5	Interrupt Information Word
0x0047	INTERRUPT 4	Interrupt Address Word
0x0046	INTERRUPT 4	Interrupt Information Word
0x0045	INTERRUPT 3	Interrupt Address Word
0x0044	INTERRUPT 3	Interrupt Information Word
0x0043	INTERRUPT 2	Interrupt Address Word
0x0042	INTERRUPT 2	Interrupt Information Word
0x0041	INTERRUPT 1	Interrupt Address Word
0x0040	INTERRUPT 1	Interrupt Information Word

The Interrupt Log Address Register points to this address after Interrupt 15 event occurs. Upon Interrupt 16 completion, device logic reinitializes the log address pointer to 0x0040 before Interrupt 17 is processed.

EXAMPLE: 2-WORD LOG BUFFER ENTRIES FOR VARIOUS INTERRUPT TYPES...

Example 1: MERR bit is set in Interrupt Enable Register. An error occurs while transacting a receive command for subaddress 30:

Address Word = 0x0278 Descriptor Address for Rx Subaddress 30.*
Information Word = 0x0400 MERR (interrupt message error) bit = 1.

Example 2: IWA bit is set in Interrupt Enable Register. The IWA bit is set in Transmit Subaddress 30 Control Word to generate an interrupt upon each message occurrence. A transmit command is received for subaddress 30:

Address Word = 0x02F8 Descriptor Address for Tx Subaddress 30.*
Information Word = 0x4000 IWA (interrupt when accessed) bit = 1.

Example 3: ILCMD bit is set in Interrupt Enable Register. "Illegal Command Detection" is being applied and all Illegalization Table bits for undefined mode codes are set. An undefined Mode Code 0 with T/$\overline{R}$ bit = 0 is received:

Address Word = 0x0300 Descriptor Address for Rx Mode Code 0.*
Information Word = 0x0100 ILCMD (interrupt illegal command) bit = 1.

Example 4: TTINT0 bit is set in Interrupt Enable Register. The Time-Tag counter rolls over from full count 0xFFFF to 0x0000:

Address Word = 0x0000 (all hardware interrupts reset the IAW)
Information Word = 0x0010 TTINT0 (Time-Tag interrupt 0) bit = 1

* Figure 8 shows where these addresses occur in the Descriptor Table.

Interrupt Log Address Register is initialized by device logic to point to this address after hardware reset ($\overline{MR}$) or software reset

Figure 15. Fixed Address Mapping for Interrupt Log Buffer

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19.5. Descriptor Table

The Descriptor Table, resides in shared RAM, in address range 0x0200 to 0x03FF. This table is initialized by the host (or auto-initialization) to define how the terminal processes valid commands. Descriptor Table settings for each command specify where message data is stored, how data is stored, whether host interrupts are generated, and other aspects essential to command processing. Shown in Figure 16, the table consists of 128 consecutive “descriptor blocks”, each comprised of four 16-bit words. The table is organized into four quadrants.

The Receive Subaddress and Transmit Subaddress quadrants define response for commands having a subaddress field ranging from 1 to 30 (0x1E). These are simple N-data word receive or transmit commands, where N can range from 1 to 32 words. When the command T/$\overline{R}$ bit equals 0, the receive command quadrant applies. When the T/$\overline{R}$ bit equals 1, the transmit command quadrant applies.

Both subaddress quadrants are padded at top and bottom with unused Descriptor Blocks for subaddresses 0 and 31 (0x1F). The word space reserved for SA0 and SA31 aligns the table addressing, but values stored in these eight locations is not used. Command subaddresses 0 and 31 indicate mode commands. The response for commands containing either SA value is defined in the two mode command table quadrants. The Receive Mode Command quadrant applies when the command word T/$\overline{R}$ bit equals 0, while the Transmit Mode Command quadrants applies when T/$\overline{R}$ equals 1.

The term “Transmit Mode Command” is a misnomer. All defined mode commands with mode code less than 0x0F haveT/$\overline{R}$ bit equal to 1, yet none of these mode commands transmits a data word. They transmit only the terminal status word, just like receive commands.

Within the Receive and Transmit Mode Command quadrants, block addressing is based on the low order 5 bits in the command word, containing the mode code value. This is fundamentally different from the Subaddress quadrants in which block addressing is based on the 5-bit subaddress field. Figure 17 shows how to derive Control Word address from the received Command Word. The Control Word address for the last valid command can also be found in the Current Control Word Address register.

All 128 4-word Descriptor Blocks start with a Control Word. There are four Control Word variants (described later), based on command type: receive vs. transmit and mode vs. non-mode commands. All descriptor Control Words are initialized by the host (or auto-initialization) to define basic command response. Each Control Word specifies the data buffer method and host interrupt for a specific subaddress or mode command.

Each subaddress has both a Receive Subaddress block and a Transmit Subaddress block. Receive and transmit commands to the same subaddress can be programmed to respond differently.

The function of the three remaining descriptor words (in each 4-word block) depends on the data buffer method specified in the Control Word. There are 4 data buffer options available:

Indexed (or Single Buffer) Method where a predetermined number of messages is transacted using a single data buffer in shared RAM. Several host interrupt options are offered, including an interrupt generated when all N messages are successfully completed.

Double (or Ping-Pong) Buffer Method where successive messages alternate between two data buffers in shared RAM. Several host interrupt options are offered.

Circular Buffer Mode 1 where buffer boundaries determine when the bulk transfer is complete and message information and time-tag words are stored with message data in a common buffer. Several host interrupt options are offered, including an interrupt generated when the allocated data buffer is full.

Circular Buffer Mode 2 where the number of messages transacted defines bulk transfer progress, and message data words are stored contiguously in one buffer while message information and time-tag words are stored in a separate buffer. Several host interrupt options are offered, including an interrupt generated when all N messages are successfully completed.

The 4-word Descriptor Table entry for each command (its descriptor block) begins with a Control Word. There are four types of descriptor Control Word:

- Receive Subaddress Control Word
- Transmit Subaddress Control Word
- Receive Mode Command Control Word
- Transmit Mode Command Control Word

The descriptor Control Word is initialized by the host to select data buffer method and interrupt options. After a command is processed by the HI-6130/21 terminal, the device updates the command’s descriptor Control Word. Update will differ based on the chosen data buffer method. Reading the descriptor table can differ from other RAM accesses. For HI-6130, see **Section XX**. For HI-6131, see **Sections XX** and **XX**.

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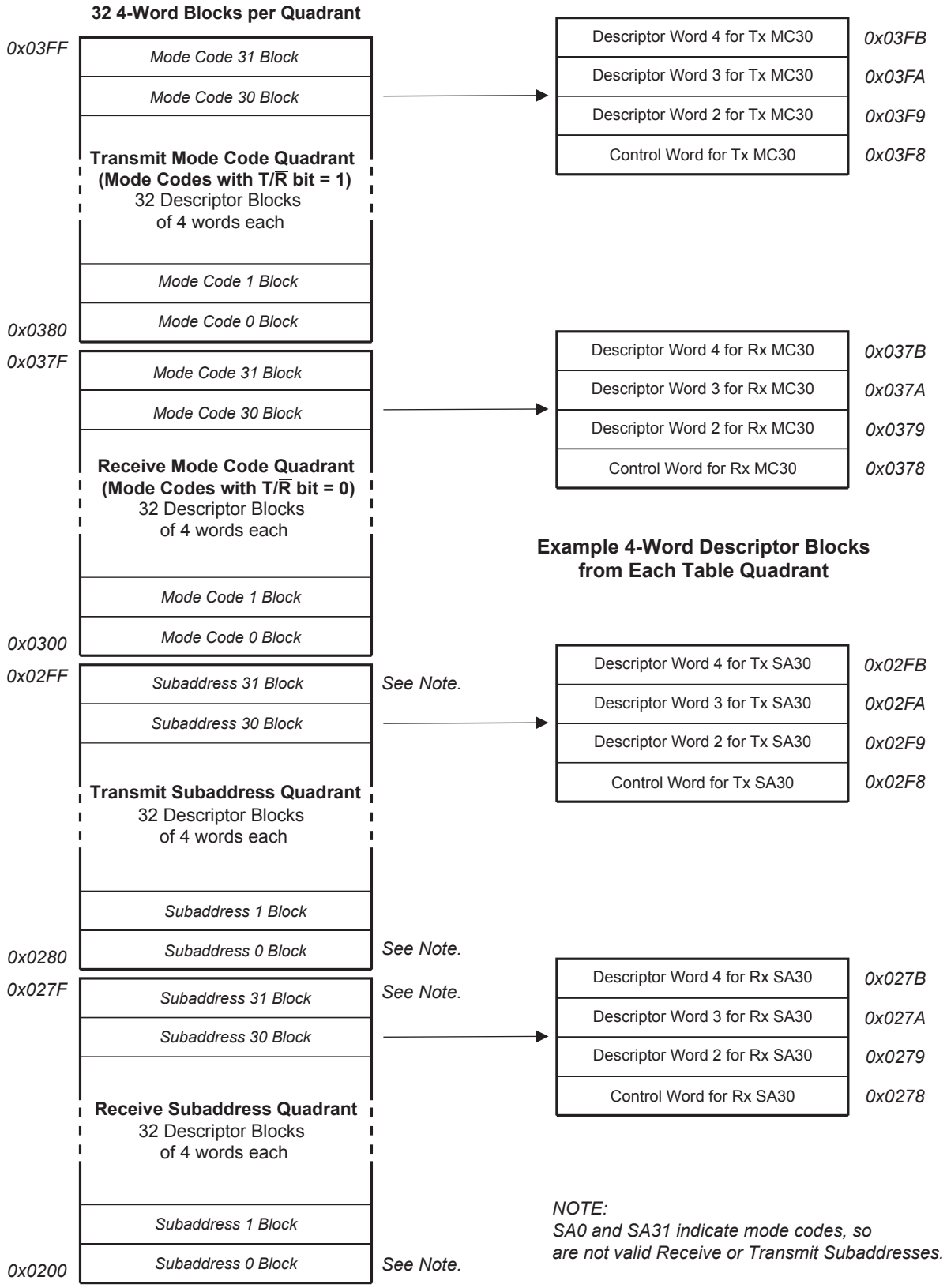

Figure 16. Address Mapping for Descriptor Table
(assumes table base address = 0x0200)

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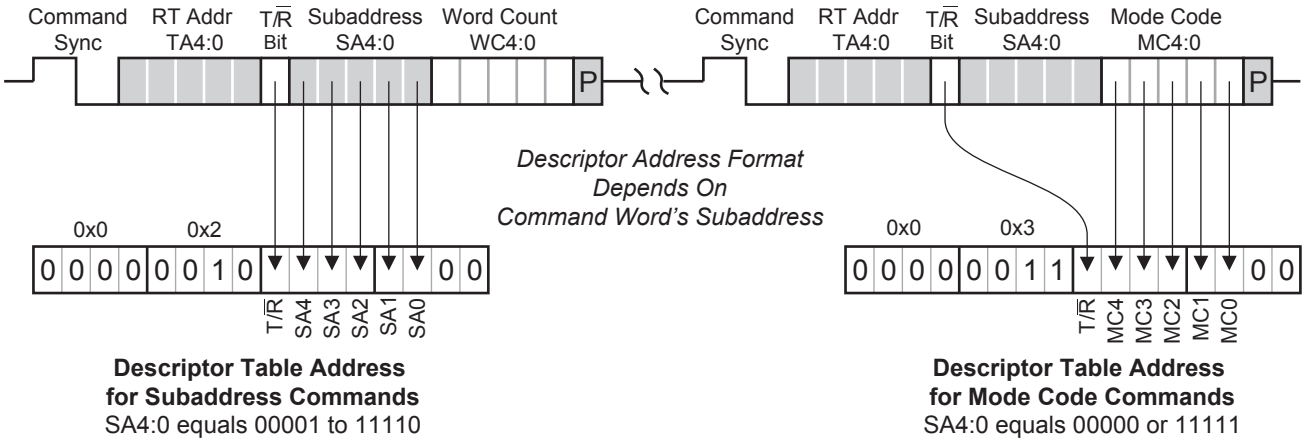

Figure 17. Deriving a Descriptor Table Control Word Address From Command Word
(assumes table base address = 0x0200)

19.5.1. Receive Subaddress Control Word

Receive Subaddress Control Words apply when a valid command word T/$\overline{R}$ bit equals zero (receive) and the subaddress field has a value in the range of 1 to 30 (0x1E). The descriptor Control Word defines terminal command response and interrupt behavior, and conveys activity status to the host. It is initialized by the host before terminal execution begins. Bits 8-11 cannot be written by the host; these bits are updated by the device during terminal execution, that is, when Configuration Register 1 STEX bit equals 1. The host can write bits 0-2 and 4-7 only when STEX equals zero; bits 3 and 12-15 can be written anytime. This register is cleared to 0x0000 by $\overline{MR}$ master reset. Software reset (SRST) clears just the DBAC, DPB and BCAST bits. **Following any read cycle to the Control Word address, the DBAC bit is reset.**

NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). The bit value following software reset is unchanged unless specifically indicated by an "SR" value.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	IXEQZ		0	Interrupt When Index Equals Zero. If the Interrupt Enable Register IXEQZ bit is high, assertion of this bit enables generation of an interrupt for (a) subaddresses using indexed buffer mode when the INDX value decrements from 1 to 0, or (b) subaddresses using a circular buffer mode when the pre-determined number of messages has been transacted. If enabled, upon completion of command processing that results in index = 0, an IXEQZ interrupt is entered in the Pending Interrupt Register, output pin $\overline{INTMES}$ is asserted, and the interrupt is registered in the Interrupt Log.

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Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
14	IWA		0	Interrupt When Accessed. If the Interrupt Enable Register IWA bit is high, assertion of this bit enables interrupt generation when the subaddress receives any valid receive command. If enabled, upon completion of command processing, an IWA interrupt is entered in the Pending Interrupt Register, output pin $\overline{\text{INTMES}}$ is asserted, and the interrupt is registered in the Interrupt Log.
13	IBR		0	Interrupt Broadcast Received. If the Interrupt Enable Register IBR bit is high, assertion of this bit enables interrupt generation when the subaddress receives a valid broadcast command. If enabled, upon completion of message processing an IBR interrupt is entered in the Pending Interrupt Register, output pin $\overline{\text{INTMES}}$ is asserted, and the interrupt is registered in the Interrupt Log. This bit has no function if the BCSTINV bit is high in Configuration Register 1. In this case, commands to RT address 31 are not recognized as valid by the device.
12	MKBUSY		0	Make Busy. The host asserts the MKBUSY bit to respond with Busy status for commands to this receive subaddress. This bit is an alternative to globally applying Busy status for all valid commands, enabled from the 1553 Status Bits Register. See that register description for additional information. When Busy is asserted, received data words are not stored and the DPB bit does not toggle after message completion.
11	DBAC		0 SR = 0	Descriptor Block Accessed. Internal device logic asserts the DBAC bit upon completion of message processing. The host may poll this bit to detect subaddress activity, instead of using host interrupts. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset, SRST software reset or a read cycle to this memory address.
10	DPB		0 SR = 0	Data Pointer B. This status bit is maintained by the device and only applies in ping-pong buffer mode. This bit indicates the buffer to be used for the next occurring receive command to this subaddress. When the DPB bit is logic 0, the next message will use Data Pointer A; when DPB is logic 1, the next message uses Data Pointer B. In ping-pong buffer mode, the bit is inverted after each **error-free** message completion. The DPB bit is not altered after messages ending in error, after illegal commands or after messages when the terminal responds with Busy status. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset or SRST software reset; therefore the first message received after either reset will use Buffer A. This bit is “don’t care” for indexed single-buffer mode or either circular buffer mode.
9	BCAST		0 SR = 0	Broadcast Command. Device logic sets this bit when a valid broadcast receive command is received at this subaddress. If IBR bit 13 and Interrupt Enable Register IBR bit are both set, the output pin $\overline{\text{INTMES}}$ is asserted. This bit has no function if the BCSTINV bit is asserted in the Configuration Register 1; in this case commands to RT address 31 are not recognized as valid by the device. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset or SRST software reset.

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>8</td><td>PPON</td><td></td><td>0</td><td>Ping-Pong Enable Acknowledge.

This bit is controlled by the device and cannot be written by the host. It only applies if PPEN bit 2 was initialized to logic one by the host after reset, enabling ping-pong buffer mode for this subaddress. Device logic asserts this bit when it recognizes ping-pong is active for this subaddress. Before off-loading the receive data buffer for this subaddress, the host can ask the device to temporarily disable ping-pong by asserting STOPP bit 3. The device acknowledges ping-pong is disabled by negating PPON. The host can safely off-load the buffer without data collision while PPON is negated. After buffer servicing, the host asks the device to re-enable ping-pong by negating STOPP bit 3. The device acknowledges ping-pong is re-enabled by asserting PPON.

If PPEN bit 2 is high and PPON bit 8 is low when new commands arrive for this subaddress, ping-pong is disabled. Each new message overwrites existing data in the buffer specified by DPB bit 10, and the DPB bit does not toggle after command completion.</td></tr>
<tr><td>7-4</td><td>CIR2ZN</td><td></td><td>0</td><td>Circular Mode 2 Zero Number.

Used only in circular buffer mode 2, this 4-bit field is initialized with the number of trailing zeros in the initialized MIBA address. This is explained in Section XX, which fully describes circular buffer mode 2.</td></tr>
<tr><td>3</td><td>STOPP</td><td></td><td>0</td><td>Stop Ping-Pong Request.

The host asserts this bit to suspend ping-pong buffering for this subaddress. The host resets this bit to ask the device to re-enable ping-pong. The device confirms recognition of ping-pong enable or disable status by writing PPON bit 8. Refer to Section XX, which fully describes ping-pong mode.</td></tr>
<tr><td>2
1
0</td><td>PPEN
CIR2EN
CIR1EN</td><td></td><td>0
0
0</td><td>Ping-Pong, Circular Buffer Mode 2 or Circular Buffer Mode 1 Enable.

The PPEN, CIR2EN and CIR1EN bits are initialized by the host to select buffer mode. The table below summarizes how buffer mode selection is encoded.

In the case of ping-pong, the host initializes the PPEN bit to logic one after reset to enable ping-pong buffering for this subaddress. The host asserts STOPP bit 3 to ask the device to temporarily disable ping-pong. Negating the STOPP bit asks the device to re-enable ping-pong. The device confirms ping-pong enable or disable state changes by writing the PPON bit.
<table>
<tr><th>PPEN</th><th>CIR2EN</th><th>CIR1EN</th><th>Buffer Mode</th></tr>
<tr><td>1</td><td>Don’t Care</td><td>Don’t Care</td><td>Ping-Pong</td></tr>
<tr><td>0</td><td>1</td><td>Don’t Care</td><td>Circular Mode 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Circular Mode 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Indexed Single Buffer</td></tr>
</table>
</td></tr>
</table>

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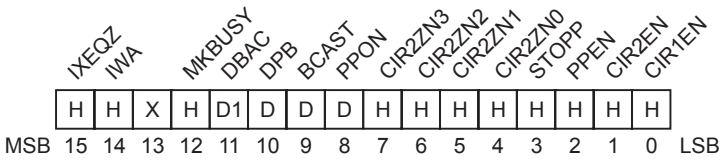
19.5.2. Transmit Subaddress Control Word

Transmit Subaddress Control Words apply when a valid command word T/$\overline{R}$ bit equals one (transmit) and the subaddress field has a value in the range of 1 to 30 (0x1E). The descriptor Control Word defines terminal command response and interrupt behavior, and conveys activity status to the host. It is initialized by the host before terminal execution begins. Bits 8-11 cannot be written by the host; these bits are updated by the device during terminal execution, that is, when Configuration Register 1 STEX bit equals 1. The host can write bits 0-2 and 4-7 only when STEX equals zero; bits 3,12 and 14-15 can be written anytime. This register is cleared to 0x0000 by $\overline{MR}$ master reset. Software reset (SRST) clears just the DBAC, DPB and BCAST bits. **Following any host read cycle to the Control Word address, the DBAC bit is reset.**



H Bit maintained by host

D Bit maintained by device

D1 Bit set by device, reset by host read cycle

X Bit is not used, may be logic 0 or 1

NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). The bit value following software reset is unchanged unless specifically indicated by an "SR" value.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	IXEQZ		0	Interrupt When Index Equals Zero. If the Interrupt Enable Register IXEQZ bit is high, assertion of this bit enables generation of an interrupt for (a) subaddresses using indexed buffer mode when the INDX value decrements from 1 to 0, or (b) subaddresses using a circular buffer mode when the pre-determined number of messages has been transacted. If enabled, upon completion of command processing that results in index = 0, an IXEQZ interrupt is entered in the Pending Interrupt Register, output pin $\overline{INTMES}$ is asserted, and the interrupt is registered in the Interrupt Log.
14	IWA		0	Interrupt When Accessed. If the Interrupt Enable Register IWA bit is high, assertion of this bit enables interrupt generation when the subaddress receives any valid transmit command. If enabled, upon completion of command processing, an IWA interrupt is entered in the Pending Interrupt Register, output pin $\overline{INTMES}$ is asserted, and the interrupt is registered in the Interrupt Log.
13	-----		0	Not Used
12	MKBUSY		0	Make Busy. The host asserts the MKBUSY bit to respond with Busy status for commands to this transmit subaddress. This bit is an alternative to globally applying Busy status for all valid commands, enabled from the 1553 Status Bits Register. See that register description for additional information. When Busy is asserted, data words are not transmitted and the DPB bit does not toggle after message completion.

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Bit No.	Mnemonic	R/W	Reset	Function
11	DBAC		0 SR = 0	Descriptor Block Accessed. Internal device logic asserts the DBAC bit upon completion of message processing. The host may poll this bit to detect subaddress activity, instead of using host interrupts. This bit is reset to logic zero by $\overline{MR}$ master reset, SRST software reset or a read cycle to this memory address.
10	DPB		0 SR = 0	Data Pointer B. This status bit is maintained by the device and only applies in ping-pong buffer mode. This bit indicates the buffer to be used for the next occurring transmit command to this subaddress. When the DPB bit is logic 0, the next message will use Data Pointer A; when DPB is logic 1, the next message uses Data Pointer B. In ping-pong buffer mode, the bit is inverted after each error-free message completion. The DPB bit is not altered after messages ending in error, after illegal commands or after messages when the terminal responds with Busy status. This bit is reset to logic 0 by $\overline{MR}$ master reset or SRST software reset; therefore the first message received after either reset will use Buffer A. This bit is “don’t care” for indexed single-buffer mode or either circular buffer mode.
9	BCAST		0 SR = 0	Broadcast Received. The device sets this bit when a broadcast-transmit command is received for this subaddress. Because non-mode broadcast-transmit commands are always illegal, the assertion of this bit in the Control Word by the device indicates an illegal command was received. Terminal response varies, depending on whether or not illegal command detection applies (any bits set in Illegalization Table). This bit has no function if the BCSTINV bit is asserted in Configuration Register 1; in this case commands to RT address 31 are not recognized as valid by the device. This bit is reset to logic 0 by $\overline{MR}$ master reset or SRST software reset.
8	PPON		0	Ping-Pong Enable Acknowledge. This bit is controlled by the device and should not be written by the host. It only applies if PPEN bit 2 was initialized to logic one by the host after reset, enabling ping-pong buffer mode for this subaddress. The RT asserts this bit when it recognizes ping-pong is active for this subaddress. Before loading the transmit data buffer for this subaddress, the host can ask the RT to temporarily disable ping-pong by asserting STOPP bit 3. The RT acknowledges ping-pong is disabled by negating PPON. The host can safely load the buffer without data collision while PPON is negated. After buffer servicing, the host asks the RT to re-enable ping-pong by negating STOPP bit 3. The RT acknowledges ping-pong is re-enabled by asserting PPON. If PPEN bit 2 is high and PPON bit 8 is low when new commands arrive for this subaddress, ping-pong is disabled. Each new message transmits data from the same buffer, specified by DPB bit 10, and the DPB bit does not toggle after command completion.
7-4	CIR2ZN		0	Circular Mode 2 Zero Number. Used only in circular buffer mode 2, this 4-bit field is initialized with the number of trailing zeros in the initialized MIBA address. This is explained in **Section XX**, which fully describes circular buffer mode 2.

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<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>3</td><td>STOPP</td><td></td><td>0</td><td>Stop Ping-Pong Request.
The host asserts this bit to suspend ping-pong buffering for this subaddress. The host resets this bit to ask the RT to re-enable ping-pong. The RT confirms recognition of ping-pong enable or disable status by writing PPON bit 8. Refer to Section XX, which describes ping-pong mode in detail.</td></tr>
<tr><td>2
1
0</td><td>PPEN
CIR2EN
CIR1EN</td><td></td><td>0
0
0</td><td>Ping-Pong, Circular Buffer Mode 2 or Circular Buffer Mode 1 Enable.
The PPEN, CIR2EN and CIR1EN bits are initialized by the host to select buffer mode. The table below summarizes how buffer mode selection is encoded.
In the case of ping-pong, the host initializes the PPEN bit to logic one after reset to enable ping-pong buffering for this subaddress. The host asserts STOPP bit 3 to ask the device to temporarily disable ping-pong. Negating the STOPP bit asks the device to re-enable ping-pong. The device confirms ping-pong enable or disable state changes by writing the PPON bit.
<table>
<tr><th>PPEN</th><th>CIR2EN</th><th>CIR1EN</th><th>Buffer Mode</th></tr>
<tr><td>1</td><td>Don’t Care</td><td>Don’t Care</td><td>Ping-Pong</td></tr>
<tr><td>0</td><td>1</td><td>Don’t Care</td><td>Circular Mode 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Circular Mode 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Indexed Single Buffer</td></tr>
</table>
</td></tr>
</table>

19.5.3. Data Buffer Options for Mode Code Commands

Data buffer options for mode code commands differ from options offered for subaddress commands. Mode commands cannot use either circular data buffer method, but may use double (ping-pong) buffering or single (indexed) buffering. Single message Index mode (INDX = 0) is suitable in many applications (see **Section XX**). An alternative called **Simplified Mode Command Processing** (SMCP) may be globally applied for all mode code commands (see **Section XX**).

To use single (indexed) buffer or double (ping-pong) buffer for mode commands, the SMCP bit in Configuration Register 1 is logic 0. The Control Word PPEN bit for each mode command determines whether ping-pong or indexed buffering is used.

To use Simplified Mode Command Processing, the SMCP bit in Configuration Register 1 is set to logic 1. The Control Word PPEN bit for mode commands is “don’t care” (no longer specifies index or ping-pong buffer mode) because Simplified Mode Command Processing stores mode command data and message information words directly within each mode command’s redefined Descriptor Table block. When SMCP is enabled, mode code command descriptor blocks (in the Descriptor Table) do not contain data pointers to reserved buffers elsewhere in the shared RAM. Instead, each 4-word descriptor block itself contains the message information word, the time-tag word and the data word transacted for each mode command (for mode codes 16-31 decimal).

When Simplified Mode Command Processing is used, the range of active bits is reduced in each receive or transmit mode command Control Word. Interrupt control and response is not affected by the SMCP option. Simplified Mode Command Processing is fully presented in the later data sheet section entitled “Mode Code Commands.”

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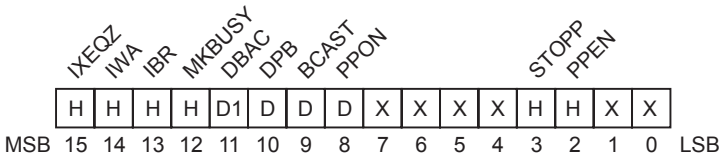
19.5.4. Receive Mode Control Word

Receive Mode Control Words apply when the command word T/$\overline{R}$ bit equals zero (receive) and the subaddress field has a value of 0 or 31 (0x1F). The descriptor Control Word defines terminal command response and interrupt behavior, and conveys activity status to the host. It is initialized by the host before terminal execution begins. Bits 8-11 cannot be written by the host; these bits are updated by the device during terminal execution, that is, when Configuration Register 1 STEX bit equals 1. The host can write bit 2 only when STEX equals zero; bits 3 and 12-15 can be written anytime. This register is cleared to 0x0000 by $\overline{MR}$ master reset. Software reset (SRST) clears just the DBAC, DPB and BCAST bits. **Following any read cycle to the Control Word address, the DBAC bit is reset.**

When single-message indexed buffering or ping-pong buffering is used instead of SMCP (Simplified Mode Code Processing), the receive mode Control Word looks like this:



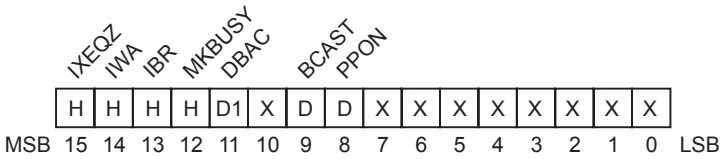
H Bit maintained by host

D Bit maintained by device

D1 Bit set by device, reset by host read cycle

X Bit is not used, may be logic 0 or 1

When SMCP applies, the number of active mode Control Word bits is reduced:



H Bit maintained by host

D Bit maintained by device

D1 Bit set by device, reset by host read cycle

X Bit is not used, may be logic 0 or 1

NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). The bit value following software reset is unchanged unless specifically indicated by an "SR" value.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	IXEQZ		0	Interrupt When Index Equals Zero. If the Interrupt Enable Register IXEQZ bit is high, assertion of this bit enables generation of an interrupt for mode code commands using indexed buffer mode when the INDX value decrements from 1 to 0. Upon completion of command processing that results in INDX = 0, when IXEQZ interrupts are enabled, an IXEQZ interrupt is entered in the Pending Interrupt Register, the $\overline{INTMES}$ output pin is asserted, and the interrupt is registered in the Interrupt Log.
14	IWA		0	Interrupt When Accessed. If the Interrupt Enable Register IWA bit is high, assertion of this bit enables interrupt generation at each instance of a valid mode code command. Upon completion of command processing, when IWA interrupts are enabled, an IWA interrupt is entered in the Pending Interrupt Register, the $\overline{INTMES}$ output pin is asserted, and the interrupt is registered in the Interrupt Log.

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Bit No.	Mnemonic	R/W	Reset	Function
13	IBR		0	Interrupt Broadcast Received. If the Interrupt Enable Register IBR bit is high, assertion of this bit enables interrupt generation at each instance of a valid broadcast receive mode code command. Upon completion of command processing, when IBR interrupts are enabled, an IBR interrupt is entered in the Pending Interrupt Register, the $\overline{\text{INTMES}}$ output pin is asserted, and the interrupt is registered in the Interrupt Log. This bit has no function if the BCSTINV bit is high in Configuration Register 1. In this case, commands to RT address 31 are not recognized as valid by the device.
12	MKBUSY		0	Make Busy. The host asserts the MKBUSY bit to respond with Busy status for commands to this mode code. This bit is an alternative to globally applying Busy status for all valid commands, enabled from the 1553 Status Bits Register. See that register description for additional information. When Busy is asserted, mode data words received with MC16-MC31 are not stored and the DPB bit does not toggle after message completion.
11	DBAC		0 SR = 0	Descriptor Block Accessed. Internal device logic asserts the DBAC bit upon completion of message processing. The host may poll this bit to detect mode command activity, instead of using host interrupts. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset, SRST software reset or a read cycle to this memory address.
10	DPB		0 SR = 0	Data Pointer B. This status bit is maintained by the device and only applies for mode commands using ping-pong buffer mode. This bit indicates the buffer to be used for the next occurring mode command. When the DPB bit is logic 0, the next message will use Data Pointer A; when DPB is logic 1, the next message uses Data Pointer B. In ping-pong buffer mode, the bit is inverted after each error-free message completion. The DPB bit is not altered after messages ending in error, after illegal commands, or after messages when the terminal responds with Busy status. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset or SRST software reset; therefore the first message received after either reset will use Buffer A. This bit is “don’t care” for indexed single-buffer mode.
9	BCAST		0 SR = 0	Broadcast Received. Device logic sets this bit when a valid broadcast mode command is received having T/$\overline{\text{R}}$ bit = 0. This bit has no function if the BCSTINV bit is asserted in Configuration Register 1. In this case, RT address 31 commands are not recognized as valid by the HI-6130/21. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset or SRST software reset.

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Bit No.	Mnemonic	R/W	Reset	Function
8	PPON		0	Ping-Pong Enable Acknowledge. This bit is read only and only applies for mode commands using ping-pong mode (PPEN bit 2 was initialized to logic 1 by the host after reset). The device asserts this bit when it recognizes ping-pong is active for this mode code. Before off-loading the receive data buffer for this mode code, the host can ask the device to temporarily disable ping-pong by asserting STOPP bit 3. The device acknowledges ping-pong is disabled by negating PPON. The host can safely load or off-load the buffer without data collision while PPON is negated. After buffer servicing, the host asks the device to re-enable ping-pong by negating STOPP bit 3. The device acknowledges ping-pong is re-enabled by asserting PPON. If PPEN bit 2 is high and PPON bit 8 is low when new commands arrive for this subaddress, ping-pong is disabled. Each new message overwrites existing data in the buffer specified by DPB bit 10, and the DPB bit does not toggle after command completion.
7-4	-----		0	Not Used
3	STOPP		0	Stop Ping-Pong Request. The host asserts this bit to suspend ping-pong buffering for this mode code. The host resets this bit to ask the device to re-enable ping-pong. The device confirms recognition of ping-pong enable or disable status by writing PPON bit 3.
2	PPEN		0	Ping-Pong Buffer Enable. The PPEN bit is initialized by the host to select buffer mode. If this bit is high, ping-pong buffering is selected. If this bit is low, indexed single buffering is selected. After reset, the host initializes this bit to logic 1 to enable ping-pong buffering for this mode code. The host asserts STOPP bit 3 to ask the device to temporarily disable ping-pong. Negating the STOPP bit asks the device to re-enable ping-pong. The device confirms ping-pong enable or disable state changes by writing the PPON bit.
1,0	-----		0	Not Used.

19.5.5. Transmit Mode Control Word

Transmit Mode Control Words apply when the command word T/$\overline{R}$ bit equals one (transmit) and the subaddress field has a value of 0 or 31 (0x1F). The descriptor Control Word defines terminal command response and interrupt behavior, and conveys activity status to the host. It is initialized by the host before terminal execution begins. Bits 8-11 cannot be written by the host; these bits are updated by the device during terminal execution, that is, when Configuration Register 1 STEX bit equals 1. The host can write bit 2 only when STEX equals zero; bits 3 and 12-15 can be written anytime. This register is cleared to 0x0000 by $\overline{MR}$ master reset. Software reset (SRST) clears just the DBAC, DPB and BCAST bits. **Following any read cycle to the Control Word address, the DBAC bit is reset.**

When single-message indexed buffering or ping-pong buffering is used instead of SMCP (Simplified Mode Code Processing), the transmit mode Control Word looks like this:

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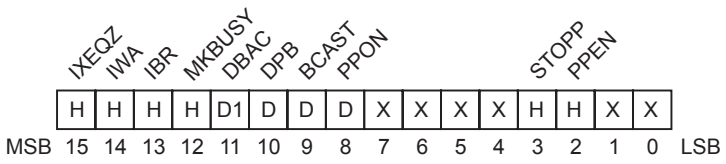


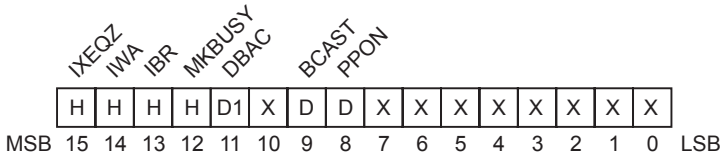
H Bit maintained by host

D Bit maintained by device

D1 Bit set by device, reset by host read cycle

X Bit is not used, may be logic 0 or 1

When SMCP applies, the number of active mode Control Word bits is reduced:



H Bit maintained by host

D Bit maintained by device

D1 Bit set by device, reset by host read cycle

X Bit is not used, may be logic 0 or 1

NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). The bit value following software reset is unchanged unless specifically indicated by an "SR" value.

Bit No.	*Mnemonic*	*RW*	*Reset*	*Function*
15	IXEQZ		0	Interrupt When Index Equals Zero. If the Interrupt Enable Register IXEQZ bit is high, assertion of this bit enables generation of an interrupt for mode code commands using indexed buffer mode when the INDX value decrements from 1 to 0. Upon completion of command processing that results in INDX = 0, when IXEQZ interrupts are enabled, an IXEQZ interrupt is entered in the Pending Interrupt Register, the $\overline{INTMES}$ output pin is asserted, and the interrupt is registered in the Interrupt Log.
14	IWA		0	Interrupt When Accessed. If the Interrupt Enable Register IWA bit is high, assertion of this bit enables interrupt generation at each instance of a valid mode code command. Upon completion of command processing, when IWA interrupts are enabled, an IWA interrupt is entered in the Pending Interrupt Register, the $\overline{INTMES}$ output pin is asserted, and the interrupt is registered in the Interrupt Log.
13	IBR		0	Interrupt Broadcast Received. If the Interrupt Enable Register IBR bit is high, assertion of this bit enables interrupt generation at each instance of a valid broadcast transmit mode code command. Upon completion of command processing, when IBR interrupts are enabled, an IBR interrupt is entered in the Pending Interrupt Register, the $\overline{INTMES}$ output pin is asserted, and the interrupt is registered in the Interrupt Log. This bit has no function if the BCSTINV bit is high in Configuration Register 1. In this case, commands to RT address 31 are not recognized as valid by the device.

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Bit No.	Mnemonic	RW	Reset	Function
12	MKBUSY		0	Make Busy. The host asserts the MKBUSY bit to respond with Busy status for commands to this mode code. This bit is an alternative to globally applying Busy status for all valid commands, enabled from the 1553 Status Bits Register. See that register description for additional information. When Busy is asserted, mode data words are not transmitted with MC16-MC31, and the DPB bit does not toggle after message completion. The MKBUSY bit is not heeded if set in the Control Word for mode code command MC8 “reset remote terminal”. For this command only, Busy is inhibited for the status response transmitted before the reset process begins.
11	DBAC		0 SR = 0	Descriptor Block Accessed. Internal device logic asserts the DBAC bit upon completion of message processing. The host may poll this bit to detect mode command activity, instead of using host interrupts. This bit is reset to logic 0 by $\overline{MR}$ master reset, SRST software reset or a read cycle to this memory address.
10	DPB		0 SR = 0	Data Pointer B. This status bit is maintained by the device and only applies for mode commands using ping-pong buffer mode. This bit indicates the buffer to be used for the next occurring mode command. When the DPB bit is logic 0, the next message will use Data Pointer A; when DPB is logic 1, the next message uses Data Pointer B. In ping-pong buffer mode, the bit is inverted after each error-free message completion. The DPB bit is not altered after messages ending in error, after illegal commands, or after messages when the terminal responds with Busy status. This bit is reset to logic 0 by $\overline{MR}$ master reset or SRST software reset; therefore the first message received after either reset will use Buffer A. This bit is “don’t care” for indexed single-buffer mode.
9	BCAST		0 SR = 0	Broadcast Received. Device logic sets this bit when a valid broadcast mode command is received having T/$\overline{R}$ bit = 1. This bit has no function if the BCSTINV bit is asserted in Configuration Register 1. In this case, RT address 31 commands are not recognized as valid by the HI-6130/21. This bit is reset to logic 0 by $\overline{MR}$ master reset or SRST software reset.
8	PPON		0	Ping-Pong Enable Acknowledge. This bit is read only and only applies for mode commands using ping-pong mode (PPEN bit 2 was initialized to logic 1 by the host after reset). The device asserts this bit when it recognizes ping-pong is active for this mode code. Before loading the transmit data buffer for this mode code, the host can ask the device to temporarily disable ping-pong by asserting STOPP bit 3. The device acknowledges ping-pong is disabled by negating PPON. The host can safely load or off-load the buffer without data collision while PPON is negated. After buffer servicing, the host asks the device to re-enable ping-pong by negating STOPP bit 3. The device acknowledges ping-pong is re-enabled by asserting PPON. If PPEN bit 2 is asserted and PPON bit 8 is negated when a new command arrives for this mode code, ping-pong disable handshake is in effect: The device applies single-buffer index mode using Data Pointer A or Data Pointer B, per DPB bit 10. The DPB bit does not toggle after command completion.

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Bit No.	*Mnemonic*	*RW*	*Reset*	*Function*
7-4	-----		0	Not Used
3	STOPP		0	Stop Ping-Pong Request. The host asserts this bit to suspend ping-pong buffering for this mode code. The host resets this bit to ask the device to re-enable ping-pong. The device confirms recognition of ping-pong enable or disable status by writing PPON bit 3.
2	PPEN		0	Ping-Pong Buffer Enable. The PPEN bit is initialized by the host to select buffer mode. If this bit is high, ping-pong buffering is selected. If this bit is low, indexed single buffering is selected. After reset, the host initializes this bit to logic 1 to enable ping-pong buffering for this mode code. The host asserts STOPP bit 3 to ask the device to temporarily disable ping-pong. Negating the STOPP bit asks the device to re-enable ping-pong. The device confirms ping-pong enable or disable state changes by writing the PPON bit.
1,0	-----		0	Not Used.

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20. REMOTE TERMINAL RT1 AND RT2 MESSAGE DATA BUFFERS

The memory structures described up to this point comprise not more than 1K words of the lower memory address space. The remaining memory is allocated by the host for message data storage, to fulfill application requirements. This section describes the remaining data structures in shared RAM that control (and result from) command processing.

By initializing the Descriptor Table, the host allocates memory space for storing data for each subaddress used in the Remote Terminal application. Each legal Receive Subaddress and each legal Transmit Subaddress are usually assigned unique buffer memory spaces. (Exception: To comply with the requirements for MIL-STD-1553 data wrap-around, it is convenient to assign the data wrap-around subaddress to use the same buffer space for both receive and transmit commands.)

As an option, data from broadcast receive commands can be stored separately from data resulting from non-broadcast receive commands. Each subaddress buffer can use any of four data storage methods offered.

Subaddress (non-mode) commands are transacted with one to 32 data words. These are stored in a data buffer in shared RAM. For receive commands, the device stores data received during message processing in the shared RAM buffer. Later, the host retrieves these data words from the buffer. In the case of transmit commands, the host has previously stored transmit data words in the transmit subaddress buffer. The device retrieves these data words for transmission while processing the transmit command.

For each complete message processed, the message data stored in the buffer is comprised of these elements:

1. Message Information Word.
2. Time-Tag Word.
3. One to 32 Data Words transmitted or received during message transaction (except no data word for mode code commands 0 - 15 decimal).

The Message Information word and Time-Tag word are generated by the device and stored in assigned buffer space to aid the host in further message processing. The Message Information word contains message type, word count and message error information. The 16-bit Time-Tag word contains the value in the device internal Time-Tag counter when the command is validated.

The host initializes the Descriptor Table entry for each subaddress or mode command to select one of four data buffering methods.

1. **Indexed (Single Buffer) Method (see 20.4).**

   A predetermined number of messages (N) is transacted using a single data buffer in shared RAM. Several host interrupt options are offered, including host interrupt when all N messages are successfully completed. This method also supports single-message mode when N is purposely initialized to zero.

2. **Double (or Ping-Pong) Buffer Method (see 20.3).**

   Successive messages alternate between two 34-word data buffers in shared RAM. Several host interrupt options are offered.

3. **Circular Buffer Mode 1 (see 20.5).**

   Buffer boundaries determine when the bulk transfer is complete. Message information and time-tag words are stored in the same buffer with data words. Several host interrupt options are offered, including host interrupt when the allocated data buffer is full.

4. **Circular Buffer Mode 2 (see 20.6).**

   The number of messages transacted defines bulk transfer progress. Message data words are stored contiguously in one buffer while message information and time-tag words are stored in a separate buffer. Several host interrupt options are offered, including host interrupt when all N messages are completed.

The data buffer options are summarized in Table 15.

Simplified Mode Command Processing.

This is a global option that applies for all mode code commands, when enabled. Mode commands have either one data word, or no data word. Instead of using data buffers for storing this limited mode command data, the message data is stored directly within the Descriptor Table. This option for mode commands is described in the section called “Mode Command Processing.”

Broadcast Data Separation

When the NOTICE2 option is enabled, data words resulting from broadcast receive commands will be stored separately from data resulting from non-broadcast receive commands when using indexed or ping-pong buffer modes. When NOTICE2 applies, all subaddresses using indexed or ping-pong modes must have an assigned 34-word broadcast data buffer in addition to the primary buffers listed above. Broadcast data segregation cannot be done using either circular buffer mode.

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Table 15. Summary of Data Buffer Modes.

Buffer Mode	Data Buffer(s) Number and Size	Message Info Word	Suitable for Mode Codes?	Primary Application
Indexed	One. Host defines size for N messages	Stored in same buffer as data	Yes, only single message mode	For transacting N (multiple) messages with optional host interrupt when done
Ping-Pong	Two 34-word buffers, one message each	Stored in same buffer as data	Yes	For transacting single messages, alternating between A and B buffers
Circular 1	One. Host defines size for N words	Stored in same buffer as data	No	For transacting messages until buffer is full / empty, optional interrupt when done
Circular 2	One. Host defines size for N messages, plus Msg Info Block	Stored in separate buffer (Msg info block)	No	For transacting N (multiple) messages with optional host interrupt when done. Data buffer holds contiguous pure data.

20.1. Subaddress Message Information Words

20.1.1. Receive Subaddress Command

For receive subaddress commands, the device stores the received data words plus two additional words. The device adds a receive subaddress Message Information Word and a Time-Tag Word to the received data words. The device stores the Message Information and Time-Tag words ahead of the data words associated with the receive command, as shown below. If message error occurs, the RT stores only the receive subaddress Message Information Word and Time-Tag Word. Once a message error is detected, the device sets the MERR bit in the receive subaddress Message Information word. When this occurs, all data words are considered invalid. Whenever the receive subaddress Message Information Word MERR bit is set, the host should disregard the record's data word(s).

Here is an example data structure for a 3-word receive command. Notice that the receive subaddress Data Pointer points to the data structure starting address, not the first data word. The data pointer is located in the receive subaddress command's Descriptor Block, fully described later:

		Data Buffer Hex Address	Word Description	Device Writes Word ...
Data pointer equals 0x0500	→	0x0500	Message Information Word	After message completion
		0x0501	Time-Tag Word	" " "
		0x0502	Data Word 1	After message completion (See **Note**)
		0x0503	Data Word 2	" " " " "
		0x0504	Data Word 3	" " " " "

Note: The data words are written after message completion when Configuration Register 2 TRXDB is 1, otherwise written when received.

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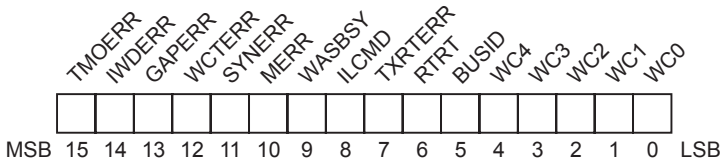

The following bits comprise the receive subaddress Message Information Word:

Bit No.	*Mnemonic*	*Function*
15	TMOERR	Time-Out Error. This bit is asserted for RT-RT receive messages when the transmitting terminal fails to start its status word and data transmission before time-out occurs, per TOSEL0-1 bits in Configuration Register 2.
14	IWDERR	Invalid Word Error. Assertion of this bit indicates Manchester error or parity error was observed in a received data word.
13	GAPERR	Gap Error. Assertion of this bit indicates bus activity was detected immediately after the last expected receive data word or that a gap occurred before all expected data words were received.
12	WCTERR	Word Count Error. This bit is asserted if command is received with less data words than the command word specifies. For example, a receive command for three data words is received with two contiguous data words.
11	SYNERR	Sync Error. This bit is asserted when an incorrect (command/status) sync type occurs in received data words.
10	MERR	Message Error. This bit is asserted when message error status change occurs during command processing. See bits 7 and 11-15 for details.
9	WASBSY	Was Busy. This bit is asserted when the terminal responds to the receive command with BUSY status, due to global BUSY bit set in 1553 Status Bits Register, or command-specific MKBUSY bit set in the descriptor table Control Word. Received data words were buffered normally.
8	ILCMD	Illegal Command Received. This bit is asserted when the Illegalization Table bit corresponding to the received command is logic 1. The Illegalization Table should only contain nonzero values when “illegal command detection” is being applied. See Section 19.2 for further information.

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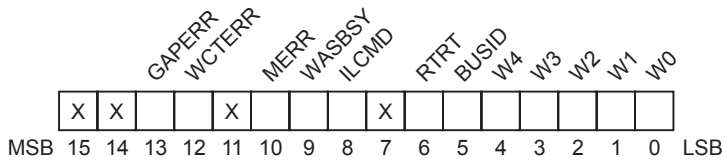
Bit No.	*Mnemonic*	*Function*
7	TXRTERR	RT-RT Transmit Remote Terminal Error. This bit is set when the terminal decodes a valid RT-RT receive command, but one of four potential errors is detected in the second command word, CW2: (1) CW2 is addressed to broadcast address RT31. (2) the CW2 T/$\overline{R}$ bit equals 0, (3) the CW2 subaddress is a mode command indicator, 00000 or 11111, or (4) CW2 has same non-broadcast terminal address as receive command word CW1. The TXRTERR bit is also set when status word received from the transmitting terminal is invalid (e.g., parity error) or bits 15:11 in the status word reflect the wrong RT address (does not match CW2).
6	RTRT	Remote Terminal to Remote Terminal Transfer. Assertion of this bit indicates the receive command was an error-free RT-to-RT transfer.
5	BUSID	Bus Identification. If this bit equals zero, message was transacted on Bus A. If bit equals one, it was transacted on Bus B.
4-0	WC4:0	Word Count. This 5-bit field contains the word count extracted from the command word. Zero indicates 32 words.

20.1.2. Transmit Subaddress Command

The external host is responsible for organizing the data packet (i.e., storing N data words) in shared RAM and initializing the applicable data pointer. The host must allocate two memory locations at the starting address of the data record for device storage of the transmit subaddress Message Information Word and Time-Tag Word.

Here is an example data structure for a 3-word transmit command. Notice that the Data Pointer points to the data structure starting address, not the first data word. The data pointer is located in the transmit subaddress command's Descriptor Block.

		Data Buffer Hex Address	**Word Description**	**Word is Written By ...**
Data pointer equals 0x0500	→	0x0500	Message Information Word	Device, after message completion
		0x0501	Time-Tag Word	" " " "
		0x0502	Data Word 1	Host, prior to terminal's data transmit
		0x0503	Data Word 2	" " " " " "
		0x0504	Data Word 3	" " " " " "



The following bits comprise the transmit subaddress Message Information Word.

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Bit No.	*Mnemonic*	*Function*
15,14	-----	Not Used.
13	GAPERR	Gap Error. Assertion of this bit indicates bus activity was detected immediately after the transmit command word, when a gap was expected.
12	WCTERR	Word Count Error. This bit is asserted if command is received with unexpected data word(s).
11	-----	Not Used.
10	MERR	Message Error. This bit is asserted when message error status change occurs during command processing. See bits 12 and 13 for details.
9	WASBSY	Was Busy Status. This bit is asserted when the terminal responds to the transmit command with BUSY status, due to global BUSY bit set in 1553 Status Bits Register, or command-specific MK-BUSY bit set in the descriptor table Control Word. No data words were transmitted.
8	ILCMD	Illegal Command Received. This bit is asserted when the Illegalization Table bit corresponding to the received command equals one. The Illegalization Table should only contain nonzero values when “illegal command detection” is being applied. See Section 19.2 for further information.
7	-----	Not Used.
6	RTRT	Remote Terminal to Remote Terminal Transfer. Assertion of this bit indicates the transmit command was an error-free RT-to-RT transfer.
5	BUSID	Bus Identification. If this bit equals zero, message was transacted on Bus A. If bit equals one, it was transacted on Bus B.
4-0	WC4:0	Word Count. This 5-bit field contains the word count extracted from the command word. Zero indicates 32 words.

20.2. Mode Command Message Information Words

Mode command data structures in shared RAM are similar to those for subaddresses. Mode codes 0 through 15 (0x0F) do not have an associated data word, so data structures for these mode code values have just a Message Information Word and Time-Tag Word. The Message Information Word is stored at the memory address specified by the descriptor table Data Pointer. Mode codes 16 through 31 (0x10 through 0x1F) have one associated data word. The Message Information Word is stored at the memory address specified by the descriptor table Data Pointer, and the Time-Tag Word is stored in the following location. The data word is stored at the memory address specified by the Data Pointer plus two locations.

20.2.1. Receive Mode Command

The receive mode command data structure contains a Message Information Word, a Time-Tag Word and may contain one Data Word. If a receive mode command has a data word, the device may apply the data as defined by MIL-STD-1553, plus store the received single mode data word at the address specified by the Data Pointer, plus two

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locations. Refer to data sheet section entitled “Mode Command Action Summary”.

Here is an example data structure for a receive mode command with data (mode code values 0x10 through 0x1F). Notice that the Data Pointer points to the data structure starting address, not the mode data word. The data pointer is located in the receive mode command’s Descriptor Block, fully described later:

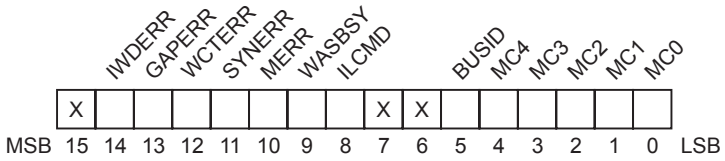
		Data Buffer Hex Address	Word Description	Word is Written By ...
Data pointer equals 0x0500	→	0x0500	Message Information Word	Device, after message completion
		0x0501	Time-Tag Word	“ “ “ “
		0x0502	Mode Data Word	“ “ “ “

Three receive mode commands with data are not defined under MIL-STD-1553B. These are MC16, MC18 and MC19 (mode codes 0x10, 0x12 and 0x13 respectively). However the device responds “in form” if illegal command detection is not used (corresponding bits in Illegalization Table are logic 0) **and** the UMCINV bit in Configuration Register 1 is logic 0.

For mode code commands without data, the data structure contains only the Message Information Word and Time-Tag Word.

Here is an example data structure for a receive mode command without data (mode code values 0x00 through 0x0F). Note: None of these receive mode commands are defined under MIL-STD-1553B but the device responds “in form” if illegal command detection is not used (corresponding bits in Illegalization Table are logic 0) and the UMCINV bit in Configuration Register 1 is logic 0. Notice that the data pointer points to the data structure starting address, the message information word. The data pointer is located in the receive mode command’s Descriptor Block, fully described later:

		Data Buffer Hex Address	Word Description	Word is Written By ...
Data pointer equals 0x0500	→	0x0500	Message Information Word	Device, after message completion
		0x0501	Time-Tag Word	“ “ “ “



The following bits comprise the receive mode Message Information Word:

Bit No.	*Mnemonic*	*Function*
15	-----	Not Used.
14	IWDERR	Invalid Word Error. Assertion of this bit indicates Manchester error or parity error was observed in a received data word.
13	GAPERR	Gap Error. Assertion of this bit indicates bus activity was detected immediately after a received mode data word or that a gap occurred before the data word was received.

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Bit No.	*Mnemonic*	*Function*
12	WCTERR	Word Count Error This bit is asserted if the command is received without expected mode data word, or with extra word.
11	SYNERR	Sync Error. This bit is asserted when incorrect (command/status) sync type occurs in received mode data word.
10	MERR	Message Error. This bit is asserted when message error status change occurs during command processing. See bits 11- 14 for details.
9	WASBSY	Was Busy Status. This bit is asserted when the terminal responds to the mode command with BUSY status, due to global BUSY bit set in 1553 Status Bits Register, or command-specific MKBUSY bit set in the descriptor table Control Word.
8	ILCMD	Illegal Command Received. This bit is asserted when the Illegalization Table bit corresponding to the received command equals one. The Illegalization Table should only contain nonzero values when “illegal command detection” is being applied. See Section 19.2 for further information.
7,6	-----	Not Used.
5	BUSID	Bus Identification. If this bit equals zero, message was transacted on Bus A. If bit equals one, it was transacted on Bus B.
4-0	MC4:0	Mode Code. This 5-bit field contains the mode code extracted from the command word.

20.2.2. Transmit Mode Command

The transmit mode command data structure contains a Message Information Word, a Time-Tag word and may contain one Data Word. For mode commands with associated data word (mode codes 16-31 decimal) the host is responsible for loading the Mode Command Data Table before transmit mode commands are received (e.g., Transmit Vector Word mode code). Two mode codes have internally generated data words: MC18 “Transmit Last Command” and MC19 “Transmit BIT Word”. For these, the device automatically transmits the data word then copies the transmitted data value to the stored data structure.

Here is an example data structure for a transmit mode command with data (mode code values 0x10 through 0x1F). This applies to MC16 “Transmit Vector Word”. Notice that the data pointer points to the data structure starting address, not the mode data word. The data pointer is located in the transmit mode command’s Descriptor Block, fully described later:

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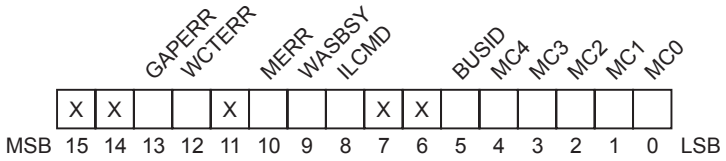
	Data Buffer Hex Address	Word Description	Word is Written By ...
Data pointer equals 0x0500 →	0x0500	Message Information Word	Device, after message completion
	0x0501	Time-Tag Word	" " " "
	0x0502	Mode Data Word	Host, prior to terminal's data transmit (except MC18, MC19 are written by the device after completion)

Three transmit mode commands with data are not defined under MIL-STD-1553B. These are MC17, MC20 and MC21 (mode codes 0x11, 0x14 and 0x15 respectively). However the device responds "in form" if illegal command detection is not used (corresponding bits in Illegalization Table are logic 0) and the UMCINV bit in Configuration Register 1 is logic 0.

For mode code commands without data, the data structure contains only the Message Information Word and Time-Tag Word. Here is an example data structure for a transmit mode command without data (mode code values 0x00 through 0x0F). Again, the data pointer points to the data structure starting address. The data pointer is located in the transmit mode command's Descriptor Block, fully described later:

	Data Buffer Hex Address	Word Description	Word is Written By ...
Data pointer equals 0x0500 →	0x0500	Message Information Word	Device, after message completion
	0x0501	Time-Tag Word	" " " "



The following bits comprise the mode transmit Message Information Word:

Bit No.	*Mnemonic*	*Function*
15,14	-----	Not Used.
13	GAPERR	Gap Error. This bit is high when bus activity was detected immediately after the mode command word, when a gap was expected.
12	WCTERR	Word Count Error This bit is asserted if command is received with unexpected data word(s).
11	-----	Not Used.
10	MERR	Message Error. This bit is asserted when message error status change occurs during command processing. See bits 12-13 for details.
9	WASBSY	Was Busy Status. This bit is asserted when the terminal responds to the mode command with BUSY status, due to global BUSY bit set in 1553 Status Bits Register, or command-specific MKBUSY bit set in the descriptor table Control Word. No mode data word was transmitted.

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Bit No.	*Mnemonic*	*Function*
8	ILCMD	Illegal Command Received. This bit is asserted when the Illegalization Table bit corresponding to the received command is logic 1. The Illegalization Table should only contain nonzero values when “illegal command detection” is being applied. See Section 19.2 for further information.
7,6	-----	Not Used.
5	BUSID	Bus Identification. If this bit equals zero, message was transacted on Bus A. If bit equals one, it was transacted on Bus B.
4-0	MC4:0	Mode Code. This 5-bit field contains the mode code extracted from the command word.

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20.3. Ping-Pong Data Buffering

20.3.1. Double Buffered (Ping-Pong) Mode

Ping-pong buffer mode is a method for storing message and time-tag information and data associated with messages. Each unique MIL-STD-1553 subaddress and mode code is assigned a pair of data buffers for transmit commands and a pair of data buffers for receive commands. The device retrieves buffer data for transmit commands, or stores buffer data for receive commands. During ping-pong operation, the device alternates message storage between Data Buffer A and Data Buffer B, on a message-by-message basis.

When a subaddress or mode command uses ping-pong data buffer mode, its 4-word descriptor block in the Descriptor Table is defined as follows:

Descriptor Word 1	Control Word
Descriptor Word 2	Data Pointer A
Descriptor Word 3	Data Pointer B
Descriptor Word 4	Broadcast Data Pointer

If Descriptor Word 1 is stored at memory address N, Descriptor Word 2 is stored at address N+1, and the other two words are stored at addresses N+2 and N+3.

Prior to starting terminal operation, enable ping-pong buffering for any subaddress (or mode code) by asserting the PPEN bit and negating the STOPP bit in the descriptor Control Word. When the device detects ping-pong is selected (PPEN = 1) and enabled (STOPP = 0), it asserts the Control Word PPON bit to confirm ping-pong is active.

During ping-pong operation, the RT determines the active data buffer at the beginning of message processing. The Control Word DPB bit indicates the data pointer to be used by the next command. DPB equals logic 0 means Data Pointer A is used next; DPB equals logic 1 means Data Pointer B is used next. For ping-pong, Data Pointers A and B are static values pointing to the first address in each buffer. At the conclusion of error-free message processing, the Control Word DPB bit is inverted so the next command “ping-pongs” to the other data buffer. Each new message to the subaddress or mode code overwrites message data and information words written two messages back. The DPB bit does not toggle when a message ends in error, or if the command was illegal, or if Busy status applied for the received command. In these cases, the next command will overwrite the same buffer. Figure 18 is a general illustration of ping-pong buffer mode. Figure 19 shows a specific example.

20.3.2. Ping-Pong Enable / Disable Handshake

Because ping-pong messages and host buffer servicing are asynchronous, there is potential for “data collision”. Here is a data collision example: The host reads data from an earlier message while the device simultaneously writes new message data to the same buffer. The host reads a mix of new and old message data. Collisions can occur for both transmit and receive messages.

A handshake scheme lets the external host asynchronously service ping-pong data buffers without data collision. To off-load or load a subaddress (or mode code) buffer, the application software performs the following sequence:

a. Host asserts the Control Word STOPP bit to suspend ping-pong operation for the subaddress. When the device recognizes STOPP bit assertion, it negates the PPON bit to acknowledge ping-pong is disabled. While PPON remains low, the last written (or read) data buffer is protected against device updates. During this time, new messages use the active buffer indicated by the Control Word DPA bit. Recurring messages repeatedly use the same buffer until ping-pong resumes.

b. Host services the last-used data buffer. If the Control Word DPB bit equals logic 1, the last command used Buffer A. The host application software off-loads or loads inactive Buffer A while the remote terminal uses active Buffer B for new message(s). If the DPB bit equals logic 0, the last command used Buffer B. The host application software off-loads or loads inactive Buffer B while the remote terminal uses active Buffer A for any new messages. Each new receive message overwrites buffer contents from the last receive message. To avoid possible data loss, host buffer servicing should be timed for completion before a second message can occur.

c. Host negates the Control Word STOPP bit to resume ping-pong operation for the subaddress. When the RT recognizes the STOPP bit is reset, it sets the PPON bit to acknowledge ping-pong is again active. As long as PPON remains set, the device alternates between data buffers A and B for new messages.

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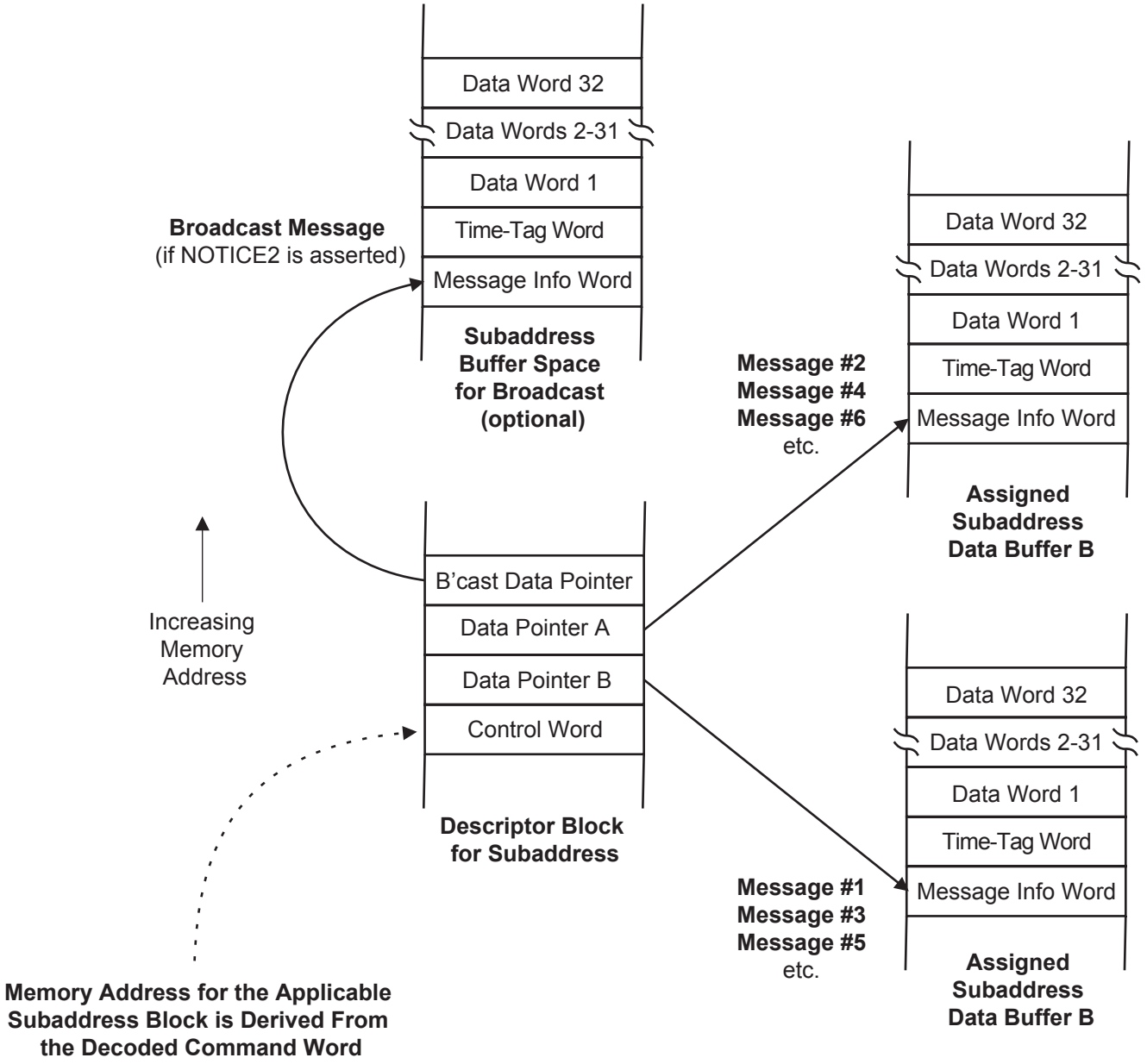

Message processing alternates between Data Buffers A and B. Upon sucessful message completion, the DPB bit in Descriptor Control Word is updated so next message uses other buffer. Buffers are overwritten every other message.

Separate buffer for broadcast messages is optional. There is no alternate buffer for successive broadcast messages.

Figure 18. Illustration of Ping-Pong Buffer Mode

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20.3.3. Broadcast Message Handling in Ping-Pong Mode

For MIL-STD-1553B Notice II compliance, a remote terminal should be capable of storing data from broadcast messages separately from non-broadcast message data. Some applications may not include this requirement. The standard does not stipulate where data separation should occur (e.g., within the RT or within the external host) so the device provides alternative strategies.

When the NOTICE2 bit in Configuration Register 1 is 1 and the BCSTINV bit is 0, ping-pong mode subaddresses (or mode codes) will buffer data words from broadcast and non-broadcast messages separately. Broadcast message information and data are stored in the broadcast data buffer; non-broadcast message information and data are stored in ping-pong buffers A and B. Since there is just one broadcast data buffer, the NOTICE2 option treats broadcast messages as exceptions to normal ping-pong mode. When using the NOTICE2 option, broadcast data buffer servicing should have high priority, because a closely following broadcast message will overwrite the broadcast buffer.

Every mode command and subaddress (including transmit subaddresses) must have an assigned valid broadcast data pointer when NOTICE2 is asserted. When the NOTICE2 bit in Configuration Register 1 is 1 and the BCSTINV bit is 0, reception of a broadcast-transmit message updates the Message Information and Time-Tag Words for the assigned broadcast buffer, but no data is transmitted on the bus. Since broadcast-transmit is not allowed, multiple transmit subaddresses may share a common “bit bucket” broadcast buffer. A two word buffer is sufficient for storing the MIW and Time-Tag Word.

When using ping-pong mode, there are two ways to handle broadcast messages, when broadcast is enabled:

Option 1 for Ping-Pong Mode Broadcast Messages:

This option isolates broadcast message information in the broadcast data buffer. If the descriptor Control Word IBR bit and Interrupt Enable Register IBR bit are both set, reception of broadcast messages generates an INTMES host interrupt. To prevent data loss, the broadcast data buffer must be serviced before the next broadcast message occurs. Broadcast messages do not affect non-broadcast message ping-pong; the Control Word DPB bit does not toggle after broadcast message completion.

Option 1 Setup: At initialization, host asserts the NOTICE2 bit in Configuration Register 1 and sets the IBR (Interrupt Broadcast Received) bit in descriptor Control Word(s). The IBR bit is asserted in the Interrupt Enable Register.

When a broadcast command is received, message information and data is stored in the broadcast data buffer and an $\overline{\text{INTMES}}$ interrupt is generated. The host must read the Interrupt Log to determine the originating subaddress (or mode code), then service the broadcast data buffer for that subaddress (or mode code) before another broadcast message to the same subaddress (or mode code) arrives.

Option 2 for Ping-Pong Mode Broadcast Messages:

The second alternative stores both broadcast and non-broadcast message information in the ping-pong data buffers A and B. IWA interrupts can signal arrival of any new message. The RT handles broadcast messages just like non-broadcast messages, except the Message Information Word BCAST bit is asserted to identify broadcast messages during host buffer servicing. All messages toggle the Control Word DPB bit in message post-processing. For Notice II compliance, separation of broadcast and non-broadcast data occurs within the host.

Option 2 Setup: At initialization, host negates the NOTICE2 bit in Configuration Register 1. If IWA interrupts are used, the host asserts the descriptor Control Word IWA (Interrupt When Accessed) bit 14 and the corresponding bit is asserted in the Interrupt Enable Register. Using this option, the IBR interrupt is probably not used.

The host typically services the ping-pong data buffers A and B whenever a message is transacted. Using the setup above, this occurs whenever the subaddress IWA interrupt generates an $\overline{\text{INTMES}}$ interrupt output for the host. The host must read the Interrupt Log to determine the originating subaddress or mode code. The applicable data buffer is indicated by the DPB bit in the Receive Control Word. The Message Information Word BCAST bit is asserted if the message was broadcast.

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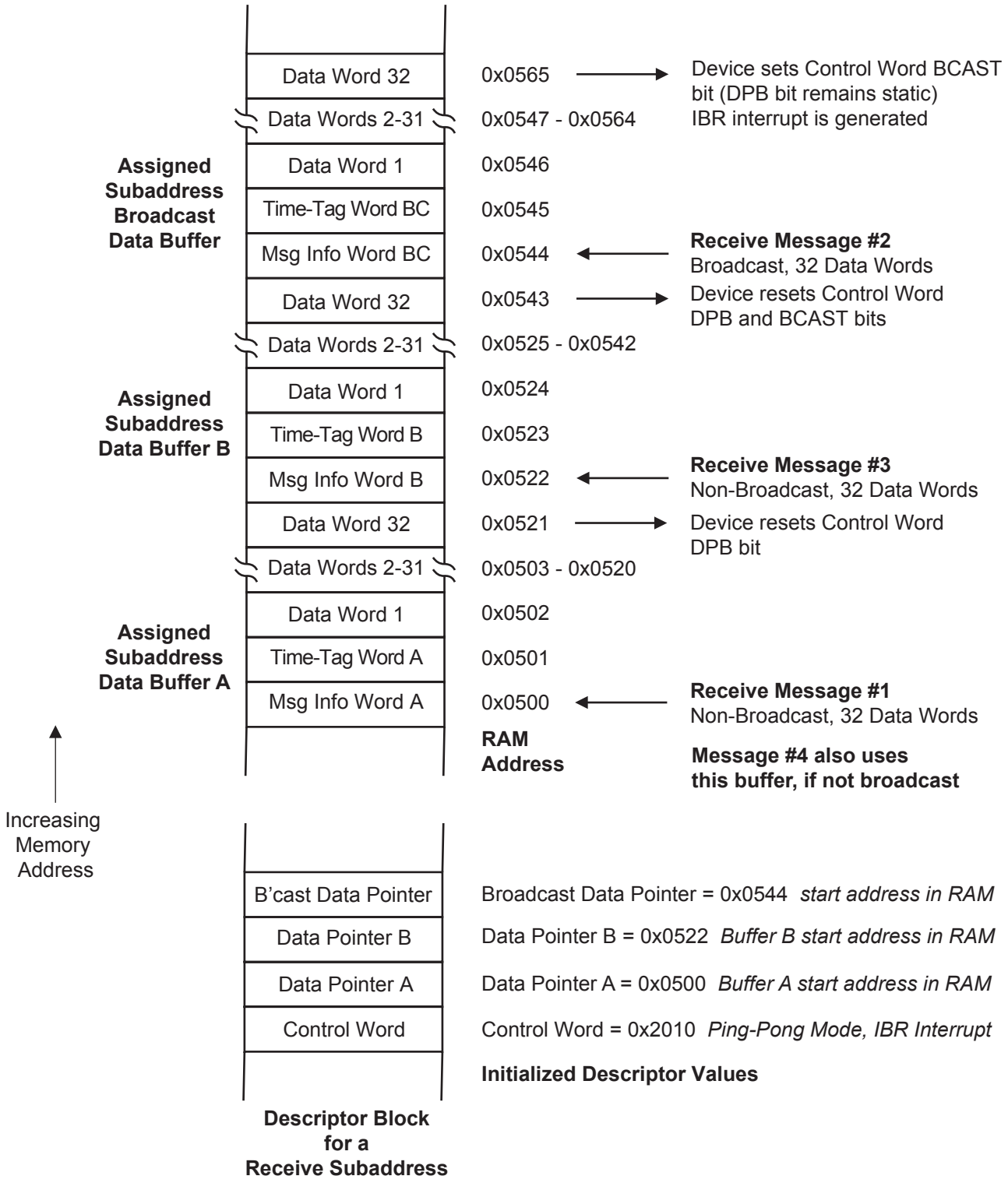

Following reset (which resets Control Word DPB bit), the subaddress transacts 4 commands of 32 data words each. The NOTICE 2 option is enabled so the device segregates data from broadcast and non-broadcast messages. Message #2 is a broadcast command, while the other three messages are non-broadcast. Notice that the broadcast message does not affect DPB bit, but the following message resets BCAST bit. The interspersed broadcast command does not affect alternation between Buffer A and Buffer B.

Figure 19. Ping-Pong Buffer Mode Example for a Receive Subaddress

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20.4. Indexed Data Buffer Mode

Also called “single buffer mode”, indexed buffering is one method for storing message and time-tag information and data associated with messages. Buffer mode is selected for each subaddress or mode code in the Descriptor Table Control Words. Indexed mode is enabled when Control Word PPEN, CIR1EN and CIR2EN bits are all zero.

When a subaddress or mode command uses the indexed data buffer mode, its 4-word descriptor block in the Descriptor Table is defined as follows:

Descriptor Word 1	Control Word
Descriptor Word 2	Data Pointer A
Descriptor Word 3	INDX Index Word
Descriptor Word 4	Broadcast Data Pointer

If Descriptor Word 1 is stored at memory address N, Descriptor Word 2 is stored at address N+1, and the other two words are stored at addresses N+2 and N+3.

As the name implies, all message information and data is stored in a single buffer, indexed by descriptor word Data Pointer A. The descriptor Control Word DPB bit is “don’t care”. The host initializes the desired message count in descriptor INDX word. During message processing, the device retrieves or stores data words from the address specified by descriptor Data Pointer A, automatically incrementing the pointer address as words are read or stored. Data Pointer A is updated during command post-processing with the current buffer address unless the message index count in descriptor INDX (word 3 of descriptor block) decrements to zero upon completion of the message. Figure 20 is a general illustration of indexed single buffer mode. Figure 21 shows a specific example.

To set up a terminal subaddress to buffer multiple messages, the host writes the desired index count (INDX) to subaddress descriptor word 3. The initial INDX value ranges from zero to 3FF hex (1023) messages. The device decrements the INDX count each time an error-free message is transacted, and the data pointer is updated to the first memory address to be used for the next message. If INDX decrements from one to zero and Control Word IXEQZ bit 15 is asserted, the IXEQZ bit is set in the Interrupt Pending Register. If the corresponding bit in the Interrupt Enable Register is asserted, an $\overline{\text{INTMES}}$ interrupt is generated when INDX decrements from one to zero.

INDX counter decrement does not occur if the command was illegalized or if INDX already equals zero. Once INDX equals zero, further commands will overwrite the last-written data buffer block and the data pointer value is not updated after successful message completion.

When using Index Mode with a non-zero INDX value, the host must remember the initial Data Pointer A address. The Data Pointer A word is not automatically re-initialized to the buffer start address when INDX decrements from 1 to 0.

20.4.1. Single Message Mode

When Index Mode is initialized with an INDX value of zero, the subaddress or mode code is operating in “Single Message Mode”. Here, the same data block is repeatedly over-read (for transmit data) or overwritten (for receive or broadcast data). The DPA pointer is not updated at the end of each message. The chief advantage of single message mode is simplicity. In comparison to other data buffering options, the single message buffer uses an absolute minimum amount of memory space. The IXEQZ interrupt cannot be used for this scheme (INDX is always zero) but IWA interrupts may be used. Single message mode is best suited to synchronous data transfer where the host processor can reliably read or write new message data prior to the start of the next message to the same subaddress or mode code.

20.4.2. Broadcast Message Handling in Index Mode

For MIL-STD-1553B Notice II compliance, a remote terminal should be capable of storing data from broadcast messages separately from non-broadcast message data. Some applications may not include this requirement. The standard does not stipulate where data separation should occur (e.g., within the RT or within the external host) so the device supports alternative strategies.

When the NOTICE2 bit is logic 1 in Configuration Register 1, broadcast message data is stored in a broadcast data buffer assigned for the subaddress or mode command. Each subaddress or mode command must have an assigned, valid non-zero broadcast buffer address. Non-broadcast message data is stored in Data Buffer A.

There are two ways to deal with broadcast messages in indexed buffer mode:

Option 1 for Index Mode Broadcast Messages:

The first alternative isolates broadcast message information in the broadcast data buffer. If the descriptor Control Word IBR bit and Interrupt Enable Register IBR bit are both set, reception of broadcast messages generates an $\overline{\text{INTMES}}$ interrupt to the host. The broadcast data buffer

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must be processed before another broadcast message arrives to prevent loss of data. Broadcast messages do not decrement the INDX register, and Data Pointer A is not updated in message post-processing. This scheme may be well suited for Single Message Mode (INDX = 0) when the host can reliably service either the broadcast data buffer or data buffer A before the next receive message arrives for the same subaddress (or mode code).

Option 1 Setup: At initialization, host asserts NOTICE2 bit in Configuration Register 1 and sets the Control Word IBR (Interrupt Broadcast Received) bit for each index mode descriptor block. The IBR bit is also asserted in the Interrupt Enable Register.

When a broadcast command is received, message information and data are stored in the broadcast data buffer. If descriptor Control Word IBR bit is set, an $\overline{\text{INTMES}}$ interrupt is generated. The host must read the Interrupt Log to determine the originating subaddress (or mode code) then service the broadcast data buffer for that subaddress (or mode code) before the next broadcast message to the same subaddress (or mode code) arrives.

Option 2 for Index Mode Broadcast Messages:

The second alternative stores both broadcast and non-broadcast message information in data buffer A. Optional IBR interrupts can signal arrival of broadcast messages. The RT handles broadcast messages just like non-broadcast messages, except the Message Information Word BCAST bit is asserted to identify broadcast messages during host buffer servicing. All messages decrement the INDX register and Data Pointer A is updated in message post-processing. This scheme is compatible with Single Message Mode or conventional N-message indexing. For Notice II compliance, separation of broadcast and non-broadcast data occurs within the host.

Option 2 Setup: At initialization, host negates the NOTICE2 bit in Configuration Register 1. If broadcast interrupts are used, the Control Word IBR (Interrupt Broadcast Received) bit is asserted at each desired index mode descriptor block. The IBR bit is also asserted in the Interrupt Enable Register.

Using option 2, the host has several options for servicing data buffer A: (a) when INDX decrements from one to zero (using the IXEQZ interrupt), (b) when a broadcast message occurs (using the IBR interrupt) or (c) when any message arrives (using the IWA interrupt).

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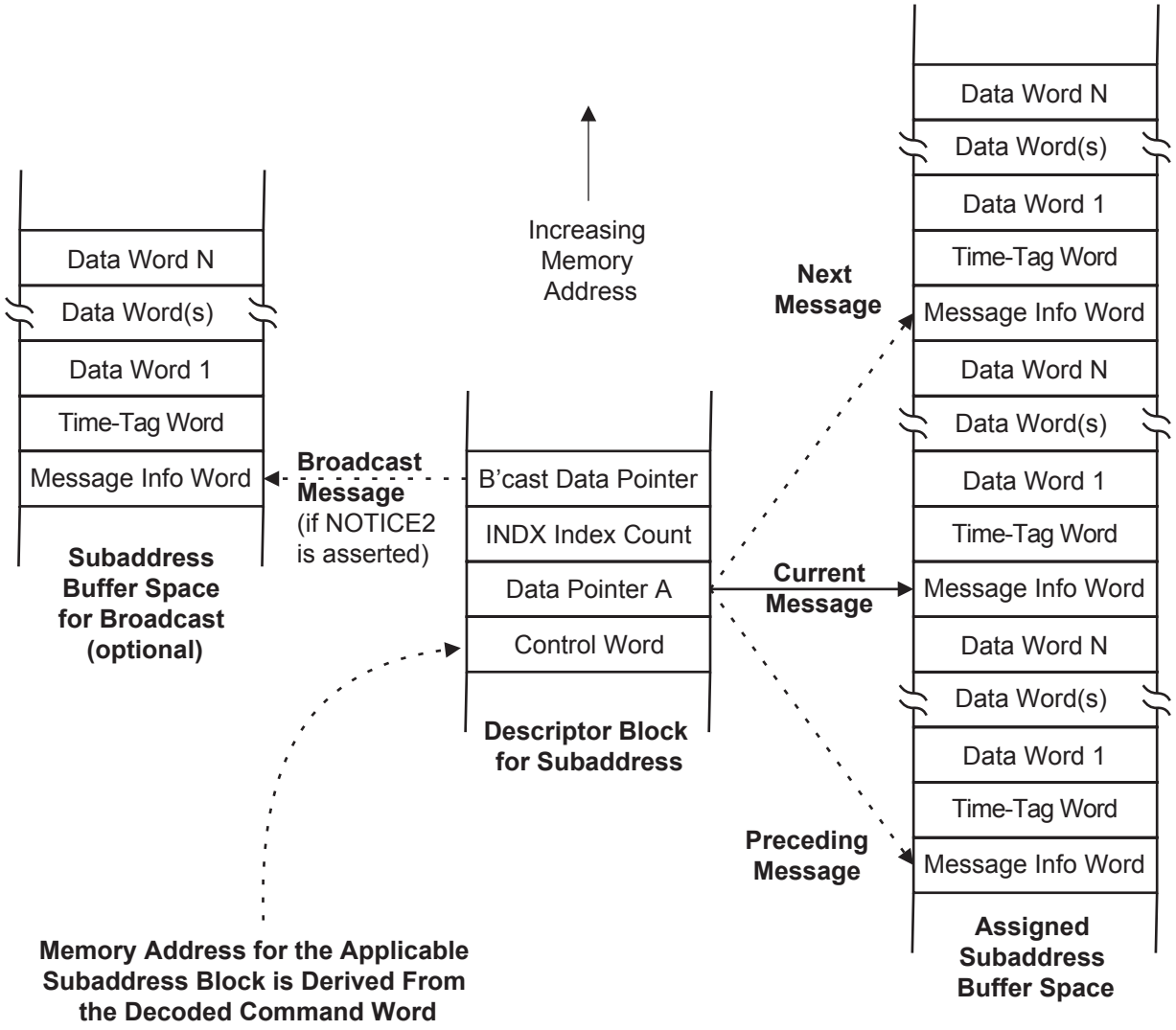

Upon successful message completion, if non-zero the INDX count in Descriptor Word 3 is decremented. If decremented result is non-zero, Data Pointer A is adjusted so next message is stored above just-completed message. If decremented INDX is zero, Data Pointer A remains static and IXEQZ interrupt occurs if enabled in Control Word.

Figure 20. Illustration of Indexed Buffer Mode

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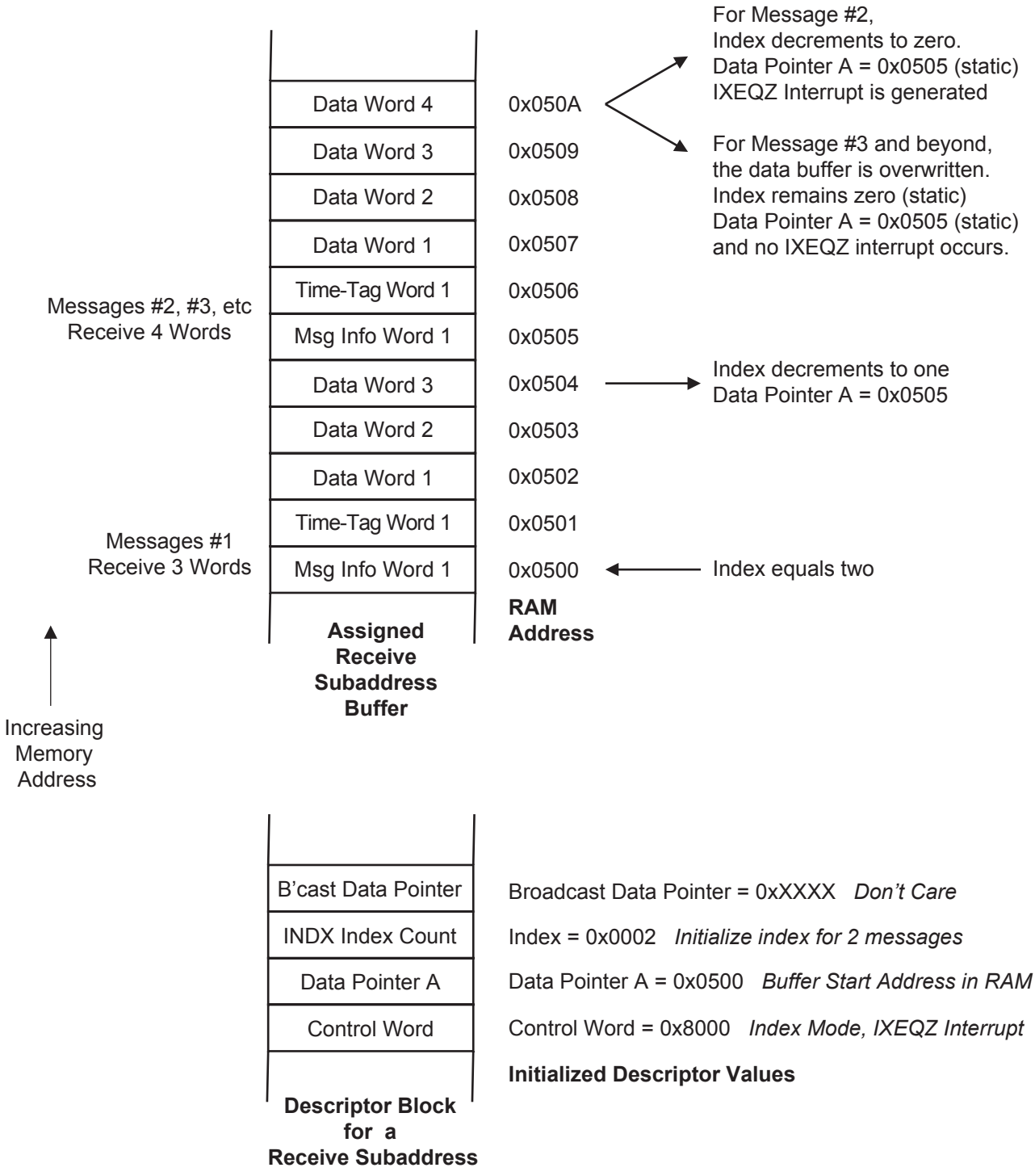

Figure 21. Indexed Buffer Mode Example for a Receive Subaddress (broadcast disabled)

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20.5. Circular Buffer Mode 1

The device offers two circular data buffer modes as alternatives to ping-pong and indexed buffering. These circular buffer options only apply for subaddress commands, not mode code commands. Circular buffering simplifies software servicing of the remote terminal when implementing bulk data transfers. A circular buffer mode can be selected for any subaddress by properly initializing its descriptor Control Word. Circular Buffer Mode 1 is selected when descriptor Control Word PPEN and CIR2EN bits are both 0, and the CIR1EN bit is logic 1.

When a subaddress uses circular buffer mode 1, its four word block in the Descriptor Table is defined as follows:

Descriptor Word 1	Control Word
Descriptor Word 2	SA (Buffer Start Address)
Descriptor Word 3	CA (Buffer Current Address)
Descriptor Word 4	EA (Buffer End Address)

If Descriptor Word 1 is stored at memory address N, Descriptor Word 2 is stored at address N+1, and the other two words are stored at addresses N+2 and N+3.

Figure 22 provides a generalized illustration of Circular Buffer Mode 1, while Figure 23 shows a specific example. Circular Buffer Mode 1 uses a single user-defined buffer that merges all transmit or receive data, along with message information. Two words (Message Information and Time-Tag) are stored at the beginning of the block for each message, followed by the message data word(s). The Mode 1 buffer pointers roll over (are reset to their base addresses) when the allocated data buffer memory is full.

For each valid receive message, the device enters a Message Information word, Time-Tag word and data word(s) into the circular receive buffer. For each valid transmit message, the device enters a Message Information word and a Time-Tag word into reserved memory locations within the circular transmit buffer. The device automatically controls the wrap around of circular buffers.

Two pointers define circular buffer length: start of buffer (lowest address) and end of buffer (highest address). User specifies the start of buffer (SA) by writing the lowest address value into the second word of a unique subaddress descriptor block. The user defines the bottom of the buffer (EA) by writing the highest address value to the fourth word of that unique descriptor block. Both SA and EA remain static during message processing. The third word in the descriptor block identifies the current address CA (i.e., last accessed address plus one). The circular buffer wraps to the start address after completing a message that results in CA being greater than or equal to EA. If CA increments past EA during message processing, the device will access memory addresses greater than the EA value. Reserve 33 address locations past the EA address to accommodate a worst-case 32 data word message with a record starting at address = EA minus 1.

Each receive subaddress and transmit subaddress may have a unique circular buffer assignment. The RT decodes the command word T/$\overline{R}$ bit, subaddress field and word count / mode code field to select the unique command descriptor block containing the Control Word, SA pointer, CA pointer and EA pointer.

For receive messages, the device stores the Message Information word to the address specified by CA, the Time-Tag word into CA+1 and the data into the next “N” locations starting with CA+2. For transmit messages, the device stores the Message Information word to the address specified by CA and the Time-Tag word into CA+1. Retrieval of data for transmission starts at address CA+2. When entering multiple transmit command data packets into the circular buffer, delimit each data packet with two reserved memory locations. The device stores the Message Information word and Time-Tag word into the reserved locations when processing the command.

Message processing for all commands begins with the device reading the unique descriptor block for the subaddress or mode code specified by the T/$\overline{R}$ bit, subaddress and word count fields in the received command word.

For receive messages, the device stores “N” received data words in the circular data buffer. The first data word received is stored at the location specified by the CA pointer +2. After message completion, the device stores the Message Information word and Time-Tag words to addresses CA and CA+1 respectively. If no errors were detected, the device updates descriptor CA register. If the next address location (last stored data word +1) is less than or equal to EA, CA is updated to (last stored address +1). If the next address location (last stored data word +1) is greater than EA, the data buffer is full (or empty); CA is updated to the SA value. If descriptor Control Word IXEQZ bit is asserted (and if Interrupt Enable Register IXEQZ bit is asserted) the device generates an interrupt to indicate full receive buffer by asserting the $\overline{INTMES}$ interrupt output.

Although all messages store Message Information and Time-Tag words, no data is stored if the message ended with error, or if the Busy status bit was set or if the commend was illegal (example: illegalized word count).

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Such messages do not update CA, so the next message overwrites the same buffer space.

For transmit commands, the device begins transmission of data retrieving the first data word stored at address CA+2. (Reminder: addresses CA and CA+1 are reserved for the Message Information and Time-Tag words.) When message processing is complete, the device writes the Message Information and Time-Tag words into the buffer. If no errors were detected, the device updates descriptor CA register. If the next address location (last retrieved data word +1) is less than or equal to EA, CA is updated to (last retrieved address +1). If the next address location (last retrieved data word +1) is greater than EA, the transmit data buffer is empty; CA is updated to the SA value. If the descriptor Control Word IXEQZ bit is asserted (and if the Interrupt Enable Register IXEQZ bit is asserted) the device indicates "transmit buffer empty" by asserting the $\overline{\text{INTMES}}$ interrupt output.

Circular Buffer Mode 1 does not support NOTICE2 segregation of broadcast data, even when the NOTICE2 bit equals 1 in Configuration Register 1. Data from broadcast and non-broadcast receive commands is stored in the same buffer. The BCAST bit in the Message Information Word reflects broadcast or non-broadcast status for each stored message. If broadcast messages are not expected during data block transmission, the host can illegalize broadcast commands for the subaddress. Broadcast illegalization can be done either permanently, or only when data block transmission is scheduled.

For transmit subaddresses using Circular Buffer Mode 1, occurrences of broadcast-transmit commands to RT31 do not result in bus transmission. However these messages update the Message Information Word addressed by the Current Address (CA) pointer (and following Time-Tag Word) but afterwards, the CA pointer remains unchanged. The next transmit command to the same subaddress, whether broadcast or not, overwrites the Message Information and Time-Tag Word locations written by the previous broadcast transmit command.

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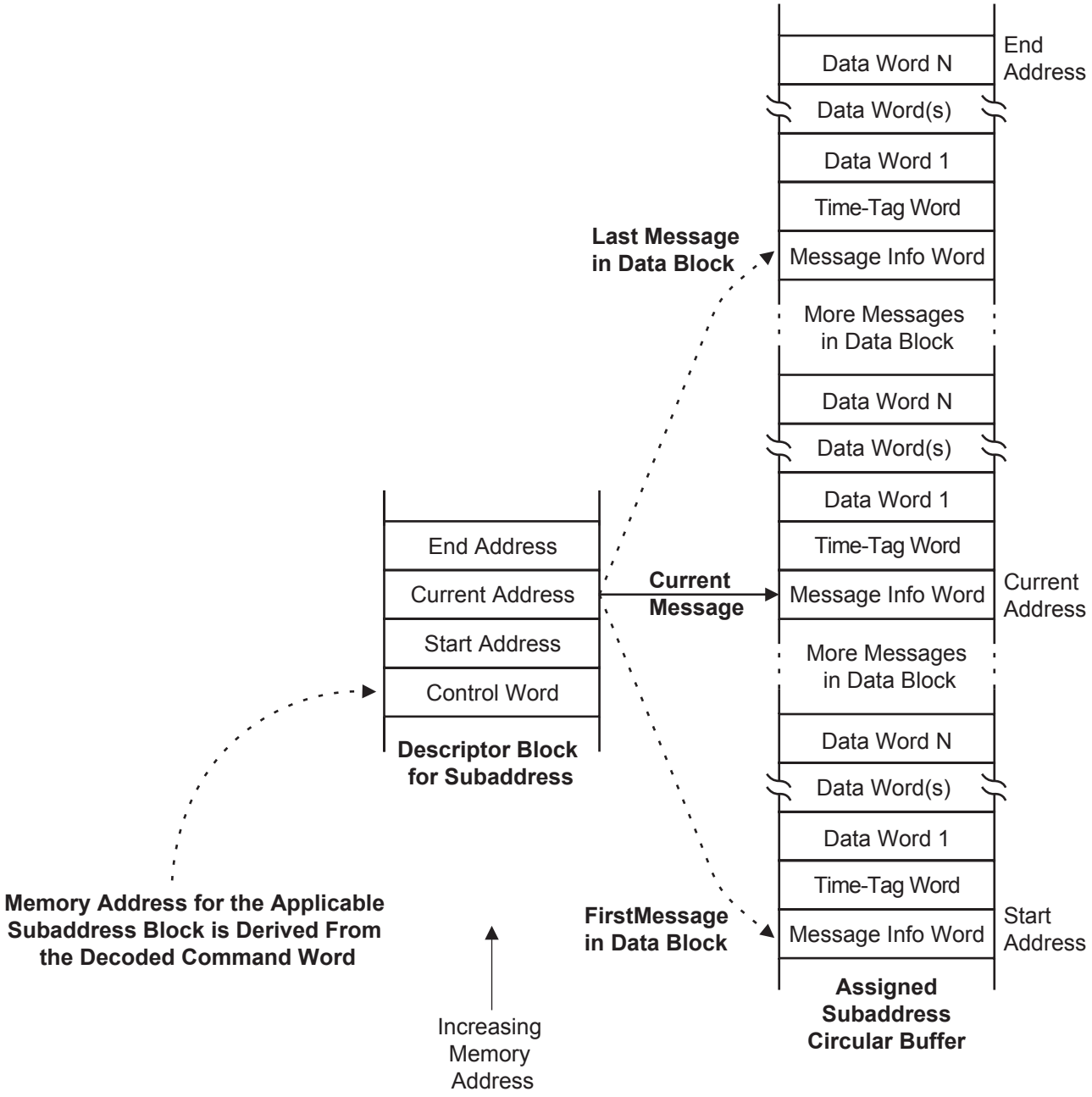

Descriptor block is initialized so Current Address equals buffer Start Address. After each successful message transaction, Current Address is adjusted to point past last data word accessed. If adjusted Current Address points past End Address, the Current Address is reinitialized to match Start Address and an optional interrupt is generated to notify host that the pre-determined data block was fully transacted.

Figure 22. Illustration of Circular Buffer Mode 1

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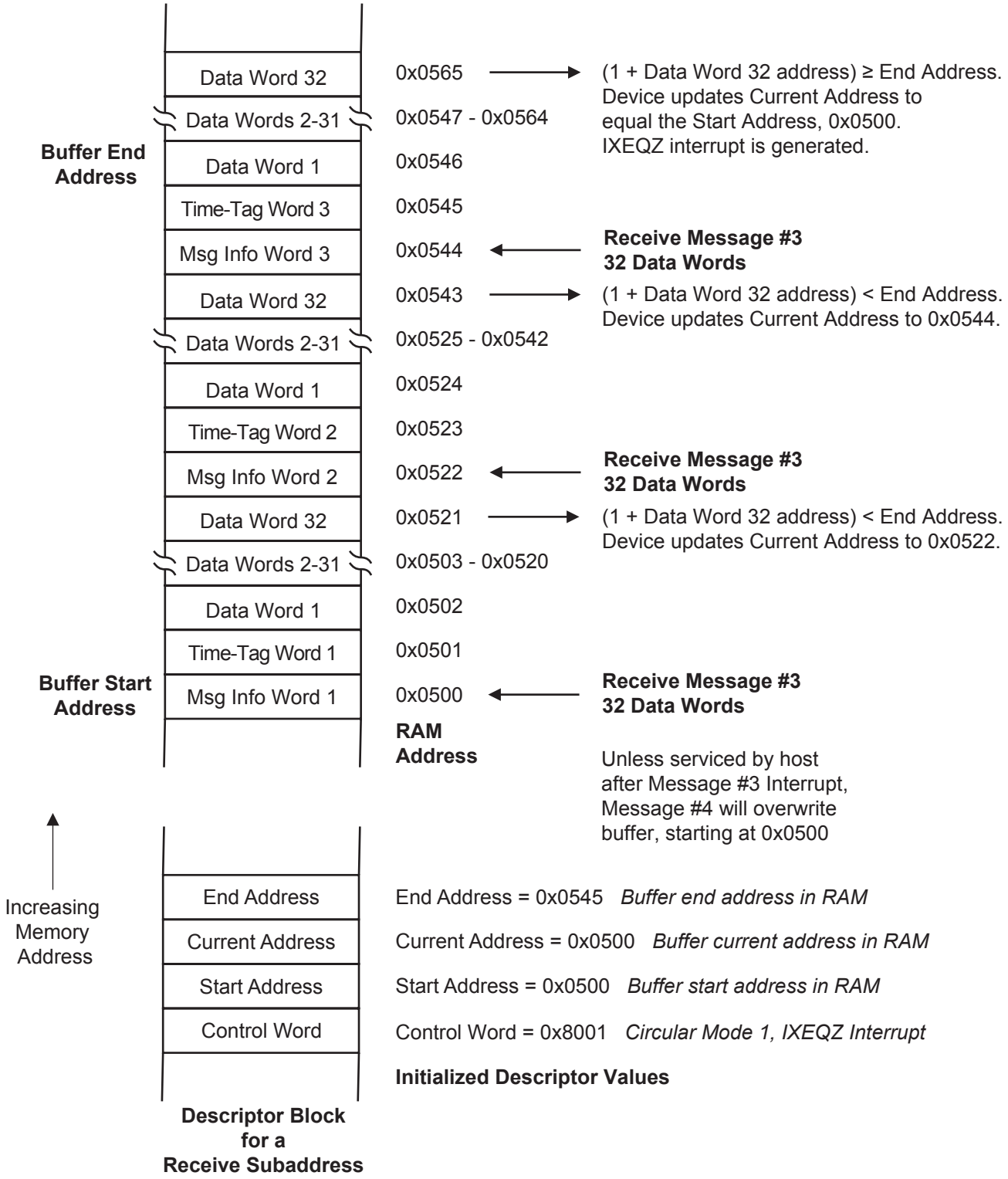

Unlike Indexed mode, Data Block completion is based on Buffer Full / Buffer Empty, not number of messages. Buffer size was purposely sized to yield remaining capacity after 2 full-count messages, to illustrate device behavior. The circular buffer should have a 33-word pad beyond its End Address to deal with buffer overrun without data loss.

Figure 23. Circular Buffer Mode 1 Example for a Receive Subaddress

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20.6. Circular Buffer Mode 2

Circular Buffer Mode 2 segregates message data and message information in separate host-defined buffers. Separating data from message information simplifies the host software that loads or unloads the data to or from the buffer. After a predetermined number of messages has been transacted, buffer address pointers for data and message information are automatically reset to their base addresses. Figure 24 is a generalized illustration of Circular Buffer Mode 2, while Figure 25 shows a specific example.

Circular Buffer Mode 2 is selected when the Control Word PPEN bit is zero and the CIR2EN bit is logic 1. When the CIR2EN bit is high, the CIR1EN bit is don't care. The descriptor Control Word DPB bit is not used.

Any receive subaddress using circular buffer mode 2 has two circular buffers: a data storage buffer and a message information buffer. A separate buffer pair may be used for transmit commands to the same subaddress, if it also uses circular buffer mode 2. Each transmit and receive subaddress using circular buffer mode 2 may have unique data buffer and message info buffer assignments. Careful management (involving the bus controller) may allow buffer sharing, as long as multiple message sequences to a given subaddress are not interrupted by messages to other subaddresses that use the same buffer space.

When a subaddress uses circular buffer mode 2, its Descriptor Table 4-word block is defined as follows:

Descriptor Word 1	Control Word
Descriptor Word 2	SA (Buffer Start Address)
Descriptor Word 3	CA (Buffer Current Address)
Descriptor Word 4	MIBA (Message Info Buffer Addr)

If Descriptor Word 1 is stored at memory address N, Descriptor Word 2 is stored at address N+1, and the other two words are stored at addresses N+2 and N+3. The first word in the descriptor block is the Control Word. The second and third words in the descriptor are the Start Address (SA) and Current Address (CA) pointers. The Message Information Buffer Address (MIBA) points to the storage location for the Message Information Word from the next occurring message.

Each time a message is completed, the device writes a new Message Information Word and Time-Tag Word in the MIB (Message Information Buffer) at the MIBA address and following location, respectively. The MIBA pointer is not updated if message error occurred, if the Busy status bit was set, or if the command was illegalized (for example an illegal word count expressed in the command word.) For these situations, the Message Information and Time-Tag words are still written, but MIB updates for the following message will overwrite the just-written Message Information and Time-Tag word addresses.

For error-free receive messages, received data words are stored in the data buffer after message completion, starting at the CA address value. The CA value is then updated for next-message readiness.

After writing the two MIB words, the device updates the MIBA value to show the buffer address to be used by the next message. Until the predetermined number of error-free messages is transacted, the MIBA value is double-incremented at each update. Before updating the MIBA in Descriptor Word 4, the pre-existing MIBA value is incremented once then checked for 'full count," occurring when all N low-order address bits initialized to zero (explained below) become N "one" bits. Full count means the predetermined number of successful messages was completed. When this occurs, the CA and MIB pointers are automatically written to their initialized values by the device.

To preserve data integrity, the TRXDB bit should be set in Control Register 2 to avoid storing incomplete data from messages resulting in error. With TRXDB asserted, the host is not bothered by message retries caused by errors. The Buffer Empty/Full interrupt (if enabled) is generated only upon successful transaction of the entire N-message data block.

To initialize Circular Buffer Mode 2, the host must know the number of messages to be transacted, always a power of two: 1, 2, 4, 8, 16, 32, 64, 128, 256 or 512 messages. The host writes descriptor Control Word bits 7:4 with an encoded 4-bit value to set the fixed number of messages to be transacted. This is illustrated in Table 16. The host initializes the descriptor block MIBA pointer with a Message Information Buffer starting address. Because the MIB stores two words for each message, the allocated MIB space should equal 2x the number of messages.

The initially-loaded MIB base address value is restricted. Some lower bits of the starting address must be zero so the device can restore the MIBA pointer to the initial MIB base address after the predetermined message count is transacted. As illustrated in Table 16, the required number of logic-0 bits depends on the message count. Initializing the MIBA base address with more trailing zeros than indicated is acceptable; initializing less trailing zeros will cause malfunction.

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Allocated space in the data buffer (see column 3, Table 16) assumes each message has the maximum 32 data words. If messages contain less than 32 words, the data buffer size can be reduced. Since Circular Buffer Mode 2 counts messages, values in all remaining Table 16 columns remain valid when message word count is reduced.

The host may read the MIBA value to determine the number of messages that have occurred since initialization. By reading the initially-zeroed lower bits of the MIB Address, the host may determine the number of the next occurring message.

From Table 16, a block of 128 messages requires 8 trailing zeros in the initial MIBA address, for example, 0x0F00. After each message is completed, the MIBA value is updated (0x0F02, 0x0F04, etc.) The device detects message block completion when all required initially-zero trailing address bits equal 1 after MIBA is incremented once. In our example, MIBA would increment from 0x0FFE to 0x0FFF. When “full count” occurs, the device updates MIBA to the original value (e.g., 0x0F00) and copies the SA starting address value to CA current address register, ready for buffer service by the host. The device optionally generates a “buffer empty-full” interrupt for the host when block transfer is completed.

During block transfer, the host can read the MIBA value to determine the number of additional messages needed before the N-message data block is complete.

Message processing for all commands begins with the RT reading the unique descriptor block for the subaddress specified by the T/$\overline{R}$ bit, subaddress and word count fields in the received command word.

Table 16. Circular Buffer Mode 2 (Initialization factors based on message block size)

Number of Messages	Control Word Bits 7:4 CIR2ZN Field	Required Data Space if 32 Words / Msg	Required MIB Space, 2 Words / Msg	Initial MIBA Value, Showing the Required Leading and Trailing Zeros
2	0010 (2)	64	4	0xxxxxxxxxxxx00
4	0011 (3)	128	8	0xxxxxxxxxxx000
8	0100 (4)	256	16	0xxxxxxxxxx0000
16	0101 (5)	512	32	0xxxxxxxxx00000
32	0110 (6)	1,024	64	0xxxxxxxx000000
64	0111 (7)	2,048	128	0xxxxxxx0000000
128	1000 (8)	4,096	256	0xxxxxx00000000
256	1001 (9)	8,192	512	0xxxxx000000000
512	1010 (A)	16,384	1,024	0xxxx0000000000

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For receive subaddresses using Circular Buffer Mode 2, the device stores received data words in the circular data buffer. The first data word received for each message is stored at the location indicated by the CA pointer. After the correct number of words is received (as specified in the command word) the device writes Message Information and Time-Tag words in the Message Information Buffer then updates the descriptor CA Current Address and MIBA Message Information pointers for next-message readiness. If the predetermined total number of messages has not yet been transacted, MIBA points to the next location in the message information buffer and CA points to the next location in the data buffer. If the completed message is the last message in the block, the CA current (data) address and MIBA message Information pointers are reinitialized to their base address values. (Control Word bits 7:4 tell the device how many MIBA lower bits to reset.) If the descriptor Control Word IXEQZ bit is asserted (and if the Interrupt Enable Register IXEQZ bit is asserted) the device generates a Buffer Full / Empty interrupt, asserting the $\overline{\text{INTMES}}$ interrupt output.

For transmit subaddresses using Circular Buffer Mode 2, the device transmits data from the assigned RAM buffer, starting at the location specified by the CA pointer. The first data word transmitted is stored at the location specified by the CA pointer. After all data words are transmitted (as specified in the command word) the device writes Message Information and Time-Tag words in the Message Information Buffer then updates the descriptor CA Current Address and MIBA Message Information pointers for next-message readiness. If the predetermined total number of messages has not yet been transacted, MIBA points to the next location in the message information buffer and CA points to the next location in the data buffer. If the completed message is the last message in the block, the CA current (data) address and MIBA message Information pointers are reinitialized to their base address values. (Control Word bits 7:4 tell the device how many MIBA lower bits to reset.) If the descriptor Control Word IXEQZ bit is asserted (and if the Interrupt Enable Register IXEQZ bit is asserted) the device generates a Buffer Full / Empty interrupt, asserting the $\overline{\text{INTMES}}$ interrupt output.

Circular Buffer Mode 2 does not support NOTICE2 segregation of broadcast data, even when the NOTICE2 bit equals 1 in Configuration Register 1. Data words from broadcast receive commands are stored in the same buffer with data from non-broadcast receive commands. The BCAST bit in the Message Information Word reflects broadcast or non-broadcast status for each stored message. If broadcast messages to the subaddresss are not expected during data block transmission or will result in data block error, the host can illegalize broadcast commands for the subaddress, either permanently or only when block transmission is scheduled.

For transmit subaddresses using Circular Buffer Mode 2, occurrences of broadcast-transmit commands to RT31 do not result in bus transmission. However these messages update the Message Information Word addressed by the Message information Block (MIB) pointer (and the following Time-Tag Word) but afterwards, the MIB and CA pointers remain unchanged. The next transmit command to the same subaddress, whether broadcast or not, overwrites the Message Information and Time-Tag Word locations written by the previous broadcast transmit command.

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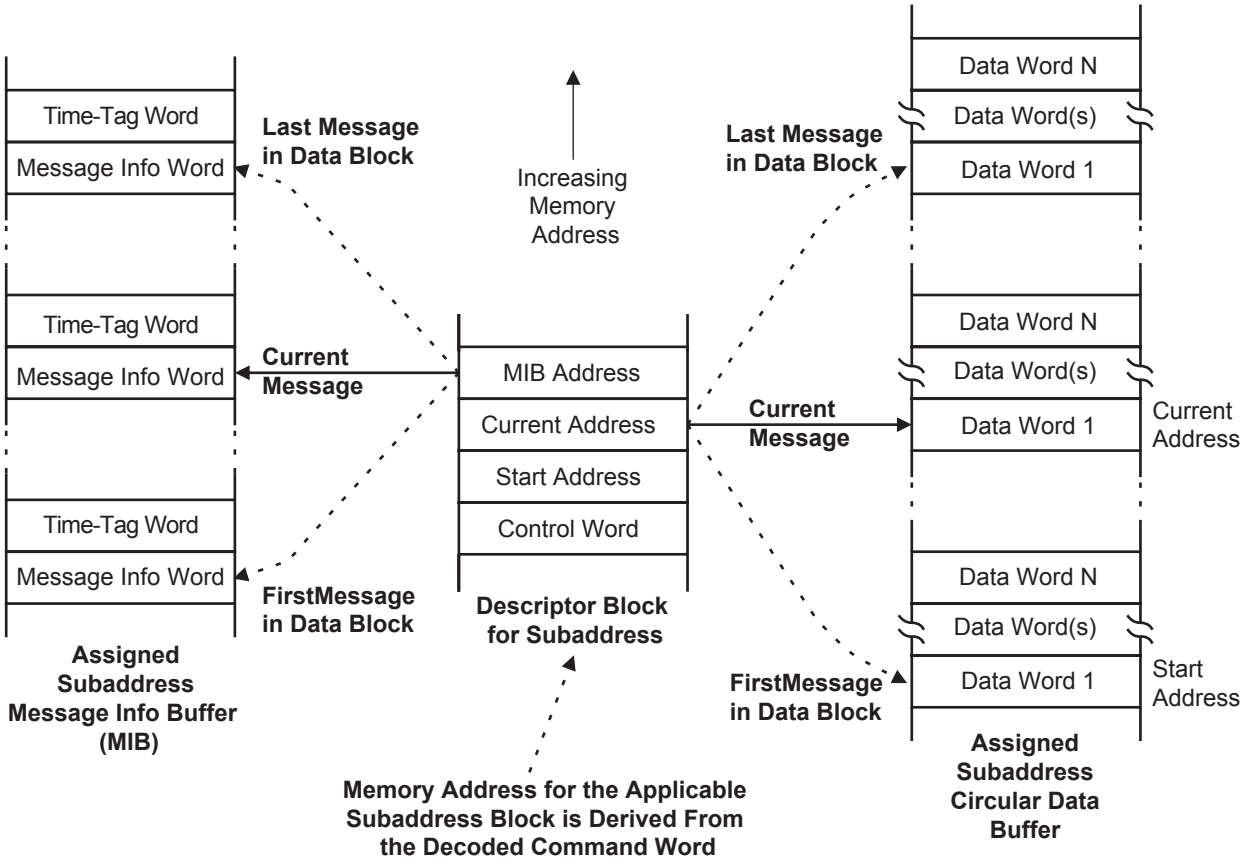

Segregated storage for data and message information simplifies host loading / offloading of buffered data. Descriptor MIB Address tracks number of messages. Full count occurs when N initialized 0-bits become N 1-bits. When full number of messages in block is transacted, an optional interrupt is generated to notify host.

Figure 24. Illustration of Circular Buffer Mode 2

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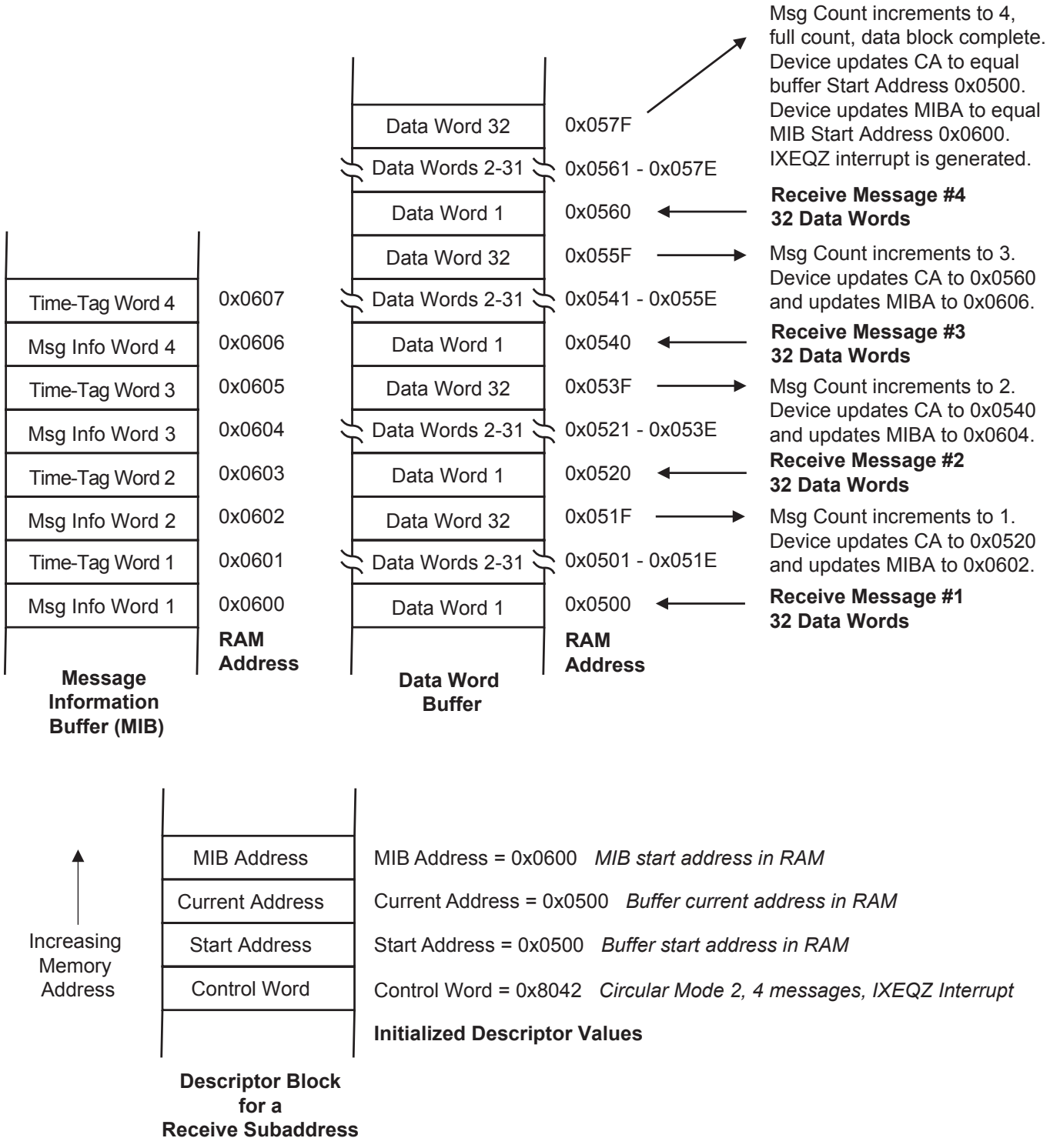

Data Block completion is based on number of messages, not Buffer Full or Buffer Empty.
Example is set to successfully transact four 32 data word receive messages, then generate IXEQZ interrupt for host.
The data buffer requires minimal processing by host because message information words are stored separately in MIB.

Figure 25. Circular Buffer Mode 2 Example for a Receive Subaddress

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21. REMOTE TERMINAL RT1 AND RT2 MODE COMMAND PROCESSING

21.1. General Considerations

The device provides decoding for all mode code combinations, consistent with MIL-STD-1553B requirements. Several mode command options are provided to suit any application requirement:

In Configuration Register 1, the option bit UMCINV (Undefined Mode Codes Invalid) globally defines whether undefined mode code commands are treated as valid (default) or invalid commands. This bit applies only to the following 22 mode code commands that are undefined in MIL-STD-1553B:

Mode Codes 0 through 15 with T/$\overline{R}$ bit = 0
Mode Codes16, 18 and19 withT/$\overline{R}$ bit = 0
Mode Codes 17, 20 and 21 with T/$\overline{R}$ bit = 1

If the UMCINV bit is low (default after $\overline{MR}$ reset) undefined mode code commands are considered valid and RT response is based on individual mode command settings in the Illegalization Table: If the command's table bit equals 0, the mode command is legal; the RT responds "in form" and updates status. If the command's table bit equals 1 the mode command is illegal, the RT asserts Message Error status and (if non-broadcast) transmits only its Status Word without associated data word. Table 17 describes explicit terminal response for each mode code value and command T/$\overline{R}$ bit state, based on various option settings.

If UMCINV is asserted, the 22 undefined mode code commands are treated as invalid: There is no terminal recognition of the command. No command response occurs and status remains unchanged for the benefit of following "transmit status" or "transmit last command" mode commands.

If UMCINV is low, the device determines legal vs. illegal status of commands from the Illegalization Table. If the terminal does not use illegal command detection, the Illegalization Table should be left in its post-reset default state, all values equal logic 0. In this case, the terminal provides "in form" response to all valid commands. The terminal responds with clear status and a transmitted mode data word for mode commands 16-31 with T/$\overline{R}$ bit equals 1. Assigned data buffer locations can be initialized to provide predictable "in form" responses for all transmit mode codes 16-31. (If UMCINV is asserted, the terminal will not respond or update status for received mode codes 17, 20 and 21 with T/$\overline{R}$ = 1.)

To use illegal command detection, the host modifies the Illegalization Table to make illegal any combination subaddress and mode code commands. This may include undefined mode codes, reserved mode codes, and/or mode codes not implemented in the application.

Note: Mode command MC0 "dynamic bus control" cannot be implemented in the device since the HI-6130/21 cannot act as a Bus Controller. Therefore, the "dynamic bus control acceptance" status bit cannot be set in the outgoing status word from this device.

21.2. Mode Command Interrupts

For mode commands, interrupt generation is programmed by the top three bits in the descriptor table Control Word. Notice that broadcast-transmit interrupts can be enabled for mode code values in the range of 0 - 15, but broadcast-transmit mode codes 16 - 31 are not allowed. When a mode command is received and the IWA interrupt bit is asserted in its descriptor Control Word, that command will generate a host interrupt if the IWA bit is high in the Interrupt Enable Register. The IWA bit is asserted in the Pending Interrupt Register and the $\overline{INTMES}$ interrupt output is asserted.

Before $\overline{INTMES}$ interrupt assertion, the device updates the Interrupt Log buffer, writing a new IIW Interrupt Information Word and a new IAW Interrupt Address Word. The IWA (interrupt when accessed) bit is asserted in the new IIW to indicate interrupt type. The IAW contains the Descriptor Table address for the mode command's Control Word, based on mode code value and command word T/$\overline{R}$ bit state. The host reads the IAW to determine the command that caused the interrupt.

21.3. Mode Command Data Words

Mode commands having mode code values from 0 through 15 (decimal) do not have an associated data word. These are received as Command Word only, never having a contiguous data word. The terminal response to valid mode commands 0-15 always consists of Status Word only, assuming command was not broadcast.

Mode commands having mode code values from 16 through 31 (decimal) always have an associated data word. When the command word T/$\overline{R}$ bit equals 0, the terminal receives a data word, contiguously following the Command Word. When valid legal mode commands 16-31 arrive with T/$\overline{R}$ bit equal to 1, the terminal responds by transmitting its status word with a single data word.

When the SMCP option bit in Configuration register 1 is zero, individual data words for mode codes 16-31

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decimal are stored in an indexed or ping-pong buffer assigned by the mode command's Descriptor Table entry. Circular buffer methods are not available for mode code commands.

When the SMCP option bit in Configuration register 1 is asserted, individual data words for mode codes 16-31 decimal are stored within the Descriptor Table itself. This is explained next.

Table 17. Mode Code Command Summary

Command T/$\overline{R}$ bit	Mode Code		MIL-STD-1553 Defined Function	Associated Data Word	Broadcast Allowed	See Note
	Binary	Dec.				
0	00000 to 01111	0 to 15	Undefined mode commands 0 - 15 when T/$\overline{R}$ bit = 0	No	No	(1)
1	00000	0	Dynamic Bus Control	No	No	(3)
1	00001	1	Synchronize (without data)	No	Yes	
1	00010	2	Transmit Status Word	No	No	
1	00011	3	Initiate Self-Test	No	Yes	
1	00100	4	Transmitter Shutdown	No	Yes	
1	00101	5	Override Transmitter Shutdown	No	Yes	
1	00110	6	Inhibit Terminal Flag	No	Yes	
1	00111	7	Override Inhibit Terminal Flag	No	Yes	
1	01000	8	Reset Remote Terminal	No	Yes	
1	01001 to 01111	9 to 15	Reserved Mode Commands 9 - 15 with T/$\overline{R}$ bit = 1	No	Yes	(2)
0	10000	16	Undefined Mode Command	Yes	No	(1)
1	10000	16	Transmit Vector Word	Yes	No	
0	10001	17	Synchronize With Data	Yes	Yes	
1	10001	17	Undefined Mode Command	Yes	No	(1)
0	10010	18	Undefined Mode Command	Yes	No	(1)
1	10010	18	Transmit Last Command	Yes	No	
0	10011	19	Undefined Mode Command	Yes	No	(1)
1	10011	19	Transmit Built-In Test Word	Yes	No	
0	10100	20	Selected Transmitter Shutdown	Yes	Yes	
1	10100	20	Undefined Mode Command	Yes	No	(1)
0	10101	21	Override Selected Transmitter Shutdown	Yes	Yes	
1	10101	21	Undefined Mode Command	Yes	No	(1)

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Command T/$\overline{R}$ bit	Mode Code		MIL-STD-1553 Defined Function	Associated Data Word	Broadcast Allowed	See Note
	Binary	Dec.				
0	01001 to 01111	22 to 31	Reserved Mode Commands 22 - 31 with T/$\overline{R}$ bit = 0	Yes	Yes	(2)
1	01001 to 01111	22 to 31	Reserved Mode Commands 22 - 31 with T/$\overline{R}$ bit = 1	Yes	No	(2)

NOTES:

1. The 22 undefined mode commands can be rendered invalid by setting the UMCINV (undefined mode codes invalid) option bit in Configuration Register1. If UMCINV is asserted, there is no recognition of the undefined command by the terminal. If UMCINV is zero, the commands are considered valid. Terminal response when UMCINV equals 0 is wholly determined by the Illegalization Table:
   a. If a command's bit in the Illegalization Table equals zero, the terminal responds "in form" with Clear Status. Mode commands 17, 20 and 21 are undefined when T/$\overline{R}$ bit equals one, but will transmit a contiguous data word. Mode commands 16, 18 or 19 are undefined when T/$\overline{R}$ bit equals 0, but will receive a contiguous data word.
   b. If a command's bit in the Illegalization Table equals one, the command is considered illegal. The Message Error (ME) status bit is asserted and the terminal transmits status without data word. Illegal mode commands 16-31 will not transmit or receive a mode data word.
2. Response to the reserved mode commands is fully defined by Illegalization Table settings. As described in (a) and (b) above, the terminal illegalizes any reserved mode command having Illegalization Table bit equal to 1, and responds "in form" when the Table bit equals zero. The "in form" response for reserved mode commands 16 through 31 transacts a received or transmitted data word.
3. HI-6130/21 cannot fulfill Bus Control duties.

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21.4. Standard Mode Command Processing

Data buffer options for mode commands differ from buffer options for subaddress commands. Mode commands can use ping-pong buffering or indexed buffering. When mode commands use indexed buffers, “single message mode” (INDX = 0) is recommended. When using indexed or ping-pong buffers for mode commands:

- For mode commands without associated data word (mode codes 0-15 decimal), only the Message Information and Time-Tag words are updated in the mode command’s assigned data buffer in RAM.
- For mode commands 16-31 (decimal) that receive a data word, indexed and ping-pong buffer methods copy the received mode data word to the mode command’s assigned data buffer in shared RAM, after the message is transacted. The Message Information and Time-Tag words are also updated.
- For most mode commands 16-31 (decimal) that transmit a data word, the device reads the data word for transmit from the buffer location assigned in the Descriptor Table. Exceptions occur for MC18 “transmit last command” and for MC19 “transmit BIT word.” The MC18 data word is automatically provided by the device, based on recent command transactions. The MC19 data word comes from register 0x14 or 0x15, depending on the state of the ALTBITW option in Configuration Register 2. For both MC18 and MC19, the transmitted data word is automatically recorded in the mode command’s assigned data buffer in RAM, after message completion. The Message Information and Time-Tag words are also updated.

21.5. Simplified Mode Command Processing

Mode commands have a buffer alternative that is unavailable for subaddress commands. The SMCP bit in Configuration Register 1 selects Simplified Mode Command Processing, a global option applying to all mode commands. When the SMCP bit is high, mode command descriptor blocks (in the Descriptor Table) do not contain data pointers to reserved buffers elsewhere in the shared RAM. Instead, each 4-word descriptor block itself contains the message information word, the time-tag word and the data from the most recent occurrence of each mode command:

Descriptor Word 1	Mode Command Control Word
Descriptor Word 2	Message Information Word
Descriptor Word 3	Time-Tag Word
Descriptor Word 4	Mode Data Word

Descriptor Word 1 contains the receive or transmit mode command Control Word. When SMCP is used, just two Control Word bits are used: DBAC (descriptor block accessed) and BCAST (broadcast).

When SMCP is enabled, the host need not initialize the mode code command segments in the Descriptor Table. When Simplified Mode Command Processing is selected, the host does not write Descriptor Words 2-3 in the Descriptor Table entries for mode commands. For mode code values 0 to 15 decimal, the Descriptor Word 4 serves no function because these mode codes do not have an associated data word. For transmit mode code values 16 to 31, the host may initialize Descriptor Word 4. The default transmit value is 0x0000. Mode command MC16 “transmit vector word” is one of the three defined mode commands that transmit a data word: MC16, MC18 and MC19. Its Descriptor Word 4 should be initialized if a value other than 0x0000 is needed. MC18 and MC19 are discussed below.

- For mode commands without associated data word (mode codes 0-15 decimal), Simplified Mode Command Processing updates the Message Information and Time-Tag words in Descriptor Words 2 and 3, and Descriptor Word 1 (bits 9,11). For these commands, SMCP does not update Descriptor Word 4, which may be non-zero if written earlier by the host.
- For receive mode commands 16-31 (decimal) that receive a data word, Simplified Mode Command Processing copies the received mode data word to Descriptor Word 4. The Message Information and Time-Tag words in Descriptor Words 2 and 3, and Descriptor Word 1 (bits 9, 11) are also updated.
- For most transmit mode codes 16-31 (decimal), the device reads the data word for transmission from each command’s Descriptor Word 4. Exceptions occur for MC18 “transmit last command” and for MC19 “transmit built-in test word”. The MC18 data word is automatically provided, based on the last command transacted. The MC19 data word comes from register 0x14 or 0x15, depending on the state of the ALTBITW option in Configuration Register 2. For MC18 and MC19, the transmitted data value is automatically copied to the mode command’s Descriptor Word 4 after message completion. The Message Information and Time-Tag words in

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Descriptor Words 2 and 3, and Descriptor Word 1 (bits 9, 11) are also updated.

The Appendix shows terminal response to all possible subaddress and mode code command combinations. The table summarizes terminal response for the full range of message conditions, including errors, incomplete messages, etc. The table explicitly describes terminal response and impact on terminal Status Word, Descriptor Control Words and data buffer Message Information Words. The table includes effects for all pertinent setup options and identifies all interrupt options available. Bold text blocks indicate error-free messages or “in form” Clear Status responses when the terminal is not using “illegal command detection”.

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22. SERIAL EEPROM PROGRAMMING UTILITY

The HI-6130 or HI-6131 can program a serial EEPROM via the dedicated EEPROM SPI port for subsequent auto-initialization events. The device copies host-configured registers and RAM (configuration tables and possibly data buffers) to serial EEPROM.

Compatible SPI serial EEPROMs are 3.3V, operate in SPI modes 1 or 3 and have 128-byte pages. The serial SPI data is clocked at 8.3 MHz SCK frequency. A 2K x 8 EEPROM can restore the lower 1K x 16 device address space. A 64K x 8 EEPROM retains the entire 32K x 16 register/RAM address space.

22.1. Auto-Initialization

A deliberate series of events initiates copy of data from HI-6130 or HI-6131 registers and RAM to serial EEPROM. This reduces the likelihood of accidental EEPROM overwrites. The following series of events must occur to initiate programming:

1. Using a fresh host initialization immediately following $\overline{MR}$ master reset as the basis for EEPROM copy

Until EEPROM reprogramming is complete, disconnect the terminal from MIL-STD-1553 buses, or take other measures to prevent bus activity detection by the device. With the AUTOEN, TXINHA and TXINHB pins in logic 0 state, apply $\overline{MR}$ master reset and wait for READY output assertion. Verify that the $\overline{IRQ}$ interrupt output does not pulse low at READY assertion, indicating likely RT address parity error at the RTA4:0 and RTAP pins. Using known good parameters, the host initializes device registers, the RAM descriptor table and transmit data buffers (if necessary).

- If auto-initialization will be used to configure the Bus Controller, the BCENA input pin should be logic 1. The corresponding BCENA bit 12 in Master Configuration Register 0x0000 should be logic 1, but BCSTRT register bit 13 must remain in the post-reset logic 0 state.
- If auto-initialization will be used to configure the Bus Monitor, the MTENA input pin should be logic 1. The corresponding MTENA bit 8 in Master Configuration Register 0x0000 should be logic 0. Until EEPROM programming is complete, the terminal should be disconnected from MIL-STD-1553 buses (or other measures taken) to prevent bus activity detection by the monitor.
- If auto-initialization will be used to configure Remote Terminals RT1 and/or RT2, the RT1ENA and/or RT2ENA input pins should be logic 1. The corresponding RT1ENA and/or RT2ENA bits 6 and 7 in Master Configuration Register 0x0000 should be logic 1, but RT1STEX and RT2STEX register bits 4 and 5 must remain in the post-reset logic 0 state.

Skip to step 3.

2. Using the existing EEPROM configuration as the baseline for a new EEPROM configuration

Until EEPROM reprogramming is complete, disconnect the terminal from MIL-STD-1553 buses, or take other measures to prevent bus activity detection by the device. If the application includes the Bus Controller, the BCENA input pin should be at logic 0. With the AUTOEN pin in logic 1 state and the TXINHA and TXINHB pins in logic 0 state, apply and release $\overline{MR}$ master reset and wait for READY output assertion. Verify that the nIRQ output does not pulse low (or go and remain low) at READY assertion. Confirm that the EECKE and RAMIF bits are logic 0 in the Operational Status Register 0x0002. If register bits 4 or 5 (RT1STEX, RT2STEX) in Master Configuration Register 0x0000 were set by auto-initialization, reset them now. Modify register and RAM values to reflect the new changes.

3. If the application includes the Bus Controller, the BCENA input pin should be set to logic 1 now. Do not assert BCSTRT bit 13 in Master Configuration Register 0x0000.

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EEPROM programming is locked out at step 4 for the following conditions:

- ACTIVE output pin assertion occurs after $\overline{MR}$ master reset.
- RT1STEX bit 4, RT2STEX bit 5 or MTENA bit 8 is set in Master Configuration Reg 0x0000.

4. The host writes a 2-part “unlock code” to RAM address 0x004E. The unlock code value selectively enables any combination of terminal devices (BC, MT, RT1, RT2) to automatically start execution, after subsequent auto-initialization sequences are performed. Programmed here, the same combination of terminal devices is simultaneously enabled after every initialization. Unlock words are encoded as shown in Table 18.

Table 18. Terminal Unlock Word Encoding

Word 1	Word 2	Initialize RT1 [2]	Initialize RT2 [3]	Initialize MT [4]	Initialize BC [5]
0xA00A	0x5FF5	No auto init. [1]	No auto init.	No auto init.	No auto init.
0xA03A	0x5FC5	X			
0xA0CA	0x5F35		X		
0xA0FA	0x5F05	X	X		
0xA30A	0x5CF5			X	
0xA33A	0x5CC5	X		X	
0xA3CA	0x5C35		X	X	
0xA3FA	0x5C05	X	X	X	
0xAC0A	0x53F5				X
0xAC3A	0x53C5	X			X
0xACCA	0x5335		X		X
0xACFA	0x5305	X	X		X
0xAF0A	0x50F5			X	X
0xAF3A	0x50C5	X		X	X
0xAFCA	0x5035		X	X	X
0xAFFA	0x5005	X	X	X	X

Note 1: Default. No terminal devices (BC, MT, RT1, RT2) are started. The host must write Master Configuration Register 0x0000 to start terminals.

Note 2: The RT1ENA register bit 6 in register 0x0000 must be set before step 4. During auto-initialization events, the RT1ENA and AUTOEN input pins must be logic 1 before rising edge of $\overline{MR}$ master reset. After auto-initialization, RT1STEX bit 4 is automatically set in Master Configuration. Register 0x0000, starting Remote Terminal RT1 execution.

Note 3: The RT2ENA register bit 7 in register 0x0000 must be set before step 4. During auto-initialization events, the RT2ENA and AUTOEN input pins must be logic 1 before rising edge of $\overline{MR}$ master reset. After auto-initialization, RT2STEX bit 5 is automatically set in Master Configuration Register 0x0000, starting Remote Terminal RT2 execution.

Note 4: The MTENA register bit 8 in register 0x0000 must be set before step 4. During auto-initialization events, the MTENA and AUTOEN input pins must be logic 1 before rising edge of $\overline{MR}$ master reset. After auto-initialization, the SMT or IMT MTENA bit is automatically set in Master Configuration Register 0x0000, starting Bus Monitor execution.

Note 5: The BCENA register bit 12 in register 0x0000 must be set before step 4. During auto-initialization events, the BCENA and AUTOEN input pins must be logic 1 before rising edge of $\overline{MR}$ master reset. After auto-initialization, BCSTRT bit 13 is automatically pulsed in Master Configuration Register 0x0000, starting Bus Controller execution.

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The four terminals can be automatically started (or not started) in any combination. For example, exclusive-ORing both default unlock Words 1 and 2 with 0x0FF0 results in unlock Word 1 = 0xAFFA and Word 2 = 0x5005. This combination automatically and simultaneously enables execution for all four terminal devices: BC, MT, RT1 and RT2, at every subsequent auto-initialization from EEPROM. Individual soft resets for a single terminal device will automatically enable that device, if enabled here.

5. The EECOPY input pin is driven high for at least 1 ms, then driven low. In response, the READY output goes low while EEPROM memory is written. The unlock code at address 0x004E is cleared. Device register and RAM contents are written to the serial EEPROM, one byte at a time.

   During programming, terminal checksums are tallied for the RT1, RT2 and SMT/IMT terminal devices, if used. An overall 32K checksum is also tallied. These checksums, stored in the EEPROM, are used for error detection later, during auto-initialization and soft reset events. There is no Bus Controller soft reset.

Checksum Type	EEPROM location corresponds to RAM Address
Overall Checksum	0x004E
RT1 Checksum	0x01C0
RT2 Checksum	0x01E0
SMT or IMT Checksum	0x005C

   On the following pages, see the list of registers included in the stored overall and terminal checksums. When the READY output goes high, EEPROM copy is complete.

6. For terminal devices selected for auto-enable by step 4 unlock word selection, the RT1STEX, RT2STEX, MTENA and/or BCSTRT bits are set in the 2-byte EEPROM image corresponding to Master Configuration Register 0x0000. During subsequent auto-initialization events, these are the last bits written, just before READY assertion. Terminal devices having enable bits set to logic 1 in the EEPROM image are automatically and simultaneously enabled just before READY assertion. Terminal devices not automatically enabled (by step 4 unlock word selection) have logic 0 enable bits RT1STEX, RT2STEX, MTENA and/or BCSTRT in the 2-byte EEPROM image corresponding to Master Configuration Register 0x0000. After auto-initialization, these terminal devices remain in standby until enabled by host write to the Master Configuration Register 0x0000.

22.2. Overall 32K Checksum Used by Auto-Initialization

When auto-initialization is performed, the overall checksum (stored in EEPROM by the EECOPY process) is used for error checking. EECOPY stored this checksum value in the two 8-bit locations corresponding to RAM address 0x004E. This checksum covers the entire 32K register and RAM address range from 0 to 0x7FFF, excluding the following register addresses. At auto-initialization, the following registers are not written using EEPROM data:

Table 19. Registers are not written using EEPROM data

Address	Excluded Register Name
0x0002	Master Status & Reset Register
0x0007	BC Pending Interrupt Register
0x0008	MT Pending Interrupt Register
0x0009	RT1 & RT2 Pending Interrupt Register
0x000A	Interrupt Log Address Pointer

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Address	Excluded Register Name
0x000B	RT1 Memory Address Pointer
0x000C	RT2 Memory Address Pointer
0x000D	MT Memory Address Pointer
0x000E	BC Memory Address Pointer
0x0018	RT1 Operational Status Register
0x001E	RT1 Built-In Test Word Register
0x0021	RT2 Operational Status Register
0x0027	RT2 Built-In Test Word Register
0x0030	MT Current Address Pointer
0x0031	MT Last Address Pointer
0x0035	BC Frame Time Remaining Register
0x0036	BC Message Time Remaining Register
0x0037	BC Condition Code Register
0x003A	MT Time Tag Counter Low
0x003B	MT Time Tag Counter Mid
0x003C	MT Time Tag Counter High
0x0043	BC Time Tag Counter Low
0x0044	BC Time Tag Counter High
0x0049	RT1 Time Tag Counter
0x004B	RT2 Time Tag Counter

The overall checksum includes individual terminal checksums for RT1, RT2 and Bus Monitor, which the EECOPY process stored at EEPROM locations corresponding to RAM addresses 0x01C0, 0x01E0 and 0x005C respectively. All checksums stored by the EECOPY process use two's complement format. Each checksum is calculated by summing the individual 16-bit data values (ignoring carry) over the full set of included register and RAM addresses. The summation is then complemented, then incremented (ignoring carry) to yield the stored two's complement checksum value.

When the device performs checksum-based error checking, a new summation is tallied (ignoring carry) for the individual 16-bit data values over the range of included register and RAM addresses. When this summation is added to the previously stored two's complement checksum, the result is zero when the new data summation is the same as that tallied by EECOPY when the checksum was stored.

The registers tallied in each of the RT1, RT2 and SMT or IMT terminal checksums are summarized on the next pages. These individual checksums are used for error checking during soft reset events. Soft reset occurs for RT1, RT2 or SMT / IMT when RT1RESET bit 10, RT2RESET bit 11 and/or MTRESET bit 12 is set in the Master Status and Reset Register 0x0001. One, two or three terminal reset bits can be individually or simultaneously set, without affecting other on-chip terminals or the Bus Controller. The HI-613x Bus Controller does not have soft reset.

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23. SOFTWARE RESET

23.1. Remote Terminal 1 (RT1)

This is initiated when RT1RESET bit 10 is set in the Master Status and Reset Register 0x0001. The following actions are performed.

Table 20. RT1 Soft Reset Summary

Action	Registers Affected
Clears these individual register bits	0x0000 Master Configuration Register, RT1STEX bit 4
	0x0006 Hardware Pending Int Register, RTIP bit 2
	0x0006 Hardware Pending Int Register, RT1APF bit 3
	0x0009 RT1 and RT2 Pending Int Register, RT1 int bits 8 – 3
Clears these entire register addresses	0x0018 RT1 Operational Status Register
	0x001A RT1 MIL-STD-1553 Status Word Bits Register
	0x001E RT1 Built-In Test Word Register
	0x0049 RT1 Time Tag Counter
Loads these registers from EEPROM *These 522 locations comprise the RT1 Terminal Checksum stored at 0x01C0 by EECOPY process*	0x000F Hardware Interrupt Enable Register
	0x0012 RT1 & RT2 Interrupt Enable Register **(see note)**
	0x0013 Hardware Interrupt Output Enable Register
	0x0016 RT1 & RT2 Interrupt Output Enable Register **(see note)**
	0x0017 RT1 Configuration Register
	0x0019 RT1 Descriptor Table Base Address Register
	0x001C RT1 Bus A Select Register
	0x001D RT1 Bus B Select Register
	0x001F RT1 Alternate BIT Word Register
	0x004A RT1 Time Tag Utility Register
	0x0200 through 0x02FF: RT1 Illegalization Table
	0x0400 through 0x05FF: RT1 Descriptor Table

Note: This register reload potentially affects both RTs.

RT1 automatically starts (RT1STEX is set in register 0x0000) after soft reset completion, if these requirements are met:

- The RT1ENA pin is logic 1 during the soft reset event
- The RT1ENA pin and RT1ENA bit 6 were both logic 1 in the Master Configuration Register when EECOPY created the EEPROM image.
- The RT1STEX bit 4 is logic 1 in the EEPROM Master Configuration Register image because the EECOPY unlock codes during programming were Unlock Word 1 = 1010-XXXX-XX11-1010 and Unlock Word 2 = 0101-XXXX-XX00-0101 where X denotes “don’t care”.

To manually start RT1 after soft reset completion (indicated by READY signal assertion), the host must set RT1STEX bit 4 in register 0x0000, if RT1 auto-start was disabled or otherwise failed for one or more of these reasons:

- The RT1ENA pin was logic 0 during the soft reset event.
- The RT1ENA pin was logic 0 and/or RT1ENA bit 6 was logic 0 in the Master Configuration Register when

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EECOPY created the EEPROM image. A new EEPROM image is needed to allow auto-start after RT1 soft reset.

- The RT1STEX bit 4 is logic 0 in the EEPROM Master Configuration Register image because the unlock codes used by EECOPY were wrong. A new EEPROM image is needed to allow auto-start after RT1 soft reset.

23.2. Remote Terminal 2 (RT2)

This is initiated when RT2RESET bit 11 is set in the Master Status and Reset Register 0x0001. The following actions are performed.

Table 21. RT2 Soft Reset Summary

Action	Registers Affected
Clears these individual register bits	0x0000 Master Configuration Register, RT2STEX bit 3
	0x0006 Hardware Pending Int Register, RTIP bit 2
	0x0006 Hardware Pending Int Register, RT2APF bit 4
	0x0009 RT1 and RT2 Pending Int Register, RT2 int bits 15 – 10
Clears these entire register addresses	0x0021 RT2 Operational Status Register
	0x0023 RT2 MIL-STD-1553 Status Word Bits Register
	0x0027 RT2 Built-In Test Word Register
	0x004B RT2 Time Tag Counter
Loads these registers from EEPROM *These 522 locations comprise the RT2 Terminal Checksum stored at 0x01E0 by EECOPY process*	0x000F Hardware Interrupt Enable Register
	0x0012 RT1 & RT2 Interrupt Enable Register **(see note)**
	0x0013 Hardware Interrupt Output Enable Register
	0x0016 RT1 & RT2 Interrupt Output Enable Register **(see note)**
	0x0020 RT2 Configuration Register
	0x0022 RT2 Descriptor Table Base Address Register
	0x0025 RT2 Bus A Select Register
	0x0026 RT2 Bus B Select Register
	0x0028 RT2 Alternate BIT Word Register
	0x004C RT2 Time Tag Utility Register
	0x0300 through 0x03FF: RT2 Illegalization Table
	0x0600 through 0x07FF: RT2 Descriptor Table

Note: This register reload potentially affects both RTs.

RT2 automatically starts (RT2STEX is set in register 0x0000) after soft reset completion, if these requirements are met:

- The RT2ENA pin is logic 1 during the soft reset event
- The RT2ENA pin and RT2ENA bit 7 were both logic 1 in the Master Configuration Register when EECOPY created the EEPROM image.
- The RT2STEX bit 5 is logic 1 in the EEPROM Master Configuration Register image because the EECOPY unlock codes during programming were Unlock Word 1 = 1010-XXXX-11XX-1010 and Unlock Word 2 = 0101-XXXX-00XX-0101 where X denotes “don’t care”.

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To manually start RT2 after soft reset completion (indicated by READY signal assertion), the host must set RT2STEX bit 5 in register 0x0000, if RT1 auto-start was disabled or otherwise failed for one or more of these reasons:

- The RT2ENA pin was logic 0 during the soft reset event
- The RT2ENA pin was logic 0 and/or RT2ENA bit 7 was logic 0 in the Master Configuration Register when EECOPY created the EEPROM image. A new EEPROM image is needed to allow auto-start after RT2 soft reset.
- The RT2STEX bit 5 is logic 0 in the EEPROM Master Configuration Register image because the unlock codes used by EECOPY were wrong. A new EEPROM image is needed to allow auto-start after RT2 soft reset.

23.3. Bus Monitor SMT / IMT

This is initiated when MTRESET bit 12 is set in the Master Status and Reset Register 0x0001. The following actions are performed.

Table 22. SMT / IMT Soft Reset Summary

Action	Registers Affected
Clears these individual register bits	0x0000 Master Configuration Register, MTENA bit 8
	0x0006 Hardware Pending Int Register, MTIP bit 1
Clears these entire register addresses	0x0008 MT Pending Interrupt Register
	0x0030 MT Next Message Stack Address Pointer
	0x0031 MT Last Message Stack Address Pointer
	0x003A MT Time Tag Counter, Low
	0x003B MT Time Tag Counter, Mid
	0x003C MT Time Tag Counter, High
Loads these registers from EEPROM *These 561 locations comprise the MT Terminal Checksum stored at 0x005C by EECOPY process*	0x000F Hardware Interrupt Enable Register
	0x0011 MT Interrupt Enable Register
	0x0013 Hardware Interrupt Output Enable Register
	0x0015 MT Interrupt Output Enable Register
	0x0029 MT Configuration Register
	0x002A IMT Packet Maximum Message Count Register
	0x002B IMT Packet Maximum MIL-STD-1553 Word Count Register
	0x002C IMT Packet Maximum Time Register
	0x002D IMT Packet Maximum Gap Time Register
	0x002E IMT Packet Channel ID Register
	0x002F MT Stack Address Table Start Address Register
	0x003D MT Time Tag Utility Register, Low
	0x003E MT Time Tag Utility Register, Mid
	0x003F MT Time Tag Utility Register, High
	0x0040 MT Time Tag Match Register, Low
	0x0041 MT Time Tag Match Register, Mid
	0x0042 MT Time Tag Match Register, High
	0x00B0 through 0x00BF: MT Stack Address Table(s)
	0x0100 through 0x017F: MT Message Filter Table

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Note: Soft reset for the Bus Monitor re-initializes the stack address pointers, but does not clear the allocated buffer space in the stack(s).

The Bus Monitor automatically starts (MTENA is set in register 0x0000) after soft reset completion, if the following requirements are met. Message recording commences when a new valid command is received:

- The MTENA pin is logic 1 during the soft reset event
- The MTENA pin was logic 1 in the Master Configuration Register when EECOPY created the EEPROM image.
- The MTENA bit 12 is logic 1 in the EEPROM Master Configuration Register image because EECOPY used these unlock codes during EEPROM programming: Unlock Word 1 = 1010-XX11-XXXX-1010 and Unlock Word 2 = 0101-XX00-XXXX-0101 where X denotes “don’t care”.

To manually start the Bus Monitor after soft reset completion (indicated by READY signal assertion), the host must set MTENA bit 12 in register 0x0000, if auto-start was disabled or otherwise failed for one or more of these reasons:

- The MTENA pin was logic 0 during the soft reset event
- The MTENA pin was logic 0 in the Master Configuration Register when EECOPY created the EEPROM image. A new EEPROM image is needed to allow auto-start after MT soft reset.
- The MTENA bit 12 is logic 0 in the EEPROM Master Configuration Register image because the unlock codes used by EECOPY were wrong. A new EEPROM image is needed to allow auto-start after Bus Monitor soft reset.

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24. HOST INTERFACE

24.1. HI-6130 Host Bus Interface

The HI-6130 uses a parallel bus interface for communications with the host. Host interface to registers and RAM is enabled through the Chip Enable ($\overline{CE}$) pin, and accessed via 16-bit data bus and several host-originated control signals described below. Timing is identical for register operations and RAM operations via the host bus interface, but read and write operations have different signal timing. The HI-6130 parallel host bus interface is capable of faster communication than the HI-6131 Serial Peripheral Interface.

Depending on the chosen microprocessor family, the processor's hardware bus interface may be described as an "external bus interface," "memory interface" or may have a different name. The user can also implement a software controlled "bit-banged" interface to the HI-6130, at the cost of substantially slower RAM and register read/write times.

The bus interface is compatible with the two prevalent bus control signal methods: "Intel style" interface, characterized by separate strobes for read and write operations ($\overline{OE}$ and $\overline{WE}$), and "Motorola style" interface, characterized by a single read/write strobe ($\overline{STR}$) and a data direction signal (R/$\overline{W}$). Bus control style is selected using the BTYPE configuration pin, which sets the function of two other input pins to serve as either $\overline{OE}$ and $\overline{WE}$, or $\overline{STR}$ and R/$\overline{W}$.

The BWID configuration pin selects either 8- or 16-bit bus widths. When the BWID pin is connected to ground, 8-bit mode is selected; two bytes are sequentially transferred for each 16-bit word operation. In 8-bit mode only, the BENDI configuration pin selects bus "endianness." This is the system attribute that indicates whether integers are represented with the most significant byte stored at the lowest address (big endian) or at the highest address (little endian). Internal device storage is "big endian". For processor compatibility, the BENDI pin sets the order for byte accesses when the host bus is configured for 8-bit width, that is, when BWID equals 0. When BENDI is low, "little endian" is chosen; the low order byte (bits 7:0) is transacted before the high order byte (bits 15:8). When BENDI is high, "big endian" is chosen and the high order byte is transacted on the host bus before the low order byte. In 8-bit mode, all transacted data uses bus data bits 7:0 and bus data bits 15:8 are not used. Further, bus address bit A0 ($\overline{LB}$) always equals 0 during the first byte read/write access, and equals 1 during the second byte access

When the BWID pin is connected high or left unconnected, 16-bit bus width is used. For 16-bit bus operation, the A0 ($\overline{LB}$) address pin is not used and the BENDI input pin is "don't care."

24.1.1. Bus Wait States and Data Prefetch

The HI-6130 has a WAIT output pin that tells the host to add wait states when additional access time is needed during bus read cycles. For compatibility with different host processors, the state of the WPOL input pin sets the WAIT output as active high or active low. The WAIT output can be ignored when the host processor read cycle time is always slow enough to work with the HI-6130 bus. When using fast host processors, cycle time is sometimes slowed down by configuring the processor to add one or more wait states during every read or write cycle, but slow-down affects all cycles, even when unnecessary.

Data prefetch is a technique used by the HI-6130 to speed up host multi-word read access to registers or RAM by eliminating wait states. Prefetching occurs when HI-6130 logic requests data before it is actually needed. Because register or RAM locations are often read sequentially, performance improves when data is prefetched in address sequence order. For every host read cycle, the device first reads the addressed location, then prefetches the following address, to speed up access in the likely event that the following word will be read next.

For the HI-6130, WAIT is always asserted for the first word fetched in any read sequence. The first read cycle has a long access time because there is no prefetch. This may be the first byte read in 8-bit mode, or the first word read in 16-bit mode. After each word (or byte) is fetched for a read operation, the next word (or byte) is prefetched to speed-up the read cycle time when sequential address read sequences occur. After the first word read, the following words read in sequence are accessed without WAIT, resulting in faster overall multi-word read timing. As long as bytes or words are read in address order, additional wait states are unnecessary.

Data prefetch during read cycles is blocked when the next RAM address is a Control Word in the Descriptor Table. The table base address (set by the value in register 0x0005) and every fourth word thereafter is a Control Word. This consists of table addresses having these address offsets from the table start address of 0, 4, 8, 0xC… 0x1F8 and 0x1FC. If allowed, prefetch (like any other read) would reset the Control Word DBAC status bit, so prefetch is disallowed in this range. Thus for HI-6130, **multi-word sequential read sequences will assert WAIT every fourth word when reading RAM**

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within the 512-word Descriptor Table address range.

For fastest read access under all conditions, the user can set host processor bus timing (by adjusting processor wait states for the chip select assigned to the HI-6130) to match the faster read cycle time for prefetched data, while the HI-6130 WAIT output adds one or more additional wait states for the slower initial read cycle.

Timing diagrams for bus read and write operations are shown in the **Section Electrical Characteristics**. Separate diagrams show “Intel style” and “Motorola style” control interfaces.

24.2. HI-6131 Serial Peripheral Interface

In the HI-6131, internal RAM and registers occupy a 32K x 16 address space. The lowest 80 addresses access registers and the remaining addresses access RAM locations. Timing is identical for register operations and RAM operations via the serial interface, and read and write operations have likewise identical timing.

24.2.1. Serial Peripheral Interface (SPI) Basics

The HI-6131 uses an SPI synchronous serial interface for host access to registers and RAM. Host serial communication is enabled through the Chip Enable (CE) pin, and is accessed via a three-wire interface consisting of Serial Data Input (SI) from the host, Serial Data Output (SO) to the host and Serial Clock (SCK). All programming cycles are completely self-timed, and no erase cycle is required before write.

The SPI (Serial Peripheral Interface) protocol specifies master and slave operation; the HI-6131 operates as an SPI slave.

The SPI protocol defines two parameters, CPOL (clock polarity) and CPHA (clock phase). The possible CPOL-CPHA combinations define four possible “SPI Modes.” Without describing details of the SPI modes, the HI-6131 operates in the two modes where input data for each device (master and slave) is clocked on the rising edge of SCK, and output data for each device changes on the falling edge. These are known as SPI Mode 0 (CPHA = 0, CPOL = 0) and SPI Mode 3 (CPHA = 1, CPOL = 1). Be sure to set the host SPI logic for one of these modes.

The difference between SPI Modes 0 and 3 is the idle state for the SCK signal, which is logic 0 for Mode 0 state and logic 1 for Mode 3 state (see Figure 26). There is no configuration setting in the HI-6131 to select SPI Mode 0 or Mode 3 because compatibility is automatic. Beyond this point, the HI-6131 data sheet only shows the SPI Mode 0 SCK signal in timing diagrams.

The SPI protocol transfers serial data as 8-bit bytes. Once CE chip enable is asserted, the next 8 rising edges on SCK latch input data into the master and slave devices, starting with each byte’s most-significant bit. The HI-6131 SPI can be clocked at 16 MHz.

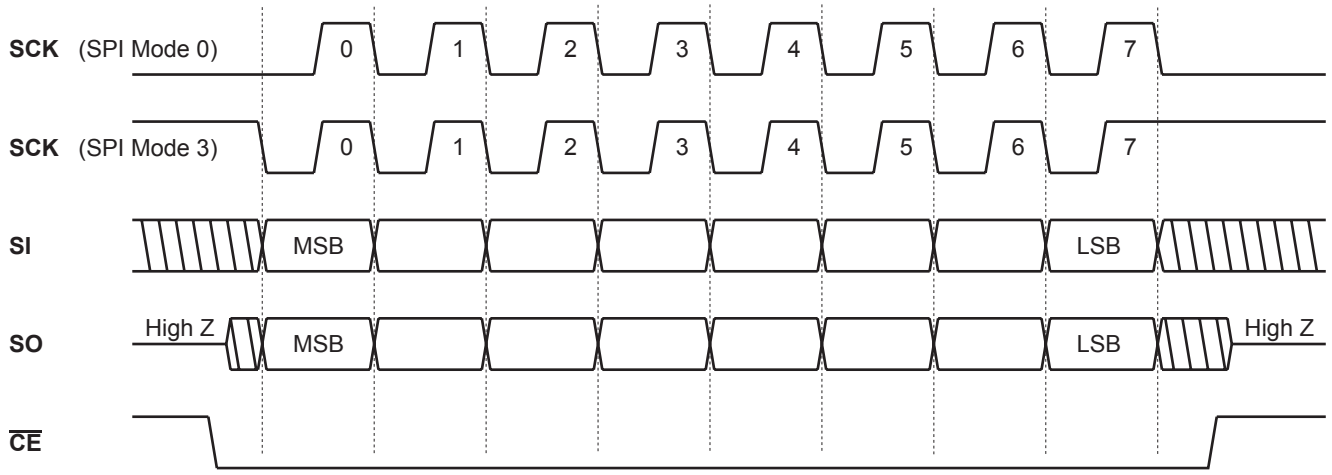

Figure 26. Generalized Single-Byte Transfer Using SPI Protocol. SCK is Shown for SPI Modes 0 and 3

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Multiple bytes may be transferred when the host holds CE low after the first byte transferred, and continues to clock SCK in multiples of 8 clocks. A rising edge on CE chip enable terminates the serial transfer and reinitializes the HI-6131 SPI for the next transfer. If CE goes high before a full byte is clocked by SCK, the incomplete byte clocked into the device SI pin is discarded.

Two byte transfers are needed for SPI exchange of 16-bit register values or RAM data. “Big endian” byte order is used for SPI data transfers. The high order byte (bits 15:8) is transferred before the low order byte (bits 7:0).

In the general case, both master and slave simultaneously send and receive serial data (full duplex) per Figure 26. However the HI-6131 operates half duplex, maintaining high impedance on the SO output, except when actually transmitting serial data. When the HI-6131 is sending data on SO during read operations, activity on its SI input is ignored. Figure 27 and Figure 28 show actual behavior for the HI-6131 SO output.

24.2.2. HI-6131 SPI Commands

For the HI-6131, each SPI read or write operation begins with an 8-bit command byte transferred from the host to the device after assertion of CE. Since HI-6131 command byte reception is half-duplex, the host discards the dummy byte it receives while serially transmitting the command byte.

The HI-6131 SPI command set uses the most significant command bit to specify whether the command is Read or Write. The command byte MSB is zero for read commands, and one for write commands.

24.2.3. Fast-Access Commands for Registers 0-15

The SPI command set includes directly-addressed read commands for registers 0 through 15. The 8-bit pattern for these read commands has the general form

0-0-R-R-R-R-0-0

where RRRR is the 4-bit register address. These fast-access read commands appear in Table 23.

24.2.4. Fast-Access Write Commands for Registers 0-63

The SPI command set includes directly-addressed write commands for registers 0 through 63. The 8-bit pattern for these read commands has the general form

1-0-R-R-R-R-R-R

where RRRRRR is the 6-bit register address. The fast-access write commands appear in Table 23.

Figure 27 and Figure 28 show read and write timing as it appears for fast-access register operations. The command byte is immediately followed by two data bytes comprising the 16-bit data word read or written. For a register read or write, $\overline{CE}$ is negated after the 2-byte data word is transferred.

24.2.5. Indirect Addressing of RAM and Registers

Refer to the HI-6131 SPI command set shown in Table 24. All SPI commands other than fast-access use a Memory Address Pointer register to indicate the starting address for read or write transactions. Four “Memory Address Pointers” reside at register addresses 0x000B through 0x000E. Just one Memory Address Pointer (MAP) is active (enabled) at any time.

The active Memory Address Pointer is selected by writing the MAPSEL bits 11-10 in the Master Configuration Register. Or use the SPI instruction op codes 0xD8, 0xD9, 0xDA or 0xDB which enable MAP registers 0x000B, 0x000C, 0x000D or 0x000E respectively, by automatically writing MAPSEL bits 11-10 in the Master Configuration Register.

The active Memory Address Pointer must be initialized before any read or write operation, other than fast-access.

To write the active MAP register, use a fast-access write op code, followed by the desired 16-bit memory address:

- Writing MAP register 0x000B uses SPI op code 0x8B followed by 16-bit address.
- Writing MAP register 0x000C uses SPI op code 0x8C followed by 16-bit address
- Writing MAP register 0x000D uses SPI op code 0x8D followed by 16-bit address.
- Writing MAP register 0x000E uses SPI op code 0x8E followed by 16-bit address.

To read the active MAP register, use a fast-access write op code. The current MAP 16-bit value is clocked out in the next 16 sequential SCK clock cycles:

- Reading MAP register 0x000B uses SPI op code 0x2C
- Reading MAP register 0x000C uses SPI op code 0x30
- Reading MAP register 0x000D uses SPI op code 0x34

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- Reading MAP register 0x000E uses SPI op code 0x38

While SPI command op codes are always 8 bits, transacted addresses and register or memory data are always 16-bit words, transferred by the SPI as two sequential bytes. After a 2-byte read/write completion, the active Memory Address Pointer automatically increments to the following register address. The host can extend the read or write operation to the next register address by continuing to hold CE low while clocking SCK 16 additional times. This auto-increment feature can be used to access one or more sequential register addresses above the command address. Auto-increment applies (ranging to the top of the address space) as long as SCK continues to be clocked under continuous CE assertion. Caution: When the primary address pointer is used for auto-incrementing multi-word read/write and reaches the top of the address range (0x7FFF) the next increment rolls over the MAP value to 0x0000. The host should avoid this situation.

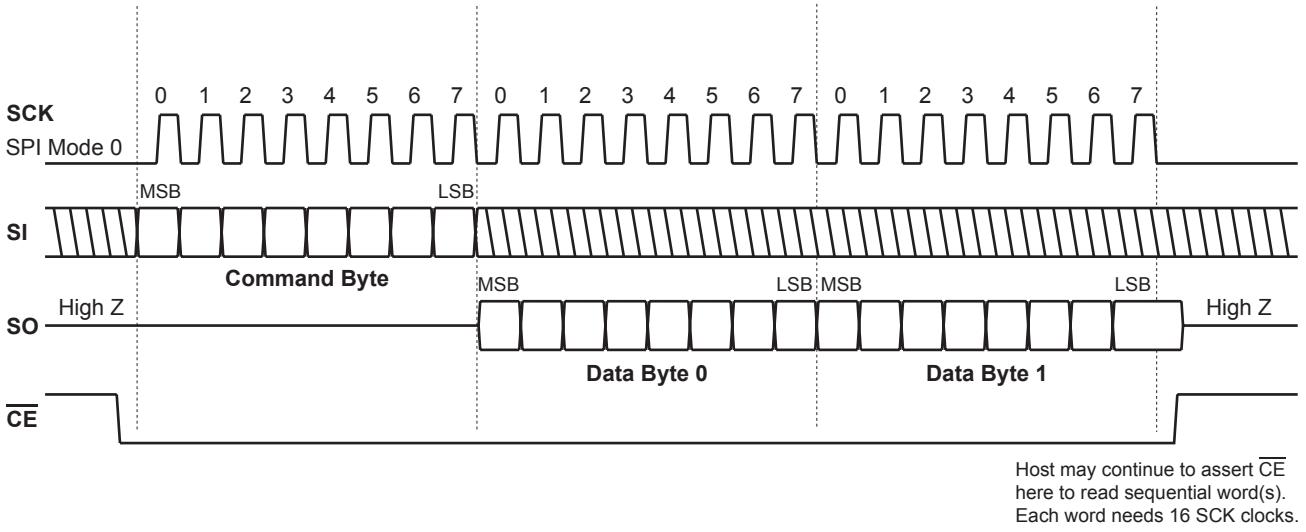

Figure 27. Single-Word (2-Byte) Read From RAM or a Register

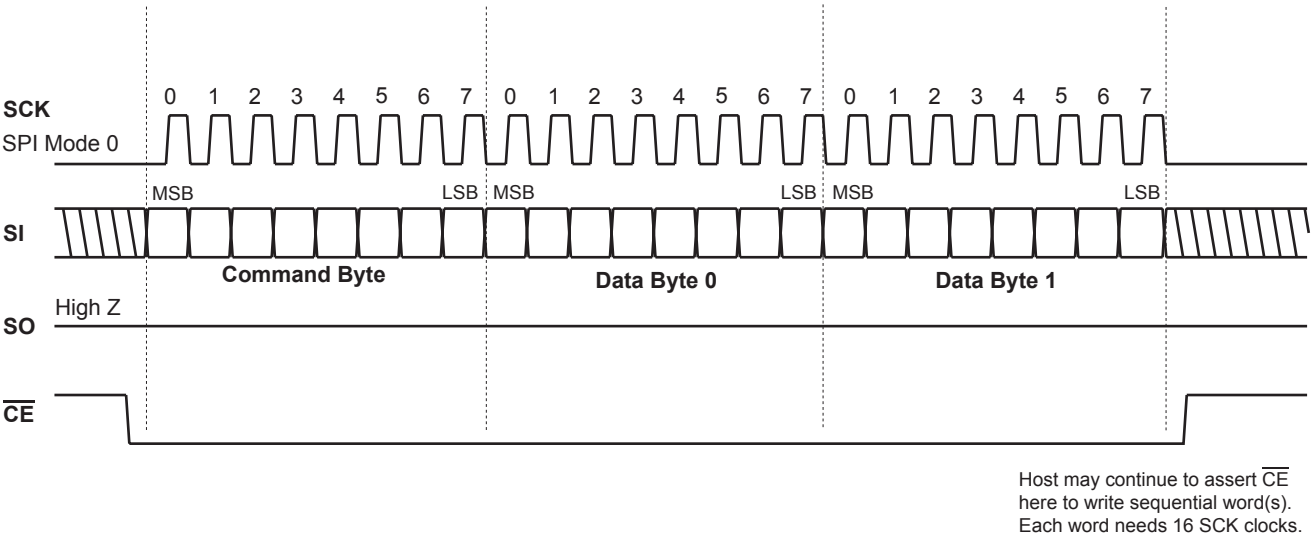

Figure 28. Single-Word (2-Byte) Write To RAM or a Register

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Three single-byte SPI commands modify the value in the active Memory Address Pointer, selected by MAP-SEL bits 11-10 in the Master Configuration Register:

Command	Address Pointer Operation
0xD0	increment enabled Memory Address Pointer value
0xD2	add 2 to enabled Memory Address Pointer value
0xD4	add 4 to enabled Memory Address Pointer value

The “Add 4” command may be useful when sequentially accessing the same word (for example, the Control Word) in a series of 4-word Descriptor Table entries. The “Add 2” command might be useful for reading the Interrupt Log Buffer, comprised of 2-word log entries. In both cases, the Add command would be probably followed by Read command 0x40 to read the location addressed by the current pointer value. Similarly, Write command 0xC0 writes the location addressed by the current pointer value. Two command bytes cannot be “chained”; the host SPI Slave Select CE must be negated after the Add command, then reasserted for the following Read or Write command.

The active Memory Address Pointer is not affected by fast-access read/writes to the low register addresses because fast-access SPI commands use a separate, internal pointer not directly accessible to the host.

Two single-byte SPI commands use the current value of the enabled Memory Address Pointer without first loading or otherwise modifying it:

Command	Read Operation
0x40	read location addressed by enabled Memory Address Pointer

Command	Write Operation
0xC0	write location addressed by enabled Memory Address Pointer

Either of these commands can be used to read or write a single location, or may be used to start a multi-word read or write that uses the MAP pointer’s auto-increment feature.

One single-byte SPI command increment the current value of the enabled Memory Address Pointer, then performs a write:

Command	Write Operation
0xC8	add 1 to enabled Memory Address Pointer then write addressed location

24.2.6. Data Prefetch for SPI Read Cycles

Data prefetch is a technique used by the HI-6131 to speed up host multi-word read access to registers or RAM. Prefetching occurs when HI-6131 logic accesses data before it is actually needed. Because register or RAM locations are often read sequentially, performance improves when data is prefetched in address sequence order. For any SPI read cycle, the HI-6131 first fetches the addressed location, then increments the memory address pointer and prefetches the following address, to speed up access in the likely event that the following word will be read next. For the HI-6131, read cycle prefetch allows the SPI host to read sequential locations back-to-back, continuing as long as the host asserts chip select and provides SPI clock. This is described as the Memory Address Pointer “auto-increment” feature.

There is an exception: read cycle prefetch is blocked when the next RAM address is a Control Word in the RT1 or RT2 Descriptor Table. If allowed, pre-fetch (like any other read) resets the Control Word DBAC status bit. To preserve DBAC status bit function, prefetch is disabled when reading Control Words within Descriptor Table address range. The table base address (set by the value in register 0x0019 for RT1 or register 0x0022 for RT2) and every fourth word thereafter is a Control Word. This consists of table addresses having these offsets from the table start address: 0, 4, 8, 0xC through and including 0x1F8 and 0x1FC. See further information in Section 24.2.8.

These two commands can be used to read or write a single location, or may be used to start a multi-word read or write that uses the pointer’s auto-increment feature.

24.2.7. Special Purpose Commands

Several other HI-6131 SPI commands load or otherwise modify the active Memory Address Pointer before initiating a read or write process. These commands were tailored to the specific needs of HI-6131 Remote Terminal host software.

Using a single-byte SPI command, the active Memory Address Pointer can be directly loaded with the memory address for the RT1 or RT2 descriptor table Control Word corresponding to the last completed MIL-STD-1553 command. The Control Word is then read.

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Command	Read Operation
0x48	Copy RT1 Current Control Word Address register 3 into the enabled Memory Address Pointer. Read the location addressed by the new pointer value.
0x50	Copy RT2 Current Control Word Address register 5 into the enabled Memory Address Pointer. Read the location addressed by the new pointer value.

This command can be used to read just the current RT1 or RT2 Control Word, or may be used to start a multi-word read because memory pointer auto-increment occurs after the Control Word is read.

Six single-byte SPI commands add an offset to the current address pointer value, then read the addressed memory location; the read value is then written to the address pointer register 15. The new pointer value is used to start a read or write operation:

Command	Read Operation
0x68	Read the location addressed by the enabled Memory Address Pointer. Write the value just read into the Memory Address Pointer. Then read.
0x70	Add 1 to the enabled Memory Address Pointer. Read value at newly addressed loca-tion and write it into the Memory Address Pointer. Then read.
0x78	Add 2 to the enabled Memory Address Pointer. Read value at newly addressed loca-tion and write it into the Memory Address Pointer. Then read.

Command	Write Operation
0xE8	Read the location addressed by the enabled Memory Address Pointer. Write the value just read into the Memory Address Pointer. Then write.
0xF0	Add 1 to the enabled Memory Address Pointer. Read value at newly addressed loca-tion and write it into the Memory Address Pointer. Then write.
0xF8	Add 2 to the enabled Memory Address Pointer. Read value at newly addressed loca-tion and write it into the Memory Address Pointer. Then write.

Primary use occurs when an RT1 or RT2 Descriptor Table Control Word was just read. For example, the last op code performed was 0x48, reading the RT1 Control Word for the last command. After reading the Control Word, the enabled Memory Address Pointer automatically incremented. The host can examine flag bits contained in the just-read Control Word to determine the applicable data buffer (e.g., Data Buffer A, Data Buffer B or the Broadcast Data Buffer) then directly service that buffer using these op codes; the three data buffer pointers occur in the three words following the initially read Control Word.

These six commands can be used to read or write a single location, or may be used to start a multi-word read or write that uses the pointer's auto-increment feature.

When some or all subaddress or mode commands are not programmed to trigger host interrupts, a different single-byte SPI command may be useful if polling the RT1 or RT2 Descriptor Table for message activity. In this situation, the host may poll a series of Descriptor Table Control Words looking for instances where the DBAC activity bit is set. The DBAC (Descriptor Block Accessed) flag is set in the Control Word each time the corresponding command is completed. The process of reading the Control Word automatically resets the register's DBAC bit so the host can detect activity the next time the DBAC flag is set by the device.

Since RT1 or RT2 Descriptor Table Control Words are spaced four words apart, this command is useful when polling a series of descriptor table Control Words:

Command	Read Operation
0x60	read addressed location then add 4 to pointer

Primary use occurs when the address pointer initially points to the first Descriptor Table Control Word in a series of Control Words to be polled (every fourth word).

After 8 SCK clocks for the SPI command, each instance of this command reads a single location using 16 SCK clocks. If CS remains low after 24 clocks and SCK continues, a multi-word read begins, using the address pointer's auto-increment feature. The second word read is at (Control Word address + 4), the next Control Word in the table.

Another single-byte SPI command is useful when servicing interrupts. When enabled interrupts occur, two words are written to the circular 64-word Interrupt Log Buffer, and the Interrupt Log Address register 0x000A is updated to show the storage address where interrupt information words will be stored for the next occurring interrupt. Buffer starting address is 0x0180 and ending address is 0x01BF. Because two words are written to

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the buffer for each interrupt, the Interrupt Log Address register always contains an even value in the range of 0x0180 to 0x01BE.

When servicing an interrupt that just occurred, the host wants timely information on that interrupt. An SPI command is provided to simplify interrupt handling:

Command	Read Operation
0x58	Write enabled Memory Address Pointer with the current bit 8:0 address value in Interrupt Log Address register minus 1. (See note.) If address bits 8:0 equal 0x0180, then 0x1BF is written into Memory Address Pointer. Then read the newly-addressed RAM location, containing the last-written Interrupt Address Word. Then decrement the Memory Address Pointer, which then addresses the corresponding Interrupt Information Word

Note: Bits 15:9 in the Interrupt Log Address register contain the interrupt count since the Log Address register was last read. These bits are not written to the Memory Address Pointer.

This command can be used to read a single location (the last-written Interrupt Address Word), or may be used to start a multi-word read in which the Memory Address Pointer automatically decrements after each word is read, reading words stored in the Interrupt Log Buffer, in Last In First Out order. This is the only SPI op code that decrements the Memory Address Pointer for multi-word operations. Repeated memory pointer decrements will wrap around the 0x0180 to 0x01BF Interrupt Log Buffer boundary.

24.2.8. RT Descriptor Table Prefetch Exceptions

For the SPI-interface HI-6131, the enabled Memory Address Pointer (register 0x000F) contains the address for each new word read by the host. When starting a read access, the host usually writes the enabled Memory Address Pointer with the address for the first word to read. The host then uses an SPI op code to initiate the read process. After the addressed word is transferred by SPI to the host, the HI-6131 continues to read and transmit words from sequential RAM memory addresses, as long as the host continuously asserts chip select while providing SCK serial clock pulses. After fetching each new word, the device increments the Memory Address Pointer and prefetches the data contained in the newly addressed location. The next word is prefetched even when the host does not ultimately read the following address. For HI-6131, sequential reads from the RT1 or RT2 Descriptor Table that rely on MAP auto-increment will stop advancing when the next address contains a RT Descriptor Table Control Word. Properly designed SPI transfers overcome this behavior.

Using SPI command op codes, the HI-6131 host must consider prefetch and pointer behavior when reading data from the Descriptor Table. Applied outside the RT Descriptor Table, the following SPI sequence would read data from six successive memory addresses. But below, applied within the table, the sequence gets stuck at the fourth word read.

Below we assume the RT1 Descriptor Table starts at default base address, 0x0400. The host first uses SPI op codes 0xD8 and 0x8B to enable Memory Address Pointer 0x000B then write the table start address 0x0400 into it. The sequence then uses op code 0x40 (and MAP auto-increment) to read the first MAP-addressed location and successive locations.

Notice: There is no MAP auto-increment or data prefetch when MAP equals 0x0403, so the final two read cycles repeat the previous read value and address.

```
FROM    FROM
HOST    HI-6131   COMMENT
======  ========  ========================================
0xD8    ----  SPI op enables memory address pointer (MAP) 0x000B.
0x8B    ----  SPI op code writes memory address pointer (MAP).
0x0400  ----  RT1 Descriptor Table start address written to MAP.
0x40    ----  SPI op code to "read location addressed by MAP"
----  <data>  data from 0x0400 (SCK continues afterward)
----  <data>  data from 0x0401 (SCK continues afterward)
----  <data>  data from 0x0402 (SCK continues afterward)
```


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```
---- <data> data from 0x0403 (SCK continues afterward, Control Word next)
---- <data> data from 0x0403 (SCK continues afterward, Control Word next)
---- <data> data from 0x0403 (SCK stops and /CS is then negated)
```

Using a different SPI op code sequence, the host can read the entire RT1 Descriptor Table without getting stuck at the first Control Word read by the multi-word transfer using op code 0x40:

```
FROM   FROM
HOST   HI-6131  COMMENT
===== ======= ========================================
0xD8   ---- SPI op enables memory address pointer (MAP) 0x000B.
0x8B   ---- op code writes memory address pointer (MAP)
0x03FF ---- decremented table start addr 0x0400 - 1 written to MAP

0xD0   ---- op code increments enabled MAP
0x40   ---- op code reads MAP-addressed location
---- <data> data from 0x0400 (SCK continues afterward)
---- <data> data from 0x0401 (SCK continues afterward)
---- <data> data from 0x0402 (SCK continues afterward)
---- <data> data from 0x0403 (SCK stops and /CS is negated)

0xD0   ---- op code increments enabled MAP
0x40   ---- op code reads MAP-addressed location
---- <data> data from 0x0404 (SCK continues afterward)
---- <data> data from 0x0405 (SCK continues afterward)
---- <data> data from 0x0406 (SCK continues afterward)
---- <data> data from 0x0407 (SCK stops and /CS is negated)

0xD0   ---- op code increments enabled MAP
0x40   ---- op code reads MAP-addressed location
---- <data> data from 0x0408 (SCK continues afterward)
---- <data> data from 0x0409 (SCK continues afterward)
---- <data> data from 0x040A (SCK continues afterward)
---- <data> data from 0x040B (SCK stops and /CS is negated)
```

The host may repeat this sequence until the entire RT1 Descriptor Table is read. The repeating read process is not shown, but the sequence could end like this, stopping at the upper table boundary…

```
0xD0   ---- op code increments enabled MAP
0x40   ---- op code reads MAP-addressed location
---- <data> data from 0x05FC (SCK continues afterward)
---- <data> data from 0x05FD (SCK continues afterward)
---- <data> data from 0x05FE (SCK continues afterward)
---- <data> data from 0x05FF (SCK stops and /CS is negated) TABLE ENDS
```

In most situations, the repeating op code block (0xD0 with 8 SCK clocks and op code 0x40 with 72 SCK clocks) would be implemented as a loop, rather than straight-line code. A total of 128 loop repetitions would be required to read the RT Descriptor Table from start to finish.

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Table 23. Fast-Access SPI Commands for Lower Registers

Op Code Bits 5:2 Convey the 4-Bit Register Read Address.
Command Bits 5:0 Convey the 6-Bit Register Write Address.

Command Bits 7 6 5 4 3 2 1 0	HEX Byte	Fast-Access Read	Command Bits 7 6 5 4 3 2 1 0	HEX Byte	Fast-Access Write
0 0 0 0 0 0 0 0	0x00	Read Register 0	1 0 0 0 0 0 0 0	0x80	Write Register 0
0 0 0 0 0 1 0 0	0x04	Read Register 1	1 0 0 0 0 0 0 1	0x81	Write Register 1
0 0 0 0 1 0 0 0	0x08	Read Register 2	1 0 0 0 0 0 1 0	0x82	Write Register 2
0 0 0 0 1 1 0 0	0x0C	Read Register 3	1 0 0 0 0 0 1 1	0x83	Write Register 3
0 0 0 1 0 0 0 0	0x10	Read Register 4	1 0 0 0 0 1 0 0	0x84	Write Register 4
0 0 0 1 0 1 0 0	0x14	Read Register 5	1 0 0 0 0 1 0 1	0x85	Write Register 5
0 0 0 1 1 0 0 0	0x18	Read Register 6	1 0 0 0 0 1 1 0	0x86	Write Register 6
0 0 0 1 1 1 0 0	0x1C	Read Register 7	1 0 0 0 0 1 1 1	0x87	Write Register 7
0 0 1 0 0 0 0 0	0x20	Read Register 8	1 0 0 0 1 0 0 0	0x88	Write Register 8
0 0 1 0 0 1 0 0	0x24	Read Register 9	1 0 0 0 1 0 0 1	0x89	Write Register 9
0 0 1 0 1 0 0 0	0x28	Read Register 10	1 0 0 0 1 0 1 0	0x8A	Write Register 10
0 0 1 0 1 1 0 0	0x2C	Read Register 11	1 0 0 0 1 0 1 1	0x8B	Write Register 11
0 0 1 1 0 0 0 0	0x30	Read Register 12	1 0 0 0 1 1 0 0	0x8C	Write Register 12
0 0 1 1 0 1 0 0	0x34	Read Register 13	1 0 0 0 1 1 0 1	0x8D	Write Register 13
0 0 1 1 1 0 0 0	0x38	Read Register 14	1 0 0 0 1 1 1 0	0x8E	Write Register 14
0 0 1 1 1 1 0 0	0x3C	Read Register 15	1 0 0 0 1 1 1 1	0x8F	Write Register 15
decimal 15 is end of read address range			1 0 0 1 0 0 0 0	0x90	Write Register 16
			1 0 0 1 0 0 0 1	0x91	Write Register 17
			1 0 0 1 0 0 1 0	0x92	Write Register 18
			1 0 0 1 0 0 1 1	0x93	Write Register 19
			1 0 0 1 0 1 0 0	0x94	Write Register 20
			1 0 0 1 0 1 0 1	0x95	Write Register 21
			and so on, to 63 decimal		. .
			1 0 1 1 1 1 0 1	0xBD	Write Register 61
			1 0 1 1 1 1 1 0	0xBE	Write Register 62
			1 0 1 1 1 1 1 1	0xBF	Write Register 63
			decimal 63 is end of write address range		

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Table 24. SPI Commands using Memory Address Pointer

Hex Byte	Read or Write	Read
Select / Enable a Memory Address Pointer		
0xD8	-------	Enable Memory Address Pointer at register 0x000B
0xD9	-------	Enable Memory Address Pointer at register 0x000C
0xDA	-------	Enable Memory Address Pointer at register 0x000D
0xDB	-------	Enable Memory Address Pointer at register 0x000E
Memory Address Pointer Operations (no data is written or read)		
0xD0	-------	Add 1 to the current value of the enabled Memory Address Pointer
0xD2	-------	Add 2 to the current value of the enabled Memory Address Pointer
0xD4	-------	Add 4 to the current value of the enabled Memory Address Pointer
Read / Write RAM or Register Location Using Current Address Pointer Value		
0x40	R	Read location addressed by the current value of the enabled Memory Address Pointer
0xC0	W	Write location addressed by the current value of the enabled Memory Address Pointer
Increment Address Pointer Then Write Addressed RAM or Register Location		
0xC8	W	Write addressed location after incrementing the enabled Memory Address Pointer
Special Purpose Commands		
0x48	R	Copy RT1 current Control Word address (register 3) to enabled Memory Address Pointer, then read the location addressed by the new pointer value (read the current Control Word for RT1)
0x50	R	Copy RT2 current Control Word address (register 5) to enabled Memory Address Pointer, then read the location addressed by the new pointer value (read the current Control Word for RT2)
0x68	R	Add 0 to the current value of the enabled Memory Address Pointer. Then . . .
0x70	R	Add 1 to the current value of the enabled Memory Address Pointer. Then . . .
0x78	R	Add 2 to the current value of the enabled Memory Address Pointer. Then copy value from newly addressed location to the enabled Memory Address Pointer then read newly addressed location.
0xE8	W	Add 0 to the current value of the enabled Memory Address Pointer. Then . . .
0xF0	W	Add 1 to the current value of the enabled Memory Address Pointer. Then . . .
0xF8	W	Add 2 to the current value of the enabled Memory Address Pointer. Then copy value from newly addressed location to the enabled Memory Address Pointer then write newly addressed location.
0x60	R	Read then add 4 to the current value of the enabled Memory Address Pointer.
0x58	R	Write storage address of last-written Interrupt Address Word to the enabled Memory Address Pointer, then read the Interrupt Address Word from the Interrupt Log buffer. Decrement Memory Address Pointer after read operation

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25. APPENDIX: RT MESSAGES RESPONSES, OPTIONS & EXCEPTIONS

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
Invalid Command Word (Manchester, parity or bit count error)	No terminal response, the message is ignored. No Status Word change.	No change	No Message Info Word is written	None
Any valid command to RT31 (broadcast). when the BCSTINV bit in Configuration Register 1 equals 1.	No terminal response, the message is ignored. No Status Word change. (Broadcast commands are rendered invalid.)	No change	No Message Info Word is written	None
RT Address Parity Error based on RTA and RTAP bits in the Operational Status Register	For commands to the RT's own address or to broadcast address RT31: No terminal response, message is ignored. No Status Word change.	No change	No Message Info Word is written	RTAPF (not optional)
Any valid non-mode (subaddress 1-30) transmit command to RT31 (undefined broadcast transmit).	No terminal response, Set Message Error (ME) and BCR status bits.	DBAC bit set. DPB bit toggles. BCAST bit set.	MERR bit set. BUSID bit updated.	IWA IBR (IXEQZ)
Any valid non-mode (subaddress 1-30) transmit command except for RT31. The corresponding bit in the Illegalization Table equals 0.*	Normal Status Word response (Clear Status). Data words for transmit are read from the RAM data buffer assigned by the Descriptor Table entry for the transmit subaddress.	DBAC bit set. DPB bit toggles. BCAST bit reset.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit updated. (Other error bits reset).	IWA IBR (IXEQZ)
Any valid non-mode (subaddress 1-30) transmit command except for RT31. The corresponding bit in the Illegalization Table equals 1. **	Assert Message Error (ME) status, then transmit ME Status Word without following data words.	DBAC bit set. DPB bit toggles. BCAST bit reset.	ILCMD bit set. BUSID bit updated. MERR bit set. RTRT bit updated. (Other error bits reset).	ILCMD IWA
Any valid non-mode (subaddress 1-30) receive command. The corresponding bit in the Illegalization Table equals 0. *	Normal Status Word response (Clear Status). After message completion, the data words received are stored in the data buffer RAM location assigned by the Descriptor Table entry for the receive subaddress.	DBAC bit set. DPB bit toggles. BCAST bit reset.	Normal update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit updated. (Other error bits reset).	IWA IBR (IXEQZ)

* Terminal is using "illegal command detection" and command is legal
OR terminal is not using "illegal command detection" and command may be legal or illegal (in form response).
** Terminal is using "illegal command detection" and command is illegal.

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
Any valid non-mode (subaddress 1-30) receive command. The corresponding bit in the Illegalization Table equals 1. **	Assert Message Error (ME) status and set BCR if broadcast. Any received data words are ignored and are not saved. When data reception stops, transmit Status Word.	DBAC bit set. DPB bit toggles. BCAST bit updated.	ILCMD bit set. BUSID bit updated. MERR bit set. RTRT bit updated. (Other error bits reset)	ILCMD IWA IBR (IXEQZ)
Valid receive command followed by invalid data word (Manchester, parity or bit count error).	No terminal response. Set Message Error (ME) status. If broadcast (RT31), also set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. BUSID bit updated. IWDERR bit set. ILCMD bit reset. RTRT bit updated (Other error bits reset).	MERR IWA IBR
Valid receive command followed by one or more good data words, then a data word having Command Sync.	No terminal response. Set Message Error (ME) status. If broadcast (RT31), also set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. BUSID bit updated. SYNERR bit set. ILCMD bit reset. (Other error bits reset).	MERR IWA IBR
Any valid command followed by wrong number of data words (too few or too many words)	No terminal response. Set Message Error (ME) status. If broadcast (RT31), also set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. BUSID bit updated. Set WCTERR (too few) or GAPERR (too many). ILCMD bit reset. RTRT bit updated. (Other error bits reset).	MERR IWA IBR
RT-RT where CW1 is a valid non-mode receive command. CW2 is a non-mode transmit command valid for different RT. (Normal RT-RT receive message)	Normal Status Word response (Clear Status). If RT-RT Command Word 1 is broadcast (RT31) set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. RTRT bit set. RTCWERR bit reset. ILCMD bit reset. (All error bits reset).	IWA IBR (IXEQZ)
RT-RT where CW1 is a valid non-mode receive command. Transmit command CW2 has an error: T/$\overline{R}$ bit = 0, or CW2 subaddress equals 0 or 31 (mode code), or CW2 has same RT address as CW1.	No terminal response. Set Message Error (ME) status. If RT-RT Command Word 1 is broadcast (RT31) also set the BCR status bit,	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. BUSID bit updated. RTRT bit set. RTRTCWERR bit set. ILCMD bit reset. (Other error bits reset).	MERR IWA IBR

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
RT-RT where CW1 is a valid non-mode receive command. CW2 is valid for different RT but transmitting RT does not respond in time.	No terminal response. Set Message Error (ME) status. If RT-RT Command Word 1 is broadcast (RT31), also set the BCR status bit.	DBAC bit set. BCAST bit updated DPB bit toggles.	MERR bit set. BUSID bit updated. RTRT bit set. TMOERR bit set. ILCMD bit reset. (Other error bits reset).	MERR IWA IBR
RT-RT receive command (CW1 is valid). The transmitting RT response has one of these errors: invalid word (Manchester, (sync, bit count, parity or word count error). Also includes transmitting RT response with Message Error or Busy status followed by no data words.	No terminal response. Set Message Error (ME) status. If RT-RT Command Word 1 is broadcast (RT31) also set the BCR status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. BUISID bit reset. RTRT bit set. IWDERR bit set, or WCTERR bit set for Tx RT Busy case. ILCMD bit reset. (Other error bits reset).	MERR IWA IBR
RT-RT command where CW2 is a valid non-mode (subaddress 1-30) transmit command. CW1 is a non-mode receive command for RT31. (Normal broadcast RT-RT transmit)	Normal Status Word response. Clear status is transmitted with the commanded number of data words. Data words for transmit are read from the RAM data buffer assigned in the Descriptor Table entry for the transmit subaddress.	DBAC bit set. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit set. (All error bits reset).	IWA (IXEQZ)
Valid mode code command to RT31 (broadcast). The BCSTINV bit in Configuration Register 1 equals 1.	No terminal response, the message is ignored. No Status Word change.	No change	No Message Info Word is written	None
Valid undefined mode code command. The UMCINV bit in Configuration Register 1 equals 1.	No terminal response, the message is ignored. No Status Word change. **NOTE:** This only applies for the undefined mode codes: MC0 to MC15 with T/$\overline{R}$ = 0 MC16,18 & 19 with T/$\overline{R}$ = 0 MC17,20 & 21 with T/$\overline{R}$ = 1	No change	No Message Info Word is written	None

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
Valid defined mode code command (including reserved mode code) not "illegalized" by Illegalization Table (table bit equals 0 *)	If MC2 (transmit status) or MC18 (transmit last command) status word from last command is transmitted. If MC18, data word transmitted is read from an internal register. **OR** If not MC2 or MC18, normal Status Word response. If broadcast, assert Status Word BCR bit. For mode codes 16-31 with T/$\overline{R}$ bit = 1 which transmit a data word, the word for transmit is read from the Mode Command Data Table. **AND** For all mode commands with mode data word (mode codes 16-31), the transmitted or received data word is written to command's Descriptor Word 4.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR (IXEQZ)
Valid defined mode code command that is "illegalized" by the IllegalizationTable (table bit equals 1 **)	Set Message Error (ME) status. If not broadcast (RT31), transmit. Status Word without a following mode data word. If broadcast (RT31), also assert the BCR status bit. **AND** For mode commands with a mode data word (mode codes 16-31), no updates are made to the Mode Command Data Table or to the command's Word 4 in Descriptor Table.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. BUSID bit updated. MERR bit reset. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR

* Terminal is using "illegal command detection" and command is legal
OR terminal is not using "illegal command detection" and command may be legal or illegal (in form response).
** Terminal is using "illegal command detection" and command is illegal.

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
Valid undefined mode code command. The UMCINV bit in Configuration Register 1 equals 0.	If bit in Illegalization Table that corresponds to the undefined mode code command equals 1 ** Set Message Error (ME) status, If not broadcast (RT31), transmit Status Word without a following mode data word. If broadcast (RT31), also assert the BCR status bit. **OR** If bit in Illegalization Table that corresponds to the undefined mode code command equals 0 * Normal Status Word (Clear Status) response. If command was broadcast (RT31), assert the BCR status bit. **AND** For mode codes 16-31 with T/$\overline{R}$ bit = 1 which transmit a data word, the word for transmit is read from the Mode Command Data Table. **AND** For all mode commands with mode data word (mode codes 16-31), the transmitted or received data word is written to command's Descriptor Word 4.	DBAC bit set. BCAST bit updated. DPB bit toggles. DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. BUSID bit updated. MERR bit reset. RTRT bit reset. (Other error bits reset.) Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	ILCMD IWA IBR IWA IBR (IXEQZ)

* Terminal is using "illegal command detection" and command is legal
OR terminal is not using "illegal command detection" and command may be legal or illegal (in form response).
** Terminal is using "illegal command detection" and command is illegal.

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
Valid receive command followed by invalid data word (Manchester, parity or bit count error).	No terminal response. Set Status Word ME bit, If broadcast, also set Status Word BCR bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. BUSID bit updated. IWDERR bit set. ILCMD bit reset. RTRT bit updated. (Other error bits reset.)	MERR IWA IBR
Superseded Message: Terminal receives an incomplete message interrupted by a gap of at least 3.5 us, followed by a new valid command on the same bus or on the other bus **OR** Terminal is transacting a transmit message on one bus and receives the start of a valid command on the other bus.	Terminal aborts processing for first message and responds in full to the second (superseding) message. The Status Word BCR bit reflects broadcast status for: the second command, unless second command is MC2 (transmit status) or MC18 (transmit last command).	No change to superseded command's Control Word. For superseding command's Control Word: DBAC bit set. BCAST bit updated DPB bit toggles.	No Msg Info Word written for the superseded command. For superseding command's data buffer, a normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit updated. (All error bits reset.)	None for super-seded command IWA IBR (IXEQZ)
Terminal is Busy for a valid receive command either globally (BUSY bit set in Status Word Bits register) or in response to a particular valid receive command (MKBUSY bit set in the command's Descriptor Table control word.)	Busy bit is set in the 1553 Status Bits register. Status Word is transmitted, unless broadcast. If broadcast, the BCR bit in Status Word is also set. After message completion, data words received are stored in the data buffer assigned by the receive subaddress Descriptor Table entry.	DBAC bit set. BCAST bit updated. DPB bit toggles.	WASBSY bit set. BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit updated. (All error bits reset.)	IWA IBR
Terminal is Busy for a valid transmit command either globally (BUSY bit set in Status Word Bits register) or in response to a particular valid receive command (MKBUSY bit set in the command's Descriptor Table control word.)	Busy bit is set in the 1553 Status Bits register. If not broadcast, Status Word is transmitted without data. If broadcast, the BCR bit in Status Word is also set.	DBAC bit set. BCAST bit updated, (mode commands with T/$\overline{R}$ = 1) DPB bit toggles	WASBSY bit set. BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit updated. (All error bits reset.)	IWA IBR

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
DYNAMIC BUS CONTROL (MC0): Mode code command with mode code 00000 and T/$\overline{R}$ bit equals 1	HI-6110 is not equipped to accept bus control duties. The host must initialize device to respond using either of the two following methods:			
The mode code's bit in Illegalization Table equals 0 *	RT is not using "illegal command detection." Respond "in form": Reset Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
OR The mode code's bit in Illegalization Table equals 1 **	**OR** RT is using "illegal command detection"and mode code is illegalized. Set Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit reset. DPB bit toggles.	ILCMD bit set. BUSID bit updated. MERR bit reset. RTRT bit reset. (Other error bits reset.)	ILCMD IWA
MC0 EXCEPTIONS:				
Broadcast address RT31 (broadcast not allowed)	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB toggles.	MERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD, RTRT bits reset. (Other error bits reset.)	MERR IWA
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (MC0 is not ndefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None

* Command is illegal but terminal is not using "illegal command detection" (in form response).
** Command is illegal and terminal is using "illegal command detection"
*** Undefined mode command rendered invalid by UMCINV option bit. Command's bit in Illegalization Table is "don't care".

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 0. Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 0. Illegalization Table bit equals 1 **	Set Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit reset. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
SYNCHRONIZE WITHOUT DATA (MC1): Mode code command with mode code 00001 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set the Status Word BCR bit and suppress Status Word transmit. Reset the Time Tag counter to 0x0000.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
MC1 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response. The Time Tag counter is not reset.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response. The Time Tag counter is not reset.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
TRANSMIT STATUS (MC2): Mode code command with mode code 00010 and T/$\overline{R}$ bit equals 1	No Status Word updates, Transmit Status from last valid command (assuming last command was not a "Transmit Status" or a "Transmit last Command" mode command.	DBAC bit set. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
MC2 EXCEPTIONS:				
Broadcast address RT31 (broadcast not allowed)	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB bit toggles.	MERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0 The Illegalization Table bit equals 0 *	Respond "In form": Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response. Time Tag counter is not reset.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0 The Illegalization Table. bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
INITIATE SELF TEST (MC3): Mode code command with mode code 00011 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set the Status Word BCR bit and suppress status transmit. Host should initiate self-test then update Built-In Test word at shared RAM address 0x0093. Resume terminal execution.	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
MC3 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
TRANSMITTER SHUTDOWN (MC4): Mode code command with mode code 00100 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set Status Word BCR bit and suppress status. transmit. After Status transmission, inhibit the inactive bus:	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
The device automatically shuts down either **transmit and receive** or **transmit only** for the inactive bus, depending on the state of the SDSEL bit in Configuration Register 2. (See description of SDSEL and MCOPT4 bits in Configuration Register 2 for further information. When a bus transmitter (or transmitter and receiver) is shut down by mode command, bus status is reflected by assertion of a TXASD or TXBSD bit in the Built-In Test Register at register address 0x0014. If SDSEL equals logic 0, an RXASD or RXBSD bit will also be asserted. See Built-In Test Register description for further information. Once shutdown, the inactive bus transmitter (or transmitter and receiver can only be reactivated by an “Override Transmitter Shutdown” MC5 or MC21 or “Reset Remote Terminal” MC8 mode code command, or by software reset (by setting the SRST bit in Configuration Register 1) or by hardware reset initiated by asserting the MR master reset input pin.				
MC4 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
OVERRIDE TRANSMITTER SHUTDOWN (MC5): Mode code command with mode code 00101 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set the Status Word BCR bit and suppress status transmit. This command is only used with dual redundant buses. After Status transmission, reactivate inactive bus:	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
The device automatically re-enables **transmit and receive** for the inactive bus, regardless of the state of the SDSEL bit in Configuration Register 2. The device affirms reenabled bus status by resetting all four TXASD, TXBSD, RXASD and/or RXBSD bits in the Built-In Test Register at register address 0x0014. Note: If the TXINHA or TXINHB input pins are asserted, the device cannot override the resulting hardware transmit inhibit for the affected bus. In this case, the corresponding TXASD and/or TXBSD bits remain high. See Built-In Test Register description for further information.				
MC5 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
INHIBIT TERMINAL FLAG BIT (MC6): Mode code command with mode code 00110 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set the Status Word BCR bit and suppress status transmit.	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
The device automatically sets the TF Inhibit bit in the BIT Word register at address 0x0013. While the TF inhibit bit is set, the device disregards assertion of the Terminal Flag (TF) bit in the 1553 Status Bits register (0x0006) and only transmits status with the Terminal Flag status bit reset. Once the Terminal Flag has been inhibited, it can be reactivated by an "Override Inhibit Terminal Flag" MC7 or "Reset Remote Terminal" MC8 mode command, by software reset (asserting the SRST bit in Configuration Register 1) or by asserting the $\overline{MR}$ master reset input pin.				
MC6 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond "In form": Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
OVERRIDE INHIBIT TERMINAL FLAG BIT (MC7): Mode code command with mode code 00111 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set the Status Word BCR bit and suppress status transmit.	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
The device automatically resets the TF Inhibit bit in the BIT Word register at address 0x0013. While the TF inhibit bit is reset, the device transmits status with the Terminal Flag status bit set if the Terminal Flag (TF) bit is asserted in the 1553 Status Bits register (0x0006).				
MC7 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
RESET REMOTE TERMINAL (MC8): Mode code command with mode code 01000 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status. If not broadcast, transmit Status Word.	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
After Status transmission, the device automatically resets the status Message Error (ME) Busy and Broadcast Command received (BCR) bits in its internal status register. The BIT Word at shared RAM address is reset to 0x0000. If either transmitter was shutdown, the shutdown condition is overridden. If the Terminal Flag (TF) status bit was inhibited, the inhibit is reset. This command does not reset any of the host-programmed registers that configure the terminal for operation. To complete the terminal reset process, the host must assert either MR hardware master reset (with or without auto-initialization) or assert the SRST bit in Configuration Register 1 to execute software reset. See following section entitled Reset and Initialization for additional details. Because MC8 requires host interaction, most applications will probably utilize the IWA interrupt to alert the host when received.				
MC8 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. GAPERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
RESERVED MODE CODES MC9 - MC15: Mode code command with mode codes 01001 through 01111 and T/$\overline{R}$ bit equals 1	The reserved mode code commands do not have defined terminal actions. Host must initialize device to respond using either of the two following methods:			
The mode code's bit in Illegalization Table equals 0 *	RT is not using "illegal command detection." Respond "in form": Reset Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit reset. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
OR The mode code's bit in Illegalization Table equals 1 **	**OR** RT is using "illegal command detection"and mode code is illegalized. Set Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. BUSID bit updated. MERR bit set. RTRT bit reset. (Other error bits reset.)	ILCMD IWA
MC9 - MC15 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond "In form": Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
TRANSMIT VECTOR WORD (MC16): Mode code command with mode code 10000 and T/$\overline{R}$ bit equals 1	Default CS response: Reset Message Error (ME) and BCR status bits. then transmit Status Word followed by the data word stored in the assigned index or ping-pong data buffer (or in Descriptor Word 4 for SMCP Simplified Mode Command Processing).	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
MC16 EXCEPTIONS:				
Broadcast address RT31 (broadcast not allowed)	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB toggles.	MERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
SYNCHRONIZE WITH DATA WORD (MC17): Mode code command with mode code 10001 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status. and transmit Status Word. If broadcast, set BCR status bit and suppress Status response.	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
Device stores received data word in the assigned ping-pong or index data buffer (or in Descriptor Word 4 for SMCP Simplified Mode Command Processing). Configuration Register 2 MCOPT2 and MCOPT3 bits allow automatic Time-Tag count loading using the data word received. If MCOPT2 equals 1, the received data word is automatically loaded to the Time-Tag counter if the low order bit of the received data word (bit 0 equals 0. If MCOPT3 equals 1, the received data word is automatically loaded to the Time-Tag counter if the low order bit of the received data word (bit 0) equals 1. If both bits are set, the received data word is unconditionally loaded into the Time-Tag counter. For non-broadcast commands, counter load occurs before status word transmission.				
MC17 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word not followed by a contiguous data word (missing data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Mode code command word followed by data word with Manchester encoding or parity error (bad data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. IWDERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”
*** Undefined mode command rendered invalid by UMCINV option bit. Command’s bit in Illegalization Table is “don’t care”.

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
TRANSMIT LAST COMMAND (MC18): Mode code command with mode code 10010 and T/$\overline{R}$ bit equals 1	Default response: Status is not updated. Transmit Status Word from the previous command, with data word containing the last valid command word (assuming it was not a "Transmit Status" or a "Transmit Last Command" mode command.	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
Transmitted data word is automatically provided from an internal register, and is copied to assigned index or ping-pong buffer (or to Descriptor Word 4 for SMCP Simplified Mode Command Processing)				
MC18 EXCEPTIONS:				
Broadcast address RT31 (broadcast not allowed)	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB toggles.	MERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond "In form": Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

* Command is illegal but terminal is not using "illegal command detection" (in form response).
** Command is illegal and terminal is using "illegal command detection"
*** Undefined mode command rendered invalid by UMCINV option bit. Command's bit in Illegalization Table is "don't care".

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
TRANSMIT BIT WORD (MC19): **Mode code command with mode code 10011** **and T/$\overline{R}$ bit equals 1**	Default response: Reset Message Error (ME) and BCR status bits. then transmit Status Word followed by data word from either BIT Word Register or Alternate BIT Word Register, depending on Configuration Reg. 2 option bit ALTBITW.	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit reset. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
Transmitted data word is automatically copied to the assigned index or ping-pong buffer (or to Descriptor Word 4 for SMCP Simplified Mode Command Processing)				
MC19 EXCEPTIONS:				
Broadcast address RT31 (broadcast not allowed)	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB toggles.	MERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”
*** Undefined mode command rendered invalid by UMCINV option bit. Command’s bit in Illegalization Table is “don’t care”.

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
SELECTED TRANSMITTER SHUTDOWN (MC20): Mode code command with mode code 10100 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status. and transmit Status Word. If broadcast, set BCR status bit and suppress Status response. This command is intended for use in 1553 systems with more than one dual redundant bus.	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA

After Status Word transmission, the device stores received data word in the assigned index or ping-pong buffer (or in Descriptor Word 4 if SMCP Simplified Mode Command Processing applies).

If the MCOPT4 bit in Configuration Register 2 equals 0, the received data word is compared to the value in the Bus Select Register corresponding to the inactive bus. For example, if the command is received on Bus A, the comparison uses the Bus B Select Register value. If the compared values match, the device automatically shuts down either **transmit and receive** or **transmit only** for the inactive bus, depending on the state of the SDSEL bit in Configuration Register 2. (See description of SDSEL and MCOPT4 bits in Configuration Register 2 for further information. When a bus transmitter (or transmitter and receiver) is shut down by this mode command, bus status is reflected by assertion of a TXASD or TXBSD bit in the Built-In Test Register at register address 0x0014. If SDSEL equals logic 0, an RXASD or RXBSD bit will also be asserted. See Built-In Test Register description for further information.

If MCOPT4 bit in Configuration Register 2 equals 1, the IWA interrupt is typically used to alert the host when an MC20 command is received. **The host** must evaluate whether the received mode data word matches the bus selection criteria. If bus selection criteria is met, **the host** fulfills bus shutdown command using one of two options:

1. set the bus shutdown bit INHBUSA or INHBUSB for the inactive bus in Configuration Register 1 **to inhibit both transmit and receive,**

OR

2. assert the transmit shutdown input pin TXINHA or TXINHB for the inactive **bus to inhibit only transmit.** The inactive bus receiver is still active and all valid commands are heeded without transmit. **This option is rarely applied.**

Once shutdown, the inactive bus transmitter (or transmitter and receiver) can only be reactivated by an “Override Transmitter Shutdown” MC5 or MC21 or “Reset Remote Terminal” MC8 mode code command, or by software reset (by setting the SRST bit in Configuration Register 1) or by hardware reset initiated by asserting the $\overline{MR}$ master reset input pin.

MC20 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond "In form": Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word not followed by a contiguous data word (missing data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. WCTERR bit updated. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Mode code command word followed by data word with Manchester encoding or parity error (bad data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. IWDERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

* Command is illegal but terminal is not using "illegal command detection" (in form response).
** Command is illegal and terminal is using "illegal command detection"
*** Undefined mode command rendered invalid by UMCINV option bit. Command's bit in Illegalization Table is "don't care".

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
OVERRIDE SELECTED TRANSMITTER SHUTDOWN (MC21): Mode code command with mode code 10101 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status. and transmit Status Word. If broadcast, set the BCR status bit and suppress Status response.	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
After Status Word transmission, the device stores received data word in the assigned index or ping-pong buffer (or in Descriptor Word 4 if SMCP Simplified Mode Command Processing applies). If the MCOPT4 bit in Configuration Register 2 equals 0, the received data word is compared to the value in the Bus Select Register corresponding to the inactive bus. For example, if the command is received on Bus A, the comparison uses the Bus B Select Register value. If the compared values match, the device automatically re-enables **transmit and receive** for the inactive bus, regardless of the state of the SDSEL bit in Configuration Register 2. The device affirms fully reenabled bus status by resetting all four TXASD, TXBSD, RXASD and/or RXBSD bits in the Built-In Test Register at register address 0x0014. Note: If the TXINHA or TXINHB input pins are asserted, the device cannot override the resulting hardware transmit inhibit for the affected bus. In this case, the corresponding TXASD and/or TXBSD bits remain high. See Built-In Test Register description for further information. If MCOPT4 bit in Configuration Register 2 equals 1, the IWA interrupt is typically used to alert the host when an MC21 command is received. **The host** must evaluate whether the received mode data word matches the bus selection criteria. If bus selection criteria is met, **the host** fulfills the “override shutdown” command using one of two options: 1. reset the bus shutdown bit INHBUSA or INHBUSB for the inactive bus in Configuration Register 1 to reenable both transmit and receive, if the host used this bit to shut down transmit and receive for an earlier MC4 or MC20 command. (Resetting this shutdown bit does not restore bus transmit capability if a TXINHA or TXINHB input pin is asserted.) **OR** 2. reset the transmit shutdown input pin TXINHA or TXINHB for the inactive bus to re-enable transmit if the host used this pin to shut down transmit only for an earlier MC4 or MC20 command.				
MC21 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word not followed by a contiguous data word (missing data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Mode code command word followed by data word with Manchester encoding or parity error (bad data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. IWDERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”
*** Undefined mode command rendered invalid by UMCINV option bit. Command’s bit in Illegalization Table is “don’t care”.

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
RESERVED MODE CODES MC22 - MC31: Mode code commands having mode codes 10110 through 11111	The reserved mode code commands do not have defined actions. Host must initialize device to respond using either of the two following methods:			
The mode code's bit in Illegalization Table equals 1 ** (RT is using "illegal command detection")	Mode code is illegalized. Set Message Error (ME) status and transmit Status Word. If T/$\overline{R}$ bit equals 1, suppress data word transmission.	DBAC bit set. BCAST bit reset. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA
OR	**OR**			
The mode code's bit in Illegalization Table equals 0 * (RT not using "illegal command detection," respond "in form")	**If T/$\overline{R}$ bit equals 1,** Reset Message Error (ME) status. Transmit Status Word with contiguous data word read from assigned index or ping-pong buffer (or from Descriptor Word 4 if the SMCP option applies.)	DBAC bit set. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
	If T/$\overline{R}$ bit equals 0, Reset Message Error (ME) status and transmit Status. If broadcast, also set BCR status and suppress Status transmit. Device stores received data word in assigned index or ping-pong buffer (or in Descriptor Word 4 if SMCP Simplified Mode Command Processing applies).	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset (All error bits reset.)	IWA IBR
MC22 - MC31 EXCEPTIONS:				
Invalid command word.	No terminal response, the message is ignored. No Status Word change.	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 and mode code command word is not followed by a contiguous data word (missing data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD, RTRT bits reset. (Other error bits reset.)	MERR IWA IBR

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
T/$\overline{R}$ bit equals 0 and command word is followed by data word with Manchester or parity error (bad data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. IWDERR bit set. BUSID bit updated. ILCMD, RTRT bits reset. (Other error bits reset.)	MERR IWA IBR
T/$\overline{R}$ bit equals 1 and mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR, WCTERR bits set. BUSID bit updated. ILCMD, RTRT bits reset. (Other error bits reset.)	MERR IWA
T/$\overline{R}$ bit equals 1 and mode code command is addressed to RT31	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB bit toggles.	MERR bit set. BUSID bit updated. ILCMD, RTRT bits reset. (Other error bits reset.)	MERR IWA IBR

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”

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26. ELECTRICAL CHARACTERISTICS

26.1. Absolute Maximum Ratings

Supply voltage (V_{DD})	-0.3 V to +5.0 V
Logic input voltage range	-0.3 V to +3.6 V
Receiver differential voltage	10 Vp-p
Driver peak output current	+1.0 A
Power dissipation at 25°C	1.0 W
Solder Temperature	275°C for 10 sec.
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

26.2. Recommended Operating Conditions

Operating Supply voltage (V_{DD})	3.3 VDC ± 5%
Operating Temperature Range	
Industrial Extended	-40°C to +85°C -55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

26.3. DC Electrical Characteristics

V_{DD} = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Operating Voltage	V_{DD}		3.15	3.3	3.45	V
Power Supply Current See Note 1 on next page	I_{CC1}	Not Transmitting	-	4	10	mA
	I_{CC2}	Continuous supply current while one bus transmits @ 100% duty cycle, 70Ω resistive load	-	720	760	mA
Power Dissipation See Note 2 on next page	PD_1	Not Transmitting	-	-	60	mW
	PD_2	Transmit one bus @ 100% duty cycle, 70Ω resistive load	-	420	550	mW
Min. Input Voltage (HI)	V_{IH}	Digital Inputs	70%	-	-	V_{DD}
Max. Input Voltage (LO)	V_{IL}	Digital Inputs	-	-	30%	V_{DD}
Min. Input Current (HI)	I_{IH}	Digital Inputs	-	-	20	I_{DD}
Max. Input Current (LO)	I_{IL}	Digital Inputs	-20	-	-	I_{DD}
Pull Up / Pull Down Current	I_{PUD}	Digital Inputs and Data Bus	-	275	-	I_{DD}
Min. Output Voltage (HI)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs	90%	-	-	V_{DD}
Max. Output Voltage (LO)	V_{IH}	I_{OUT} = 1.0mA, Digital outputs	-	-	10%	V_{DD}
RECEIVER (Measured at Point "AD" in Figure XX unless otherwise specified)						
Input Resistance	R_{IN}	Differential	20	-	-	kΩ
Input Capacitance	C_{IN}	Differential	-	-	5	pF
Common Mode Rejection Ratio	CMRR		40	-	-	dB
Input Level	V_{IN}	Differential	-	-	9	Vp-p

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Parameters		Symbol	Test Conditions	Limits			Unit
				Min	Typ	Max	
Input Common Mode Voltage		V_{ICM}		-5	-	+5	V-pk
Threshold Voltage (Direct-Coupled)	Detect	V_{THD}	1 Mhz Sine Wave (Measured at Point “AD“ in Figure XX)	1.15	-	20.0	Vp-p
	No Detect	V_{THND}		-	-	0.28	Vp-p
Threshold Voltage (Transformer-Coupled)	Detect	V_{THD}	1 Mhz Sine Wave (Measured at Point “AT“ in Figure XX)	0.86	-	14.0	Vp-p
	No Detect	V_{THND}		-	-	0.2	Vp-p
TRANSMITTER (Measured at Point “AD” in Figure XX unless otherwise specified)							
Output Voltage	Direct Coupled	V_{OUT}	35Ω Load	6.0	-	9.0	Vp-p
	Transformer Coupled	V_{OUT}	70Ω Load (Measured at Point “AT“ in Figure XX)	18.0	-	27.0	Vp-p
Output Noise		V_{ON}	Differential, inhibited	-	-	10.0	mVp-p
Output Dynamic Offset Voltage	Direct Coupled	V_{DYN}	35Ω Load	-90	-	90	mV
	Transformer Coupled	V_{DYN}	70Ω Load (Measured at Point “AT“ in Figure XX)	-250	-	250	mV
Output Resistance		R_{OUT}	Differential, not transmitting	10	-	-	kΩ
Output Capacitance		C_{OUT}	1 MHz sine wave	-	-	15	pF

Note 1: In actual use, the highest practical transmit duty cycle is 96%, occurring when a Remote Terminal responds to a series of 32 data word transmit commands (RT to BC) repeating with minimum intermessage gap of 4µs (2µs dead time) and typical HI-6110 RT response delay of 5µs.

Note 2: While one bus continuously transmits, the power delivered by the 3.3V power supply is 3.3V × 720mA typical = 2.4W. Of this, 420mW is dissipated in the device, the remainder in the load.

26.4. AC Electrical Characteristics — HI-6131 Host Bus Interface Timing

V_{DD} = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Limits			Units
		Min	Typ	Max	
HI-6131 INTERFACE TIMING (SPI Host Bus Interface)					
SCK clock Period	t_{CYC}	50	-	-	ns
$\overline{CE}$ set-up time to first SCK rising edge	t_{CES}	25	-	-	ns
$\overline{CE}$ hold time after last SCK falling edge	t_{CEH}	25	-	-	ns
$\overline{CE}$ inactive between SPI instructions	t_{CPH}	100	-	-	ns
SPI SI Data set-up time to SCK rising edge	t_{DS}	10	-	-	ns
SPI SI Data hold time after SCK rising edge	t_{DH}	10	-	-	ns
SCK high time	t_{SCKH}	25	-	-	ns
SCK low time	t_{SCKL}	100	-	-	ns
SO valid after SCK falling edge	t_{DV}	-	-	20	ns
SO high-impedance after $\overline{CE}$ inactive	t_{CHZ}	-	-	75	ns

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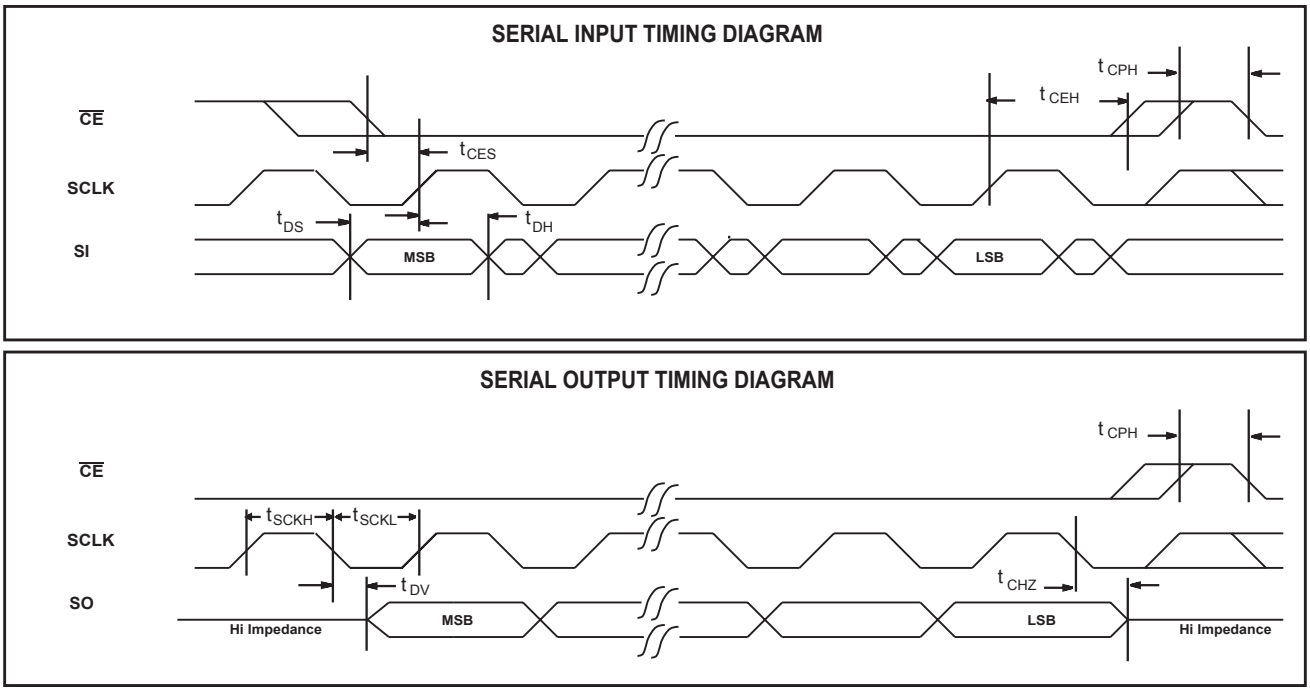

Figure 29. HI-6131 Host Bus Interface Timing Diagram

26.5. AC Electrical Characteristics — HI-6130 Host Bus Interface Timing

Parameters	Symbol	Limits			Units
		Min	Typ	Max	
HI-6130 INTERFACE TIMING (Parallel Host Bus Interface)					
Write cycle	t_{WR}	55	-	-	ns
Read/Write inactive time	t_{INACT}	25	-	-	ns
Non-sequential read time	t_{NSR}	110	-	-	ns
8-bit sequential read time	t_{SR8}	55	-	-	ns
16-bit sequential read time	t_{SR16}	65	-	-	ns
Wait assertion time	t_{WAS}	20	-	-	ns
Wait time	t_{W}	-	-	130	ns

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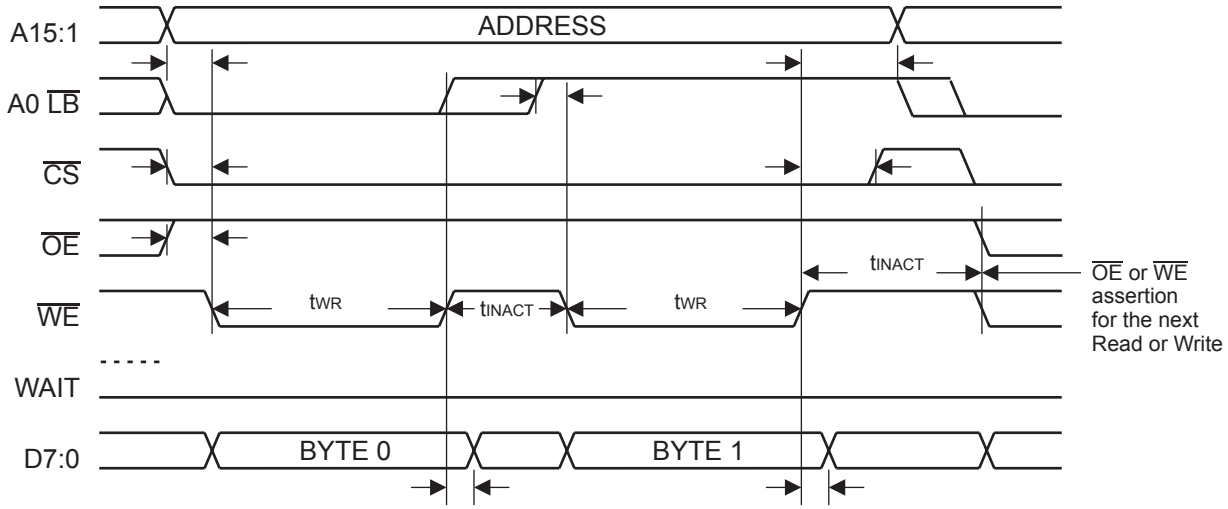
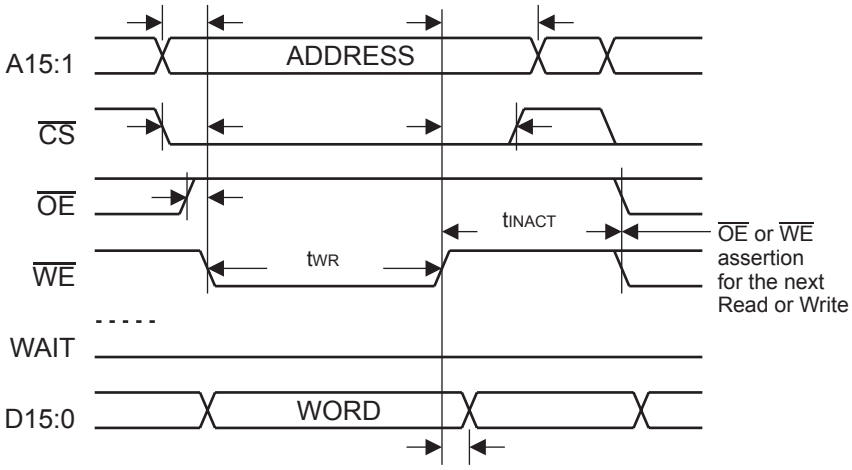
HOST WRITE IN DUAL-BYTE MODE (8-BIT BUS WIDTH)
using BTYPE = 1 (“Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)
showing 2 bytes written for a single 16-bit word



All timing intervals equal 0 ns MIN unless otherwise indicated.

HOST WRITE IN WORD MODE (16-BIT BUS WIDTH)
using BTYPE = 1 (”Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)
showing a one-word write cycle. Successive writes to sequential addresses have same timing.



All timing intervals equal 0 ns MIN unless otherwise indicated.

Figure 30. Register and RAM Write Operations for BTYPE = 1

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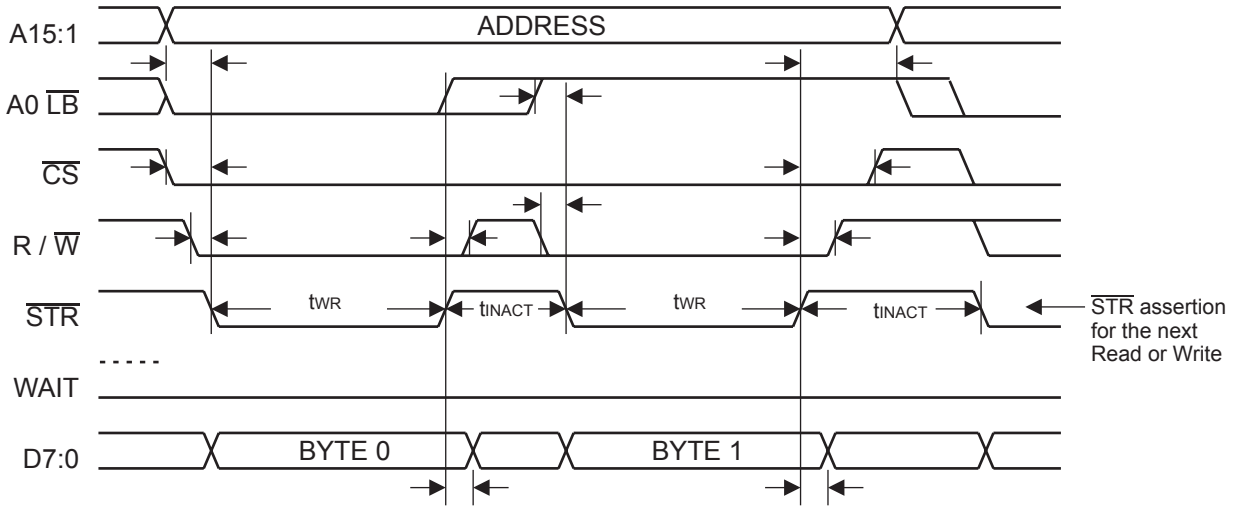
HOST WRITE IN DUAL-BYTE MODE (8-BIT BUS WIDTH)
using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)

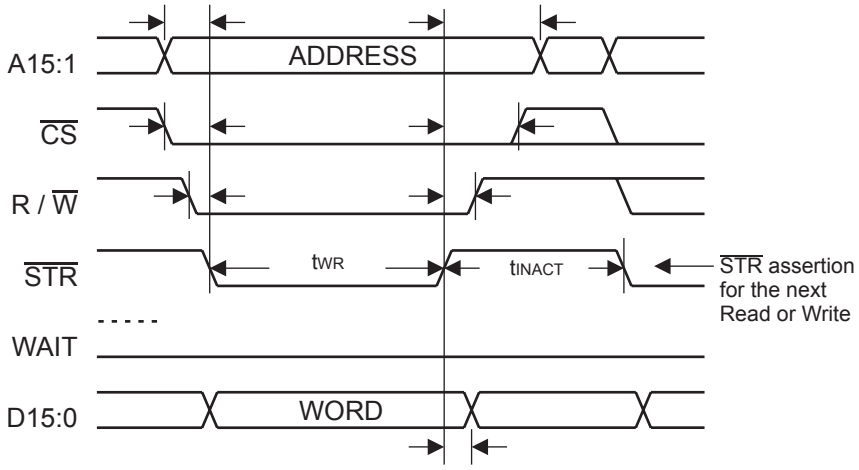
showing 2 bytes written for a single 16-bit word



All timing intervals equal 0 ns MIN unless otherwise indicated.

HOST WRITE IN WORD MODE (16-BIT BUS WIDTH)
using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)

showing a one-word write cycle. Successive writes to sequential addresses have same timing.



All timing intervals equal 0 ns MIN unless otherwise indicated.

Figure 31. Register and RAM Write Operations for BTYPE = 0

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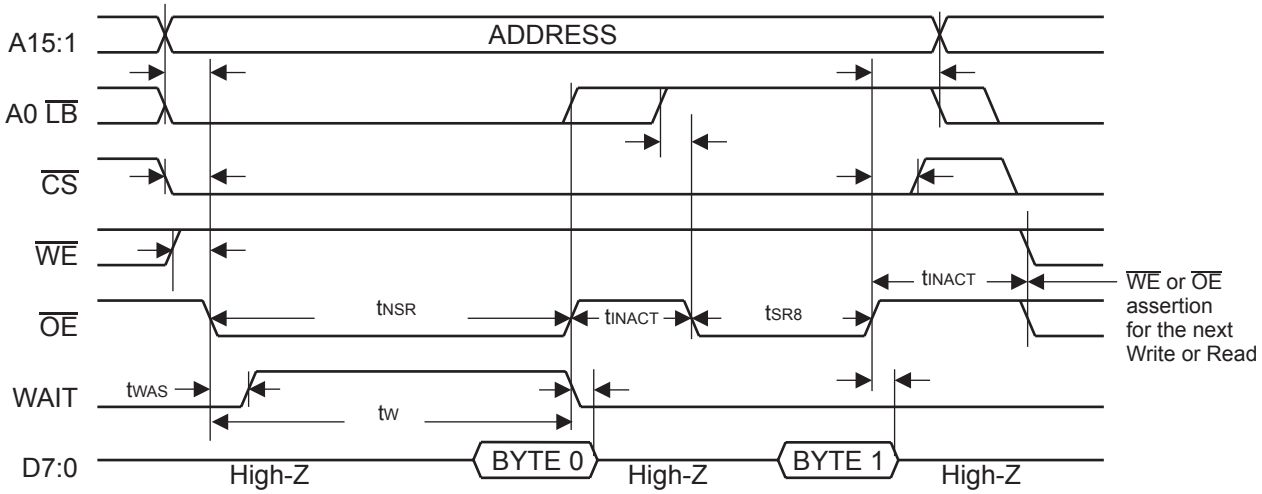
HOST READ IN DUAL-BYTE MODE (8-BIT BUS WIDTH)
using BTYPE = 1 (”Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)

showing 2 bytes read for a single 16-bit word



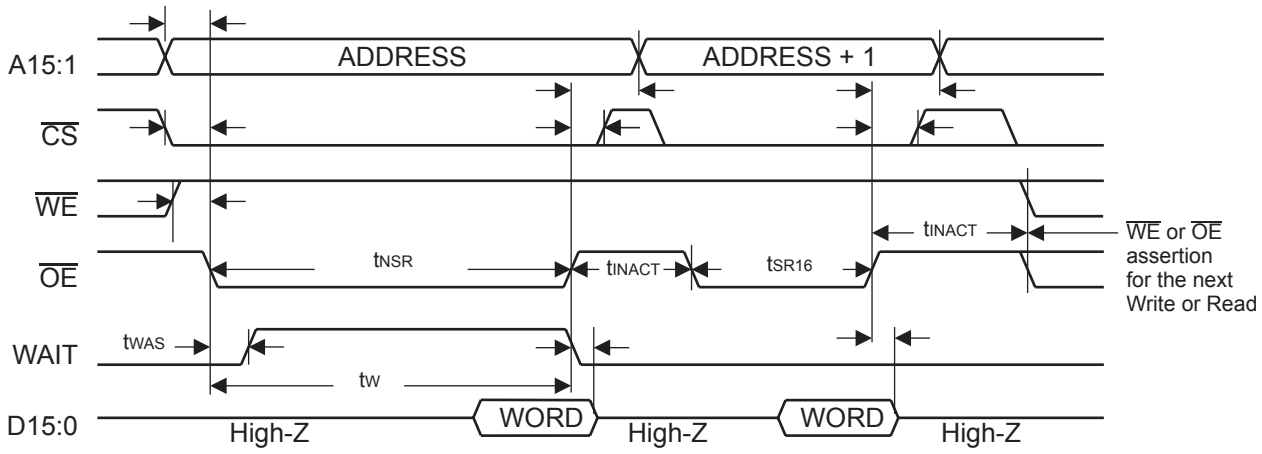
All timing intervals equal 0 ns MIN unless otherwise indicated.

After first byte is read, prefetch allows faster access times for successive reads, as long as addresses are sequential.

WAIT is always asserted during the first read cycle, is never asserted for successive read cycles to sequential adresses. This allows default host bus configuration for the HI-6120 chip select to match the timing characteristics of the faster successive cycles, while the slower initial cycle is handled on a WAIT-controlled exception basis. WAIT can be optionally inverted.

HOST READ IN WORD MODE (16-BIT BUS WIDTH)
using BTYPE = 1 (”Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)

showing two successive words read from sequential addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

After first word is read, prefetch allows faster access times for successive reads, as long as addresses are sequential.

WAIT is always asserted during the first read cycle, is never asserted for successive read cycles to sequential adresses. This allows default host bus configuration for the HI-6120 chip select to match the timing characteristics of the faster successive cycles, while the slower initial cycle is handled on a WAIT-controlled exception basis. WAIT can be optionally inverted.

Figure 32. Register and RAM Read Operations for BTYPE = 1

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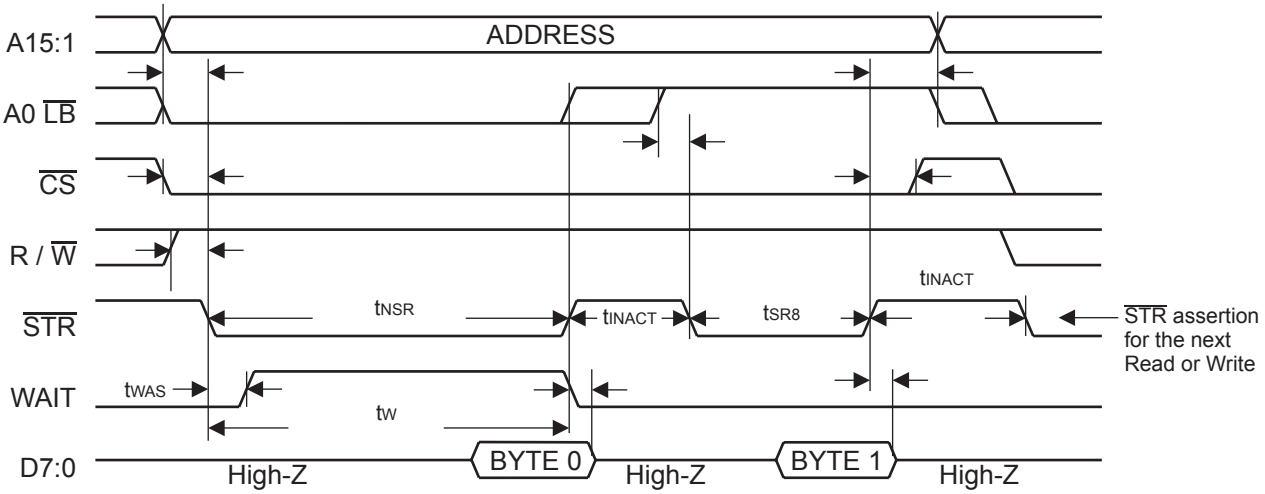
HOST READ IN DUAL-BYTE MODE (8-BIT BUS WIDTH)
using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)

showing 2 bytes read for a single 16-bit word



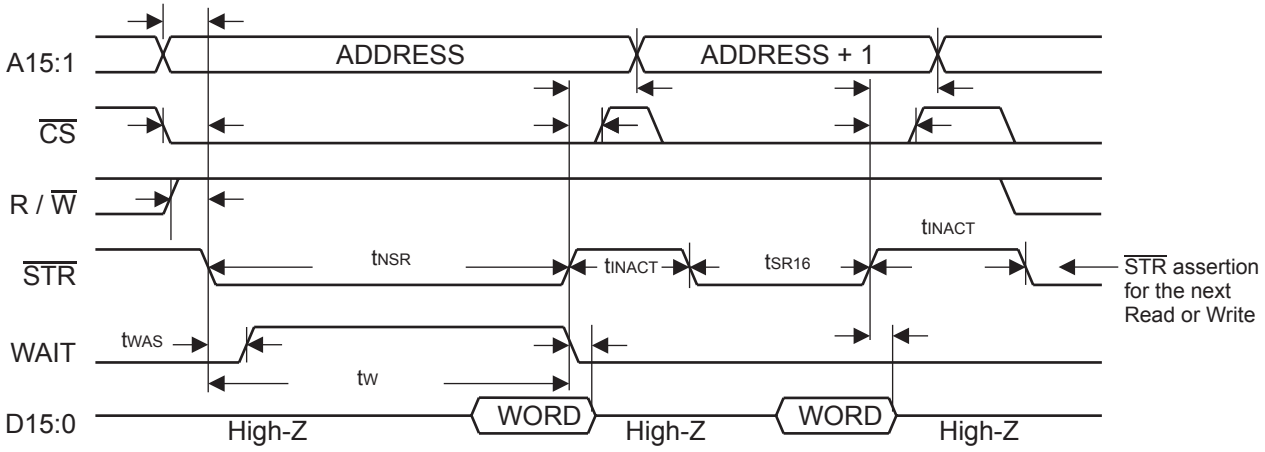
All timing intervals equal 0 ns MIN unless otherwise indicated.

After first byte is read, prefetch allows faster access times for successive reads, as long as read addresses are sequential.

WAIT is always asserted during the first read cycle, is never asserted for successive read cycles to sequential adresses. This allows default host bus configuration for the HI-6120 chip select to match the timing characteristics of the faster successive cycles, while the slower initial cycle is handled on a WAIT-controlled exception basis. WAIT can be optionally inverted.

HOST READ IN WORD MODE (16-BIT BUS WIDTH)
using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)

showing two successive words read from sequential addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

After first word is read, prefetch allows faster access times for successive reads, as long as read addresses are sequential.

WAIT is always asserted during the first read cycle, is never asserted for successive read cycles to sequential adresses. This allows default host bus configuration for the HI-6120 chip select to match the timing characteristics of the faster successive cycles, while the slower initial cycle is handled on a WAIT-controlled exception basis. WAIT can be optionally inverted.

Figure 33. Register and RAM Read Operations for BTYPE = 0

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27. MIL-STD-1553 BUS INTERFACE

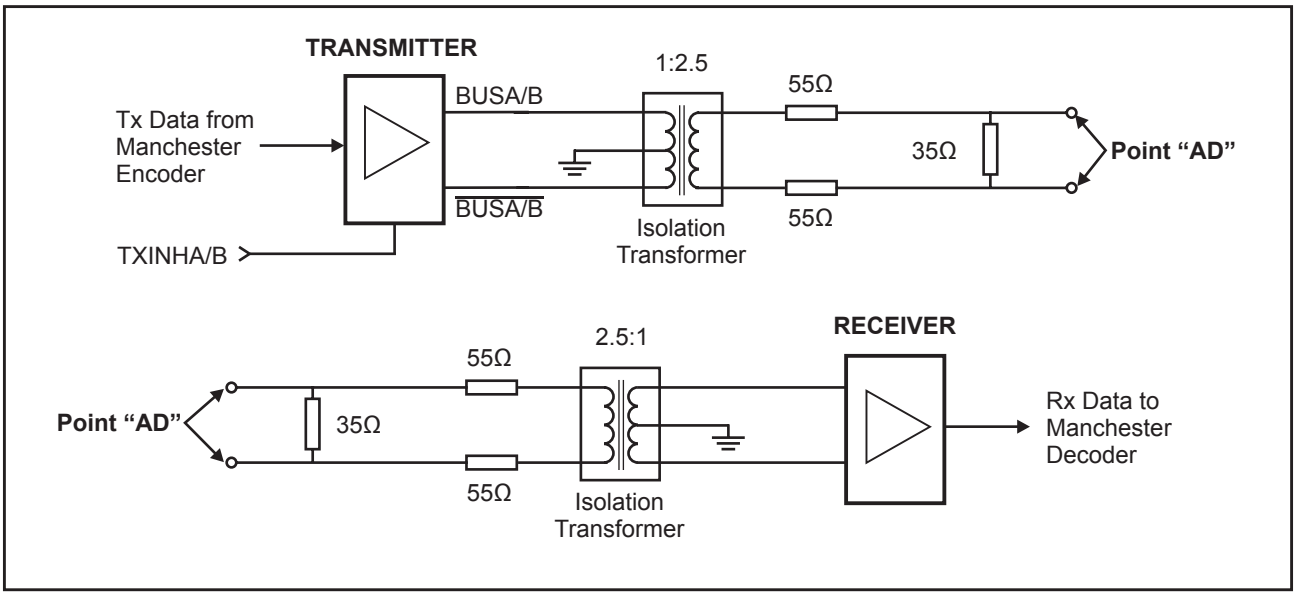

Figure 34. MIL-STD-1553 Direct Coupled Test Circuits

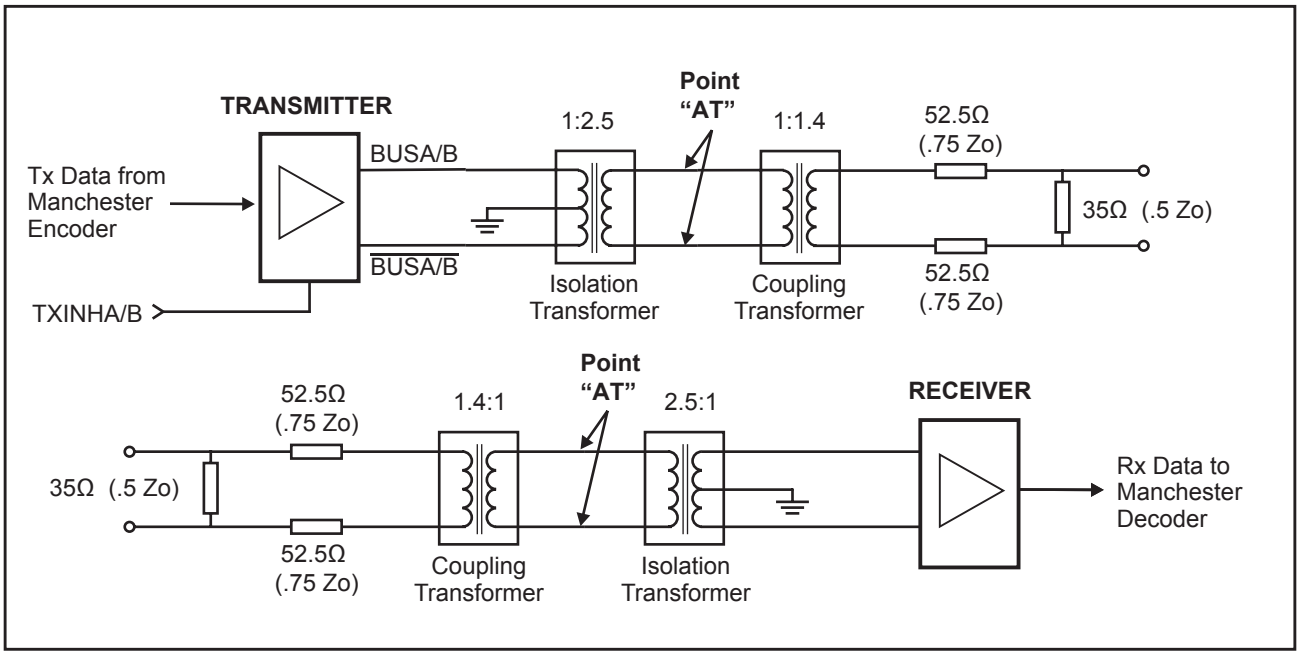

Figure 35. MIL-STD-1553 Transformer Coupled Test Circuits

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28. THERMAL CHARACTERISTICS

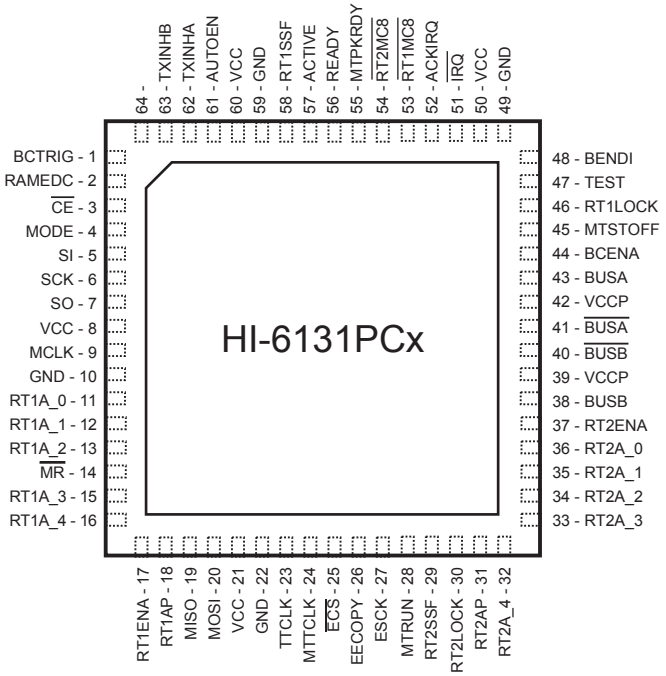
Part Number	Package Style	Condition	θ_{ja} (°C/W)	Junction Temp, T_j (°C)		
				T_A = 25°C	T_A = 85°C	T_A = 125°C
HI-6130PQx	100-pin PQFP	Mounted on circuit board	52.7	56	116	156
HI-6131PQx	64-pin PQFP	Mounted on circuit board	tbd	tbd	tbd	tbd
HI-6131PCx	64-pin QFN	Heat sink pad unsoldered	31.1	41	101	141
		Heat sink pad soldered	22.8	37	97	137

29. ADDITIONAL PIN / PACKAGE CONFIGURATIONS

Notes:

1. All VCC, VCCP and GND pins must be connected.
2. See page 1 for HI-6130, 100-Pin PQFP Package Configuration.

29.1. HI-6131PCx (64-pin QFN)



TOP VIEW

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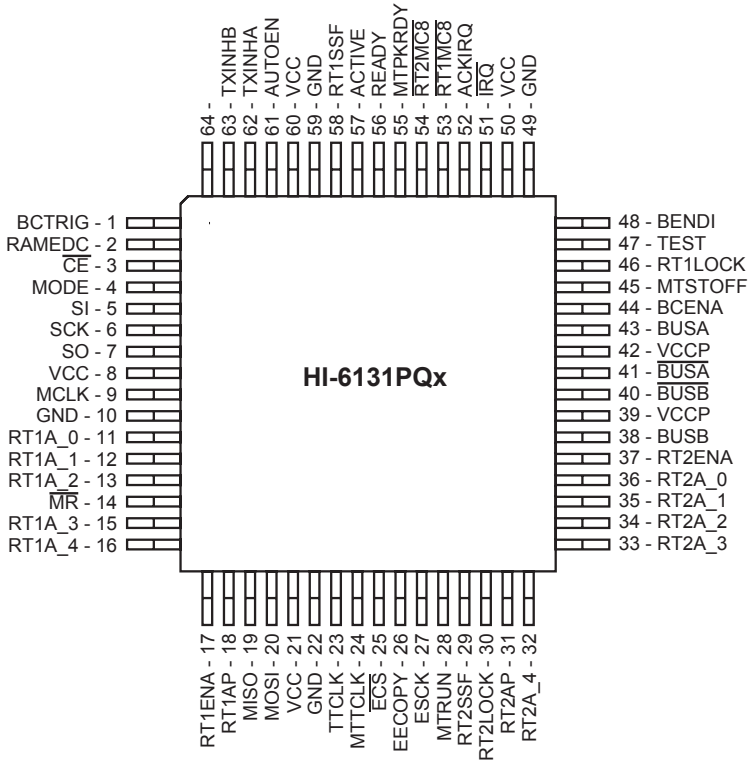
29.2. HI-6131PQx (64-pin PQFP)



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30. ORDERING INFORMATION

HI - 6130 PQ x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PQ	100 PIN PLASTIC QUAD FLAT PACK, PQFP (100PQS)

HI - 6131 Px x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PC	64 PIN PLASTIC CHIP-SCALE PACKAGE, 9 x 9mm QFN (64PCS)
PQ	64 PIN PLASTIC QUAD FLAT PACK, PQFP (64PQTS)

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31. REVISION HISTORY

Revision	Date	Description of Change
DS6130, Rev. New.	8/10/11	Initial Release

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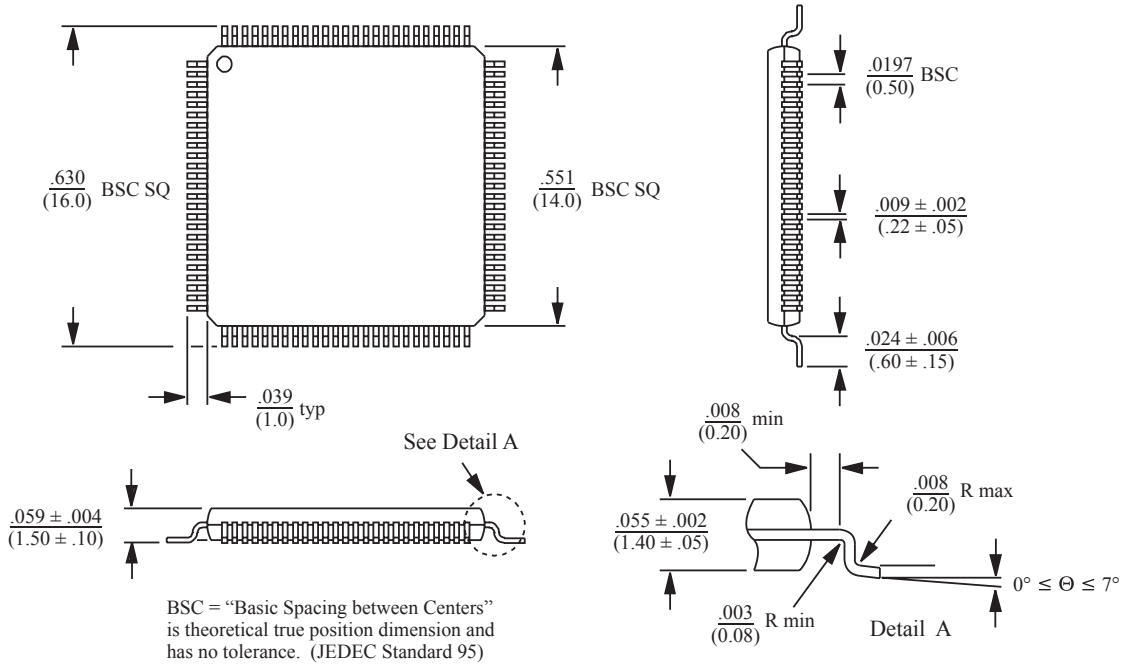
32. PACKAGE DIMENSIONS

HI-6130: 100-PIN PLASTIC QUAD FLAT PACK (PQFP)

inches (millimeters)

Package Type: 100PQS

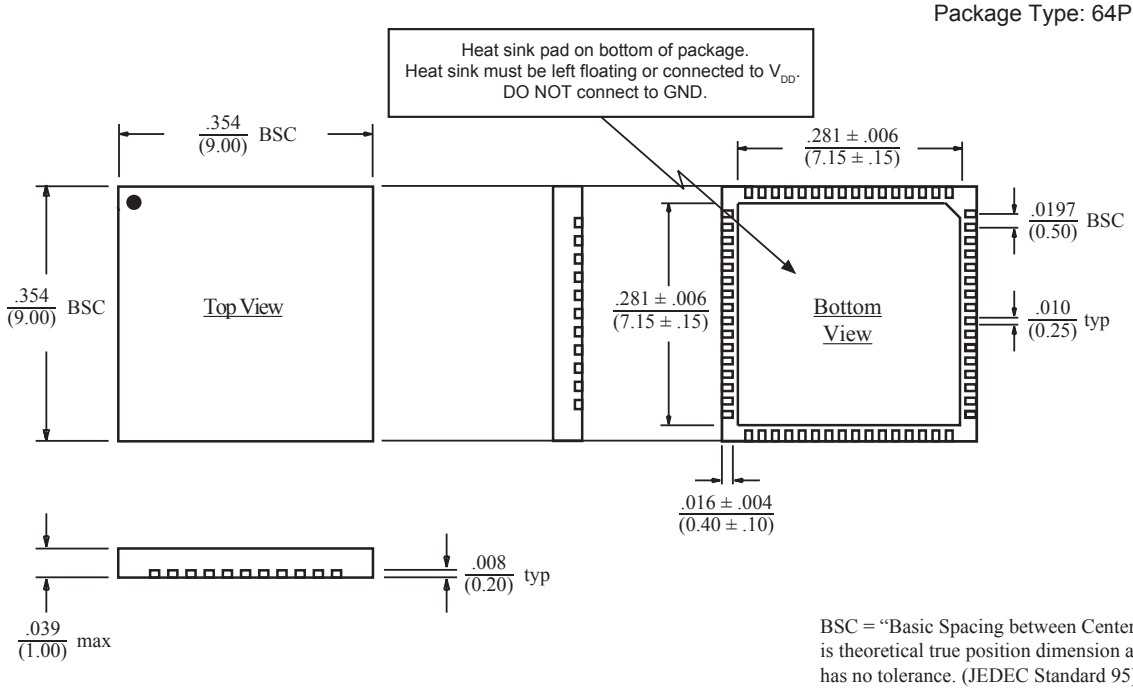


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

HI-6131: 64-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

inches (millimeters)

Package Type: 64PCS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

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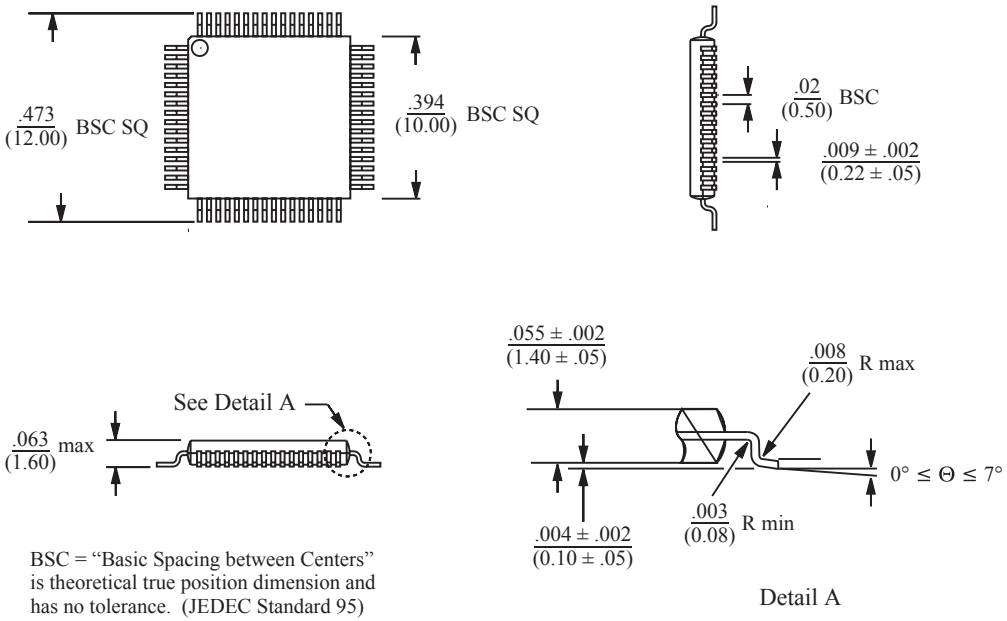
HI-6131: 64 PIN PLASTIC QUAD FLAT PACK (PQFP)

inches (millimeters)

Package Type: 64PQTS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

Detail A

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