Ordering number : ENA0989

SANYO Semiconductors
DATA SHEET

LV4920H — Bi-CMOS IC Class-D Audio Power Amplifier Power Cell BTL 15W×2CH, 10W×2CH

Overview

The LV4920H is a 2-channel BTL full-bridge driver for digital power amplifiers. It requires a PWM modulator IC in the previous stage. This IC is a power cell that takes in PWM signals as an input and is used to form a digital amplifier system for TVs, amusement equipment, and other such systems.

Application

- TV sets (PDP/LCD)
- Amusement equipment (pinball or pinball-slot-machines)
- Home audio equipment (mini-/micro-audio systems)
- Home theater equipment

Features

- BTL output, class D amplifier system
- High-efficiency class D amplifier
- Muting function reduces impulse noise at power on/off
- Full complement of built-in protection circuits: overcurrent protection, thermal protection, and low power supply voltage protection circuits
- Built-in bootstrap diodes

Specification

- Output 1=10W/ch, THD+N=10%, 8Ω Load, 1kHz, AES17, V_D=13V
- Output 2=15W/ch, THD+N=10%, 8Ω Load, 1kHz, AES17, V_D=16V
- High efficiency 85% or larger (Condition: 8Ω Load)
- THD+N<0.1% 1W/1kHz/8Ω Load (Filter: AES17)
- Package: HSOP36

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D0507 TI IM 20071022-S00006 No.A0989-1/12

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Maximum supply voltage	V_D max	Externally applied voltage			24	V
Maximum output current	I_O peak	Per channel			6	A/ch
Maximum pull-up pin voltage	Vpup max	Nch open drain terminal 16 pin, 17 pin applied voltage			20	V
Allowable power dissipation	Pd max	Mounted on a specified board*			3.95	W
Maximum junction temperature	Tj max				+150	°C
Operating temperature	Topr		-25		+75	°C
Storage temperature	Tstg		-50		+150	°C
Package thermal resistance	θjc				2.5	°C/W

* Mounted on a specified board: 80.0mm×63.0mm×1.5mm, glass epoxy (two-layer).

Recommended Operating Condtions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Recommended supply voltage	V_D	Externally applied voltage	8	13	20	V
Recommended pull-up supply voltage	Vpup	Nch open drain supply voltage		16	18	V
Recommended load resistance	R_L	Speaker load	4	8		Ω

Electrical Characteristics at Ta = 25°C, V_D = 13V, LC less filter and no load

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}	MUTEB=L		1.0	3.0	mA
Standby current	Ist	STBYB=L			1	μA
H input voltage	V_{IH}	PWM_A, PWM_B MUTEB, STBYB	2.5		5.5	V
L input voltage	V_{IL}	PWM_A, PWM_B STBYB, MUTEB	0		1.0	V
H input current	I_{IH}	V_{IN}=5.0V			20	μA
L input current	I_{IL}	V_{IN}=0V	-10			μA
Output pin leakage current	I_{OFF}	Nch open drain output OFF-stage 5.0V pull-up			1	μA
Output pin current	I_{OL}	Nch open drain output ON-stage, V_{OL}=0.4V	0.15			mA
Power Tr ON resistance *2	RdsON	I_D=1A		300		mΩ
Turn ON delay time	td ON	fin=384kHz		40	70	ns
Turn OFF delay time	td OFF	fin=384kHz		40	70	ns
Rise-up time	tr	fin=384kHz		20	40	ns
Fall time	tf	fin=384kHz		20	40	ns
Minimum output pulse range	VOPW		100			ns

*2: Design guaranteed maximum ON resistance of power Tr (RdsON): 360mΩ.

Electrical Characteristics / Operating Conditions (Reference values)

Ta = 25°C, V_D = 13V, R_L = 8Ω, filter: 20kHz AES17

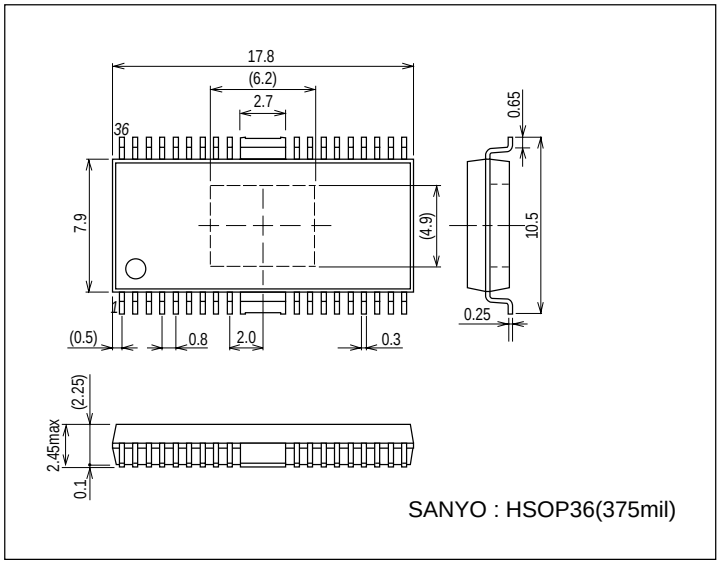
Given below are reference characteristic values of a digital amplifier system shown in the recommended application circuit (on page 10) in which the SANYO reference model of PWM modulator (BD-mode) is used.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output 1	Po1	THD+N=10%		10		W
Output 2	Po2	V_D=16V, THD+N=10%		15		W
Total harmonic distortion	THD+N@1W	Po=1W		0.1		%
Output Noise	Vno			50		μVrms
SN-ration	S/N			100		dB
Dynamic range	DNR			100		dB

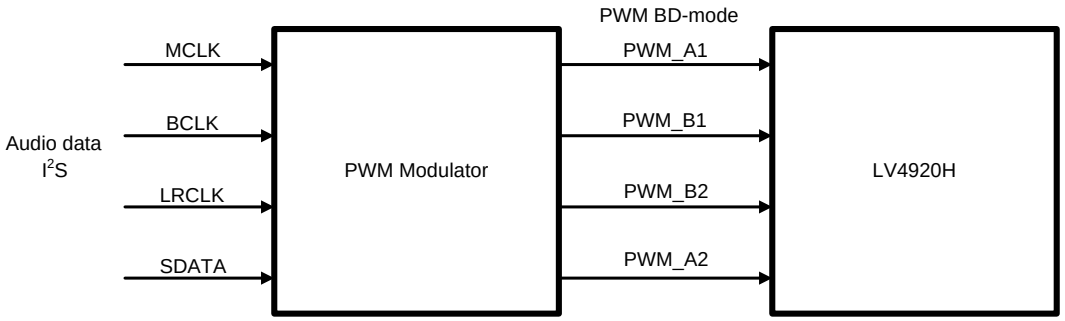
Note: The values of these characteristics were measured in SANYO test environment. The actual values in an end system will vary depending on the printed circuit board pattern, the external components actually used, and other factors.

Package Dimensions

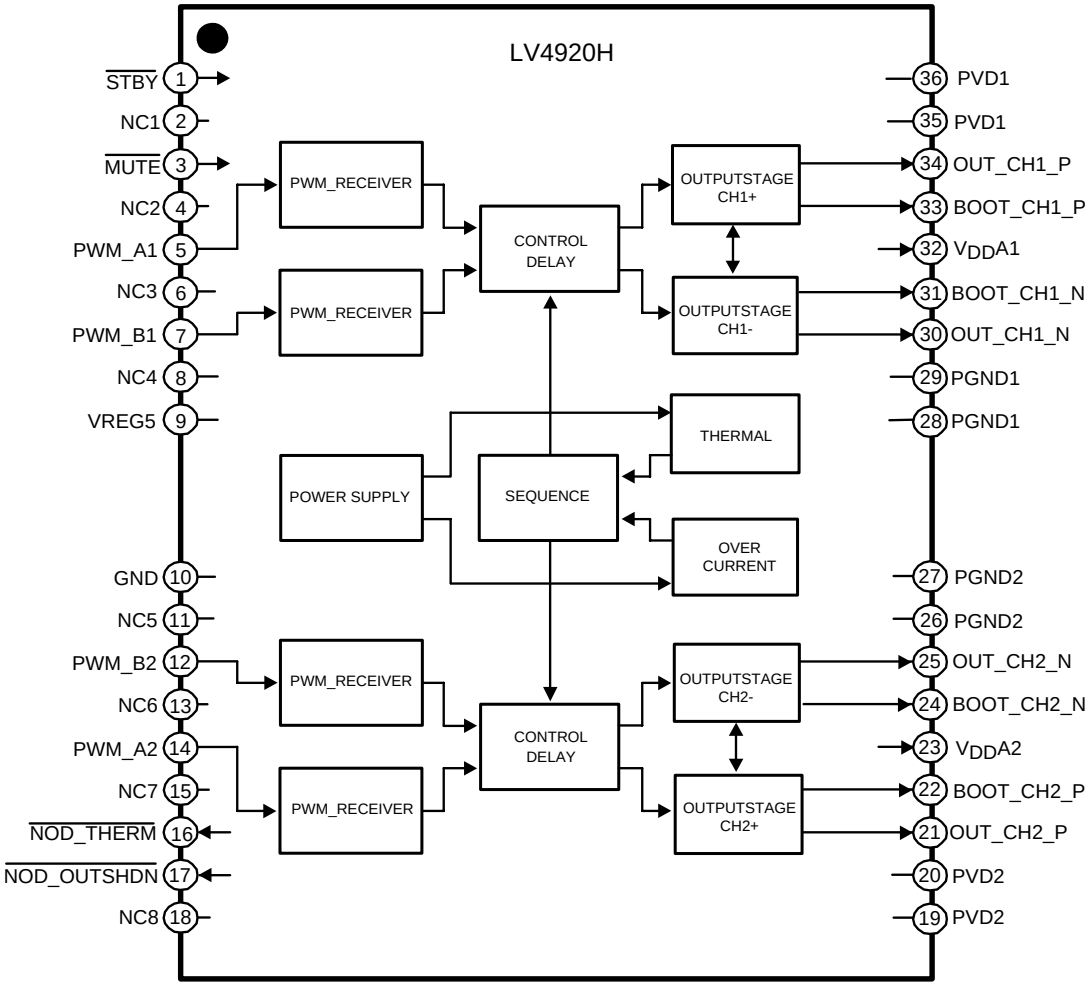
unit : mm (typ)
3235A



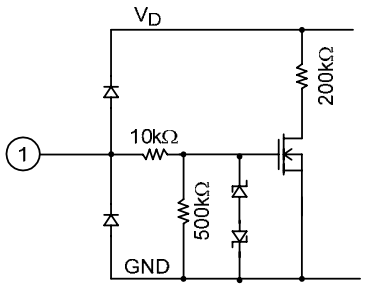
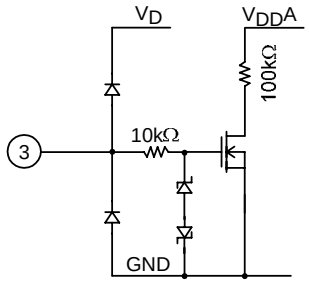
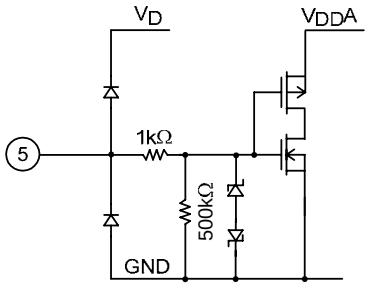
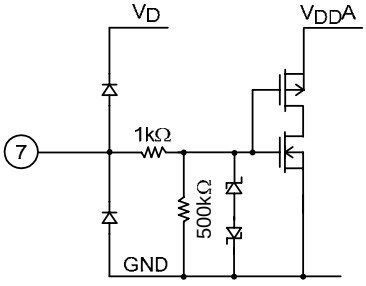
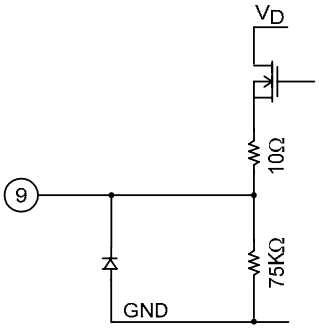
Test Circuit and Block Diagram



Block Diagram



Pin Functions

Pin No	Pin name	I/O	Pin explanation	Internal equivalent circuit
1	$\overline{\text{STBY}}$	I	Standby mode control	
2	NC1	-	Non connection	
3	$\overline{\text{MUTE}}$	I	Muting control	
4	NC2	-	Non connection	
5	PWM_A1	I	PWM input (plus input) of OUT_CH1_P	
6	NC3	-	Non connection	
7	PWM_B1	I	PWM input (negative input) of OUT_CH1_N	
8	NC4	-	Non connection	
9	VREG5	O	Smoothing capacitor connection pin for internal 5V power supply.	

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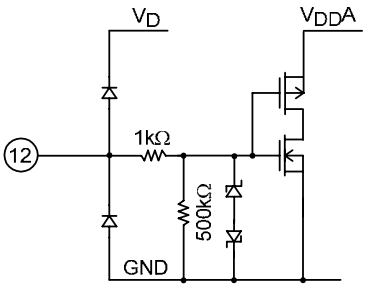
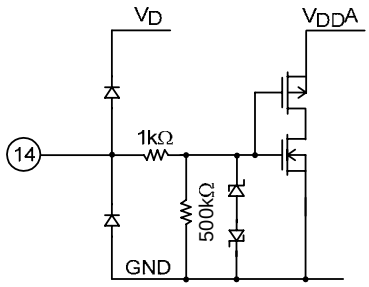
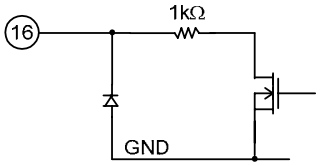
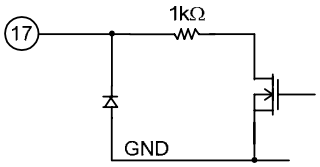
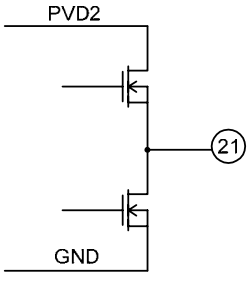
Pin No	Pin name	I/O	Pin explanation	Internal equivalent circuit
10	GND	-	Analog ground	
11	NC5	-	Non connection	
12	PWM_B2	I	PWM input (negative input) of OUT_CH2_N	
13	NC6	-	Non connection	
14	PWM_A2	I	PWM input (plus input) of OUT_CH2_P	
15	NC7	-	Non connection	
16	$\overline{\text{NOD\_THERM}}$	O	Thermal detector circuit for output (N-ch open drain)	
17	$\overline{\text{NOD\_OUTSHDN}}$	O	Output shutdown monitor output (N-ch open drain) (when thermal protection circuit is activated, when low power supply voltage protection circuit is activated, or when in mute mode)	
18	NC8	-	Non connection	
19	PVD2	-	Channel 2 power system power supply	
20	PVD2	-	Channel 2 power system power supply	
21	OUT_CH2_P	O	Channel 2 high side output	

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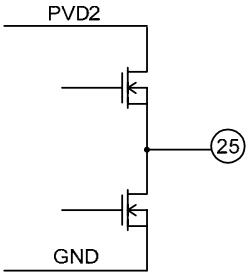
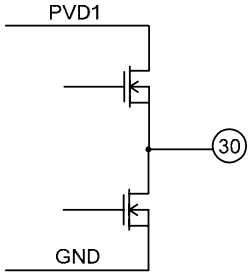
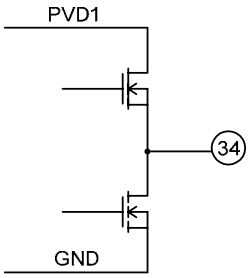
Pin No	Pin name	I/O	Pin explanation	Internal equivalent circuit
22	BOOT_CH2_P	I/O	Bootstrap I/O pin, channel 2 power supply high side	
23	$V_{DD}A2$	O	Internal power supply decoupling capacitor connection	
24	BOOT_CH2_N	I/O	Bootstrap I/O pin, channel 2 power supply low side	
25	OUT_CH2_N	O	Channel 2 low side output	
26	PGND2	-	Channel 2 power system ground	
27	PGND2	-	Channel 2 power system ground	
28	PGND1	-	Channel 1 power system ground	
29	PGND1	-	Channel 1 power system ground	
30	OUT_CH1_N	O	Channel 1 low side output	
31	BOOT_CH1_N	I/O	Bootstrap I/O pin, channel 1 power supply low side	
32	$V_{DD}A1$	O	Internal power supply decoupling capacitor connection	
33	BOOT_CH1_P	I/O	Bootstrap I/O pin, channel 1 power supply high side	
34	OUT_CH1_P	O	Channel 1 low side output	
35	PVD1	-	Channel 1 power system power supply	
36	PVD1	-	Channel 1 power system power supply	

Functional Descriptions

1. System Standby

The built-in 5V regulator is turned on and off under control of the high/low state of the STBYB pin. When the STBYB pin is low, the regulator will be turned off, and when that pin is high, the regulator will be turned on. Also, the signal initializes the internal logic of the IC. When the STBYB pin is low, the internal logic is initialized, and when the STBYB pin is high, the IC is put into normal operation.

2. Mute Function

The mute function is provided mainly to mute the output so that impulse noise will not appear in the output when the power supply is being turned on.

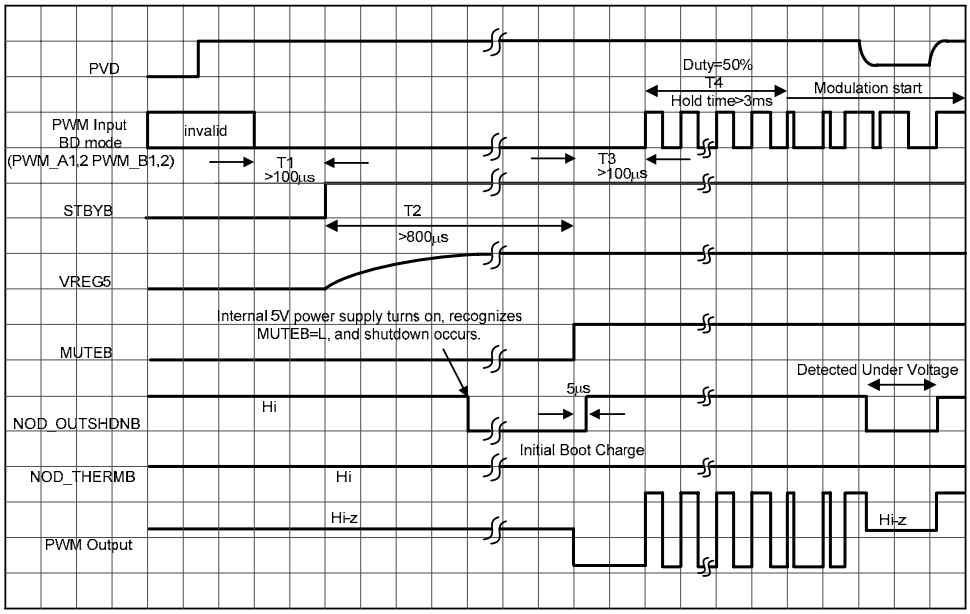
2.1 Output muting

The PWM output signal can be turned on or off by setting the MUTEB pin high or low. When the MUTEB pin is low, the PWM output is stopped (all PWM output signals are set in the high-impedance state) and when the MUTEB pin is high, the IC is placed in normal operation mode. Also the NOD_OUTSHDNB (Nch open drain) signal is output for an external monitor pin.

2.2 Power-on sequence

The power-on sequence must be controlled by timing as shown below (PWM=BD mode) to minimize impulse noise.

Note that when MUTE is released, all PWM input signals must be held low.

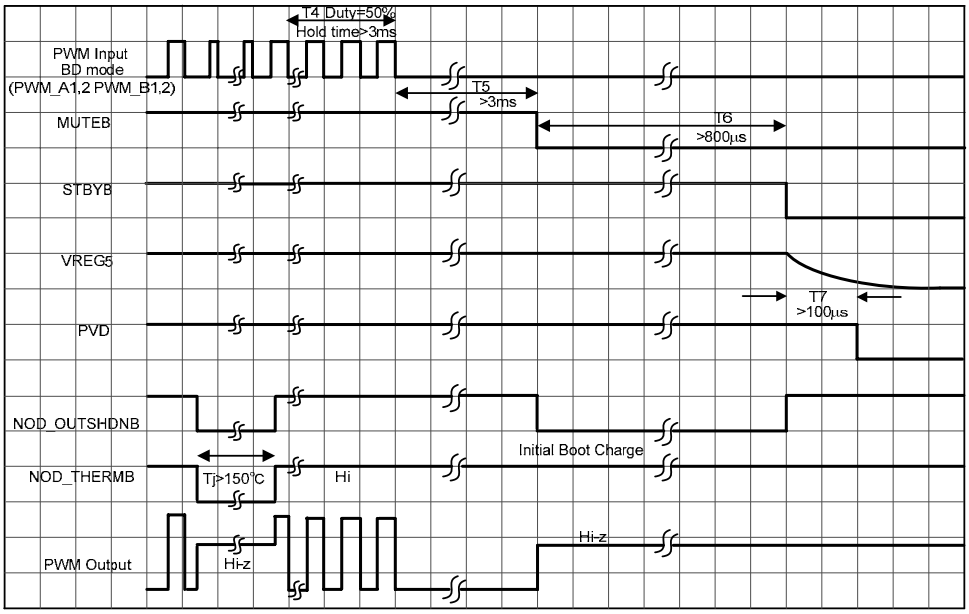


The NOD_OUTSHDNB (Nch open drain) output signal is generated (Nch open drain output is turned on) when output is shut down (except when the overcurrent protection circuit is activated). This operating condition is established when either one of the following conditions occurs:

(1) Thermal shutdown circuit is activated.
(2) Low power voltage protection circuit is activated.
(3) MUTEB set low (all outputs muted)

2.3 Power Down Sequence

The power shut-down sequence must be controlled by timing as shown below (PWM=BD mode) to minimize impulse noise.



3. Protection Circuits

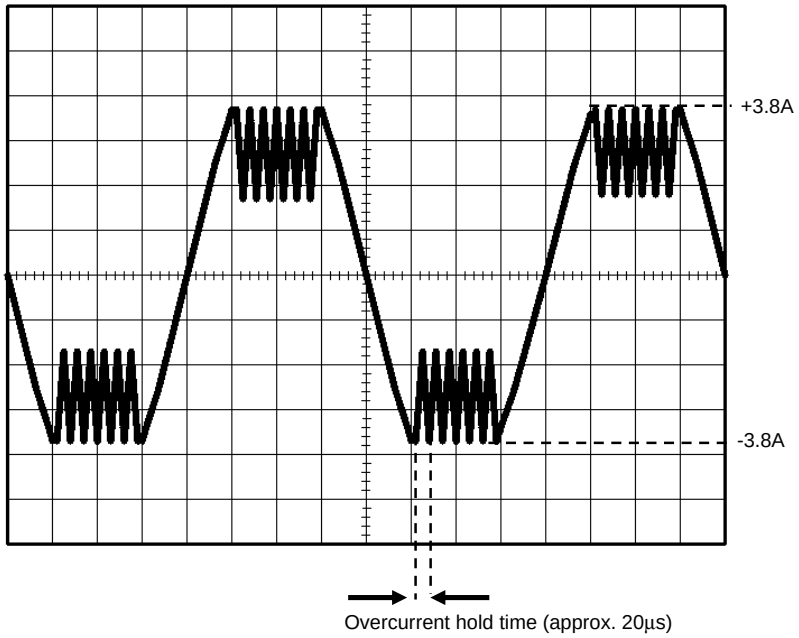
The LV4920H has full complement of built-in protection circuits: overcurrent protection, thermal protection, and low power supply voltage protection circuits.

3.1 Overcurrent protection circuit

The overcurrent protection circuit protects the output transistors by detecting current that exceeds a predetermined value due to load shorting, shorting to power, shorting to ground, etc.

When the protection circuit is activated, both the high- and low-side output transistors are turned off and the output is placed in a high-impedance state.

The figure below shows the waveform of current that flows when load shorting (1Ω) occurs.



3.2 Thermal protection circuit

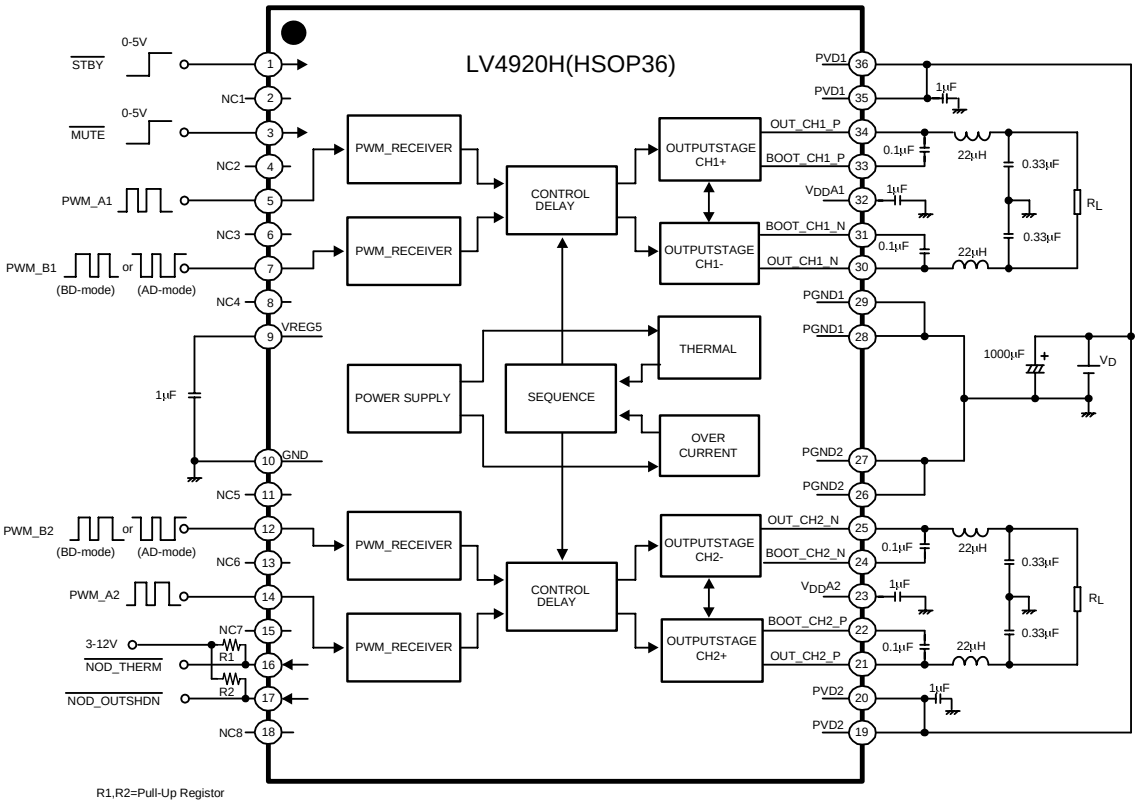
The thermal protection circuit detects the temperature (150°C or higher) inside the IC and protects the IC from thermal damage. When the protection circuit is activated, both the high- and low-side output transistors are turned off, placing the output into the high-impedance state. This protective operation is given a hysteresis. Also, NOD_OUTSHDNB (Nch open drain) signal is output for an external monitor pin.

3.3 Low power supply voltage protection circuit

The low power supply voltage protection circuit turns off both of the high- and low-side output transistors to place the output into the high-impedance state when the power supply voltage (PVD) falls below a predetermined value (6.7V or lower). This operation (activating the protective circuit when V_D rises beyond 7.5V) is given a hysteresis (0.8V or greater).

Also, NOD_OUTSHDNB (Nch open drain) signal is output for an external monitor pin.

Application Circuit Example



* $\overline{\text{NOD\_THERM}}$ at pin 16 and $\overline{\text{NOD\_OUTSHDN}}$ at pin 17 are outputs of N-ch open-drain type. When CPU or other device monitors these outputs, it is necessary to connect pull-up resistors to a power supply for the CPU and other device. The pull-up resistors are not required if they are not to be used (not monitored).

Characteristic Data