



SANYO Semiconductors

DATA SHEET

LV4900H — Bi-CMOS LSI Class-D Audio Power Amplifier BTL 10W×2ch

Overview

The LV4900H is a 10W per channel stereo digital power amplifier that takes analog inputs. The LV4900H uses unique SANYO-developed feedback technology to achieve excellent audio quality despite being a class D amplifier and can be used to implement high quality flat display panel (FDP) based systems.

Features

- Supports circuit designs that do not require output LC filters
- BTL output, class D amplifier system
- Unique SANYO-developed feedback technology achieves superb audio quality
- High-efficiency class D amplifier
- Soft muting function reduces impulse noise at power on/off
- Full complement of built-in protection circuits : overcurrent protection, thermal protection, and low power supply voltage protection circuits
- Built-in bootstrap diodes
- Internal oscillator frequencies : channel 1 = 325kHz, channel 2 = 300kHz

Functions

- 10W output (At $V_D = 12V$, $R_L = 8\Omega$, $THD + N = 10\%$)
- 15W output (At $V_D = 12V$, $R_L = 4\Omega$, $THD + N = 10\%$)
- Efficiency : 88% ($V_D = 12V$, $R_L = 8\Omega$, $f_{in} = 1kHz$, $P_O = 10W$)
- Low THD + N : 0.15% ($V_D = 12V$, $R_L = 8\Omega$, $f_{in} = 1kHz$, $P_O = 1W$, Filter : AES17)
- Noise : 100 μ Vrms (Filter : A-weight)

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LV4900H

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|------------|----------------------------|-------------|------------------|
| Maximum supply voltage | VD | Externally applied voltage | 15 | V |
| Maximum output current | I_O peak | | 3.75 | A/ch |
| Allowable power dissipation | P_d max | Independent package | 886 | mW |
| Operating temperature | T_{opr} | | -25 to +75 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -50 to +150 | $^\circ\text{C}$ |

Operating Conditions at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|----------------------------------|--------|----------------------------|---------|-----|-----|----------|
| | | | min | typ | max | |
| Recommended supply voltage range | VD | Externally applied voltage | 10 | 12 | 14 | V |
| Recommended load resistance | R_L | Speaker load | 4 | 8 | | Ω |

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_D = 12\text{V}$, $R_L = 8\Omega$, $L = 22\mu\text{H}$, $C = 0.33\mu\text{F}$

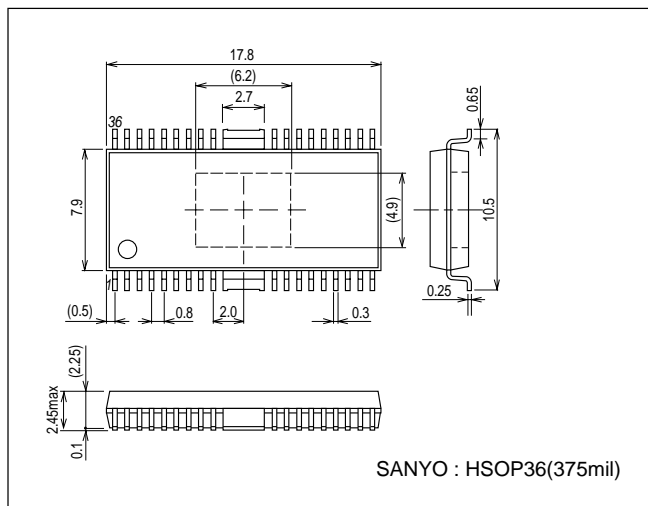
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|---------------|---|---------|------|-----|------------------|
| | | | min | typ | max | |
| Standby current | I_{st} | STBY = L, MUTE = L | | 13 | 25 | μA |
| Muting current | I_{mute} | STBY = H, MUTE = L | | 13.5 | 20 | mA |
| Quiescent current | I_{CCO} | STBY = H, MUTE = H | | 60 | 70 | mA |
| Voltage gain | VG | $f_{in} = 1\text{kHz}$, $V_O = 0\text{dBm}$ | 27 | 29 | 31 | dB |
| Output offset voltage | V_{offset} | $R_g = 0$ | -150 | | 150 | mV |
| Total harmonic distortion | THD@1W | $P_O = 1\text{W}$, $f_{in} = 1\text{kHz}$, AES17 | | 0.15 | 0.5 | % |
| Maximum output | $P_{O1@10\%}$ | THD+N = 10%, AES17 | 8 | 10 | | W |
| Channel separation | CH sep. | $R_g = 0$, $V_O = 0\text{dBm}$, DIN AUDIO | 55 | 70 | | dB |
| Ripple rejection ratio | SVRR | $f_r = 100\text{Hz}$, $V_r = 0\text{dBm}$, $R_g = 0$, A-weight | 50 | 65 | | dB |
| Noise | V_{NO} | $R_g = 0$, A-weight | | 100 | 300 | μVrms |
| High-level input voltage | V_{IH} | STBY pin and MUTE pin | 3 | | | V |
| Low-level input voltage | V_{IL} | STBY pin and MUTE pin | | | 1 | V |
| Power supply voltage drop protection circuit upper limit value | UV_UPPER | VD pin voltage monitor | | 8.0 | | V |
| Power supply voltage drop protection circuit lower limit value | UV_LOWER | VD pin voltage monitor | | 7.0 | | V |

Note : The values of these characteristics were measured in the SANYO test environment. The actual values in an end system will vary depending on the printed circuit board pattern, the external components actually used, and other factors.

Package Dimensions

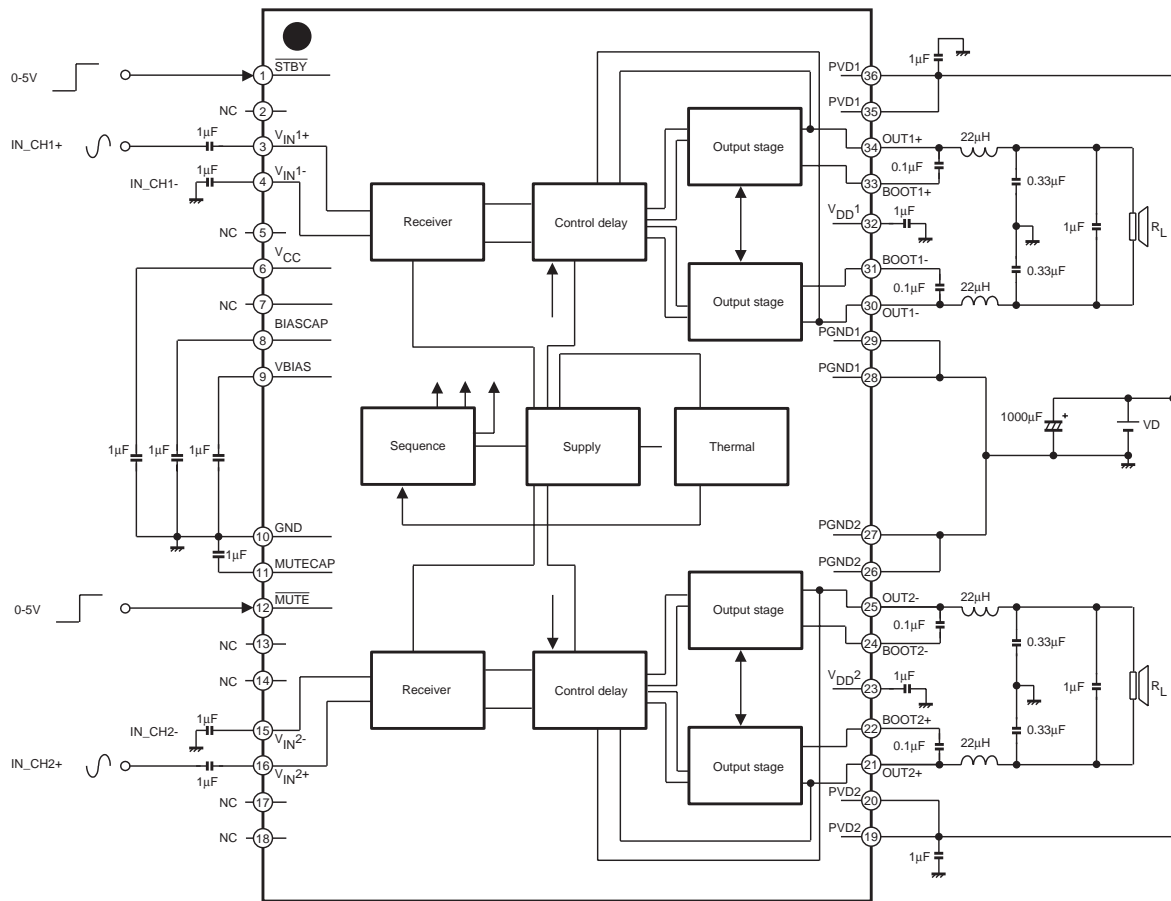
unit : mm (typ)

3235A



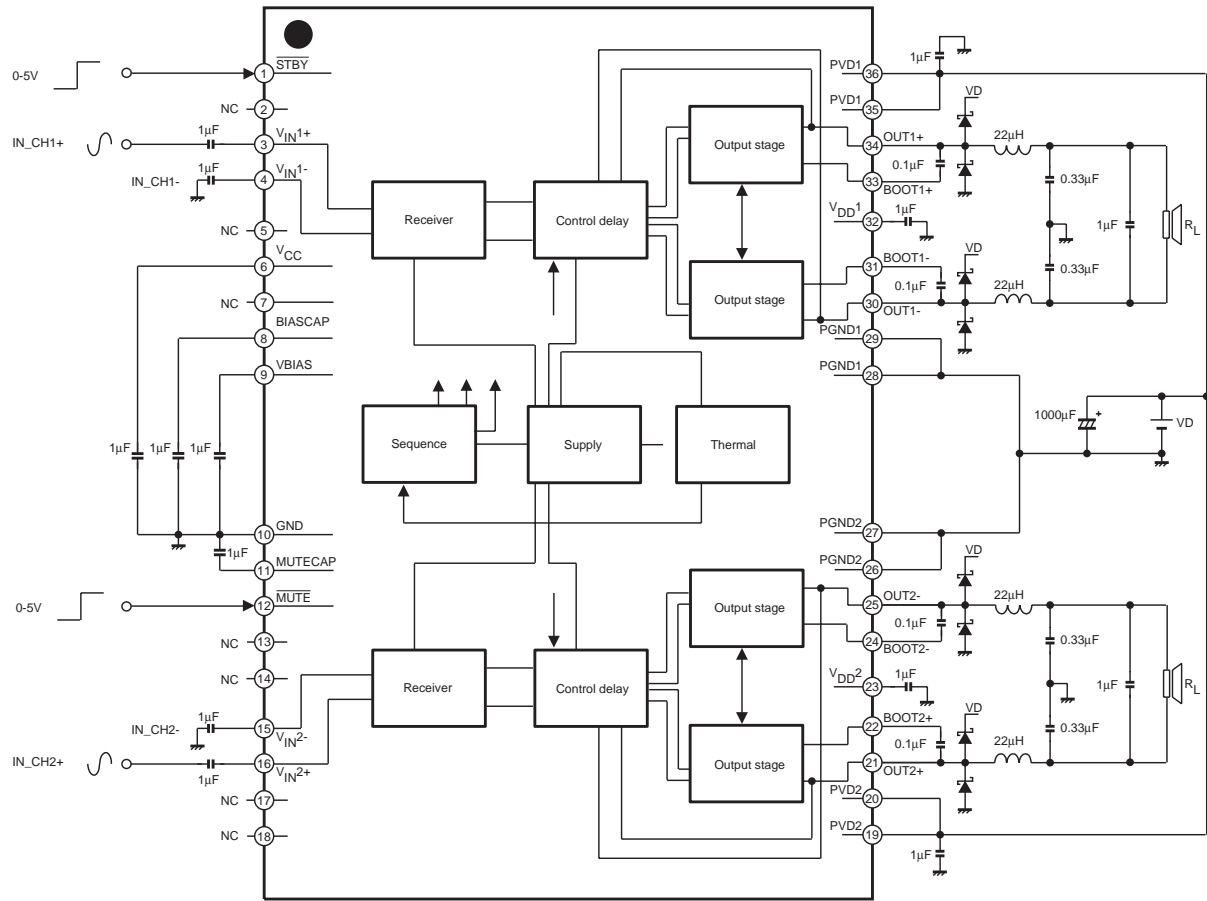
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Block Diagram and Application Circuit Example 1 ($R_L = 8\Omega$)



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Application Circuit Example 2 ($R_L = 4\Omega$)



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Pin Equivalent Circuit

| Pin No. | Pin | I/O | Description | Equivalent Circuit |
|---------|-------------------|-----|---|--------------------|
| 1 | STBY | I | Standby mode control | |
| 2 | NC | | No connection | |
| 3 | V _{IN1+} | I | Channel 1 noninverting input | |
| 4 | V _{IN1-} | I | Channel 1 inverting input | |
| 5 | NC | | No connection | |
| 6 | V _{CC} | O | Internal power supply decoupling capacitor connection | |
| 7 | NC | | No connection | |
| 8 | BIASCAP | O | Internal power supply decoupling capacitor connection | |

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| Pin No. | Pin | I/O | Description | Equivalent Circuit |
|---------|-------------------|-----|---|--------------------|
| 9 | VBIAS | O | Internal power supply decoupling capacitor connection | |
| 10 | GND | | Analog system ground | |
| 11 | MUTECAP | O | Muting system capacitor connection | |
| 12 | MUTE | I | Muting control | |
| 13 | NC | | No connection | |
| 14 | NC | | No connection | |
| 15 | V _{IN2-} | I | Channel 2 inverting input | |
| 16 | V _{IN2+} | I | Channel 2 noninverting input | |
| 17 | NC | | No connection | |
| 18 | NC | | No connection | |
| 19 | PVD2 | | Channel 2 power system power supply | |
| 20 | PVD2 | | Channel 2 power system power supply | |

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| Pin No. | Pin | I/O | Description | Equivalent Circuit |
|---------|------------------|-----|---|--------------------|
| 21 | OUT2+ | O | Channel 2 high side output | |
| 22 | BOOT2+ | I/O | Bootstrap I/O pin, channel 2 power supply high side | |
| 23 | V _{DD2} | O | Internal power supply decoupling capacitor connection | |
| 24 | BOOT2- | I/O | Bootstrap I/O pin, channel 2 power supply low side | |
| 25 | OUT2- | O | Channel 2 low side output | |
| 26 | PGND2 | | Channel 2 power system ground | |
| 27 | PGND2 | | Channel 2 power system ground | |
| 28 | PGND1 | | Channel 1 power system ground | |
| 29 | PGND1 | | Channel 1 power system ground | |
| 30 | OUT1- | O | Channel 1 low side output | |
| 31 | BOOT1- | I/O | Bootstrap I/O pin, channel 1 power supply low side | |

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| Pin No. | Pin | I/O | Description | Equivalent Circuit |
|---------|------------------|-----|---|--------------------|
| 32 | V _{DD1} | O | Internal power supply decoupling capacitor connection | |
| 33 | BOOT1+ | I/O | Bootstrap I/O pin, channel 1 power supply high side | |
| 34 | OUT1+ | O | Channel 1 high side output | |
| 35 | PVD1 | | Channel 1 power system power supply | |
| 36 | PVD1 | | Channel 1 power system power supply | |

Note : Smoothing capacitors must be connected to each power supply pin.

Functional Descriptions

System Standby

The bias levels are turned on and off under control of the high/low state of the STBY pin. When the STBY pin is low, the bias levels will be turned off, and when that pin is high, the bias levels will be applied.

Mute Function

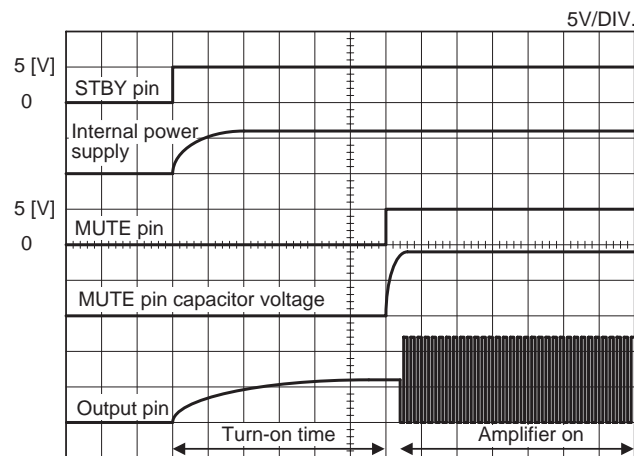
The mute function is provided mainly to mute the output so that impulse noise will not appear in the output when the power supply is being turned on.

(1) Output Muting

The output PWM signal can be turned on or off by setting the MUTE pin high or low. When the MUTE pin is low, the internal oscillator is stopped. This oscillator operates at all times that the MUTE pin is high.

(2) Power On Sequence

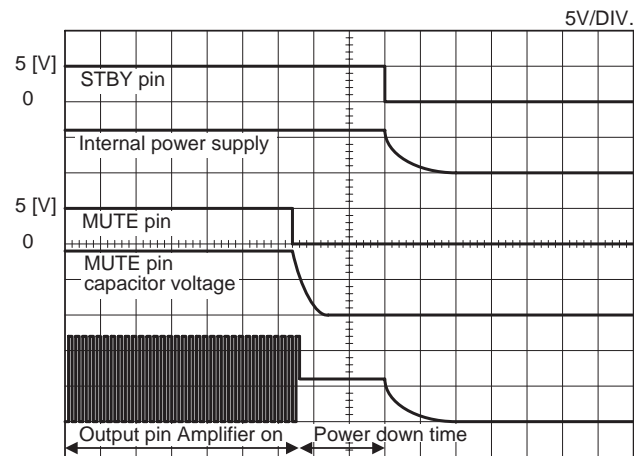
Applications should provide a power-on muting period of at least 500ms to minimize impulse noise.



Turn-on time : the time between the point the STBY pin is set high and the point the MUTE pin is set high.

(3) Power Down Sequence

Applications should provide a power down muting period of at least 100ms to minimize impulse noise.

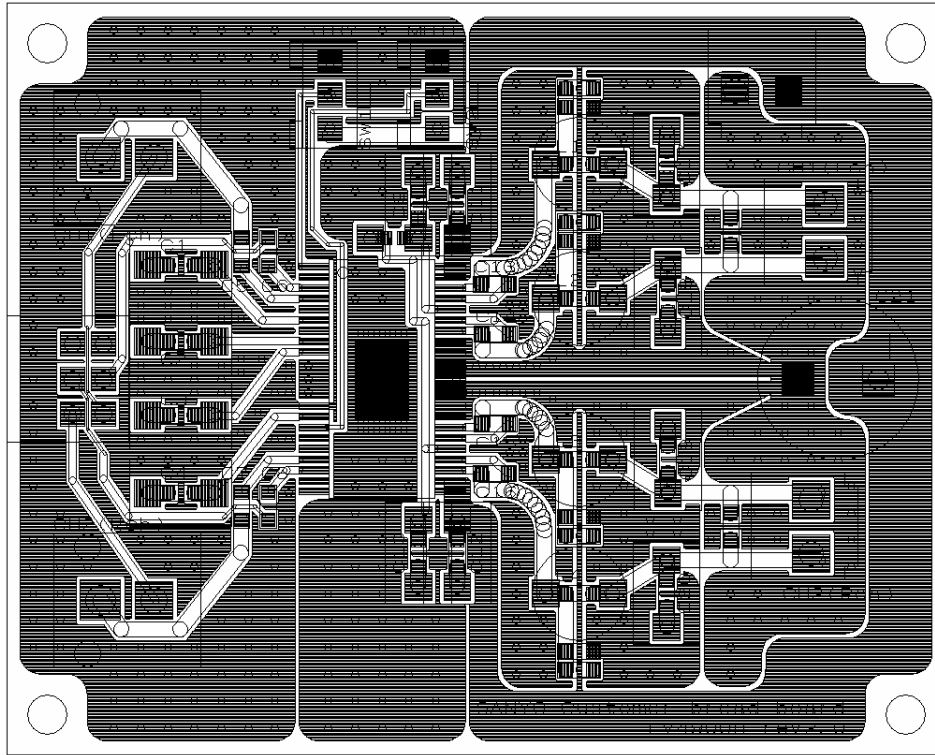


Turn-off time : the time between the point the MUTE pin is set low and the point the STBY pin is set low.

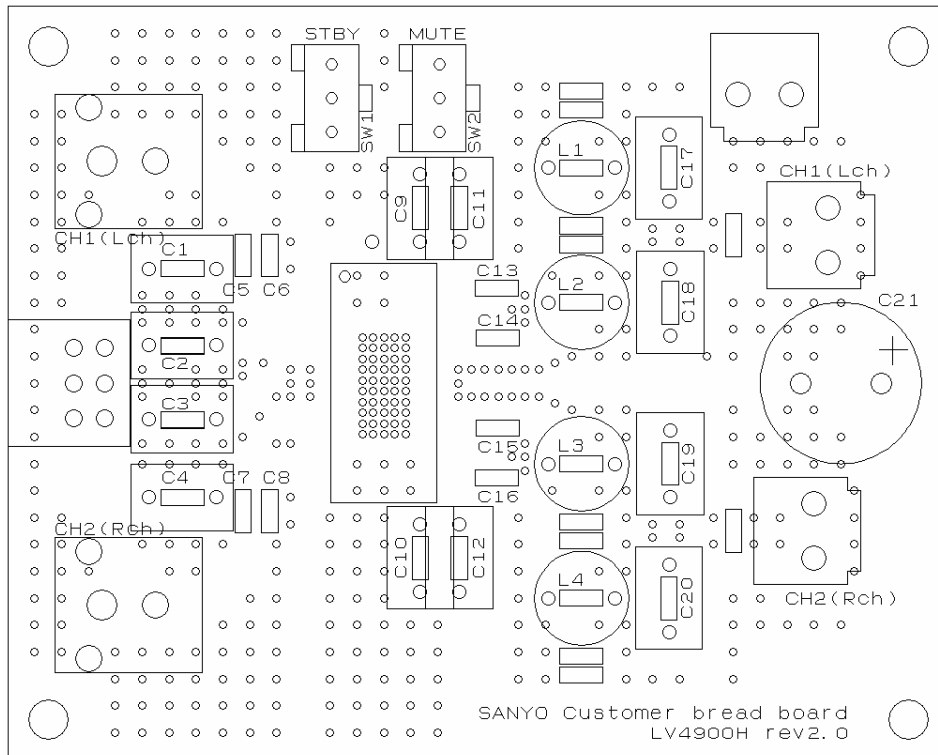
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LV4900H customer bread board rev.2.0

Pattern



Silk

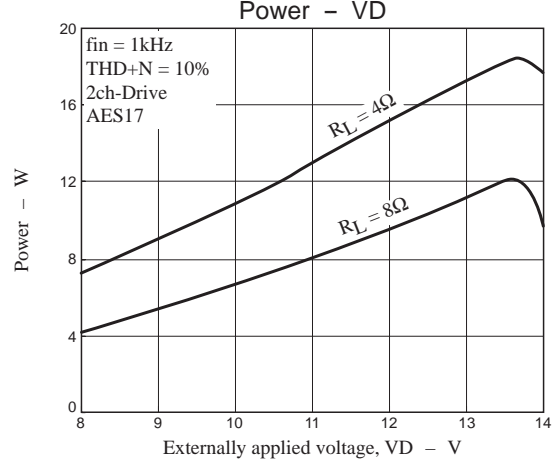
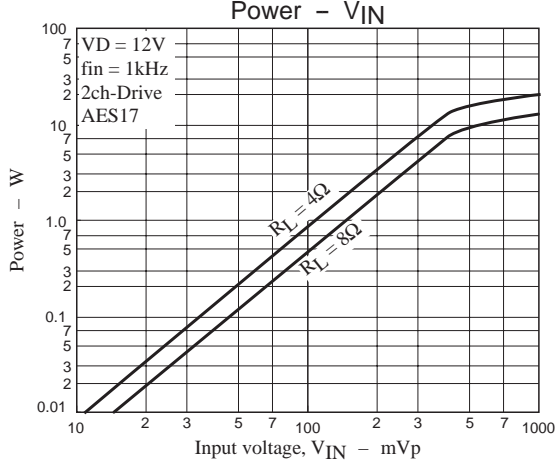
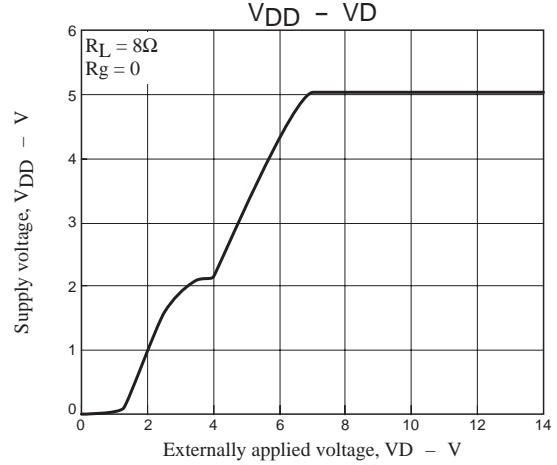
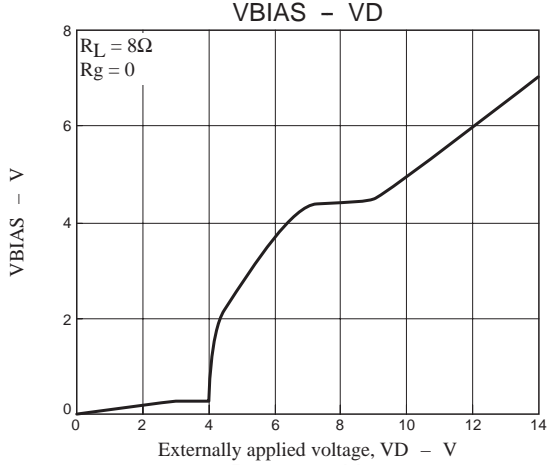
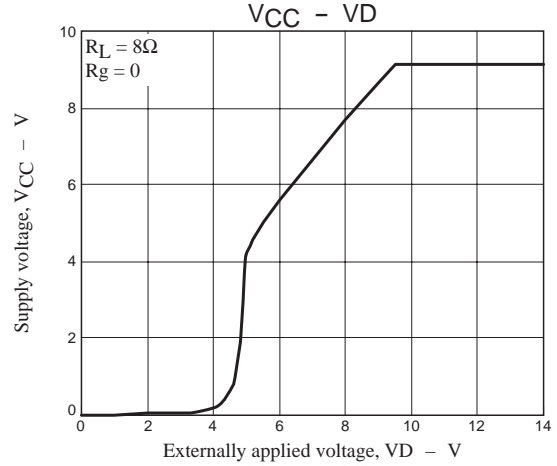
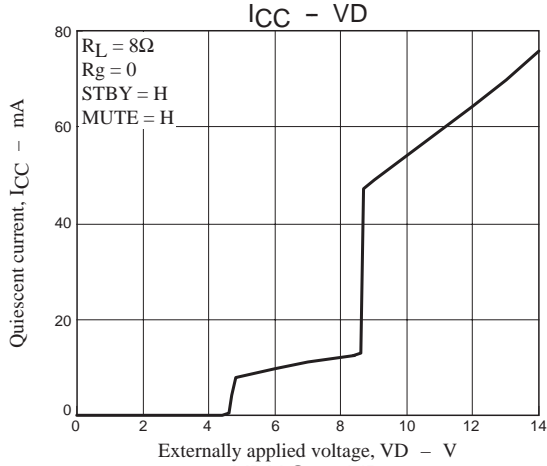
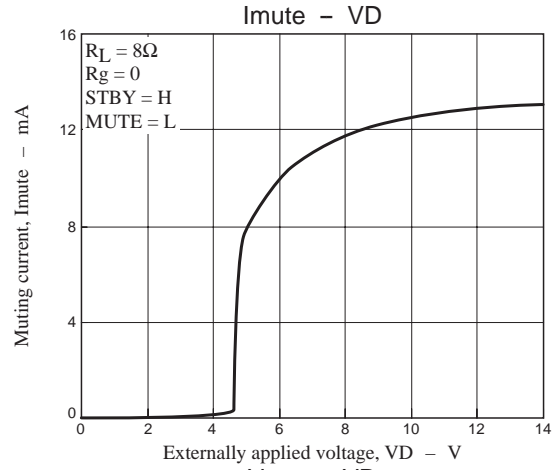
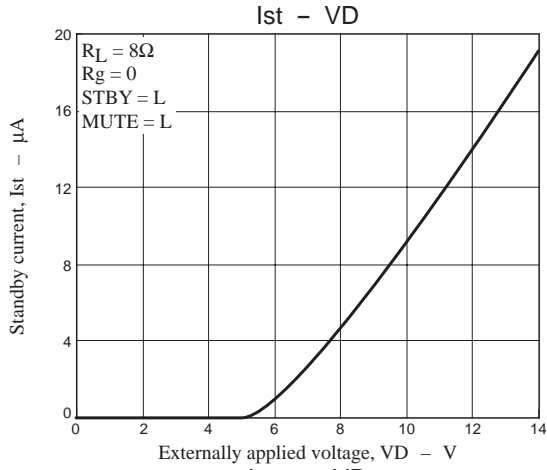


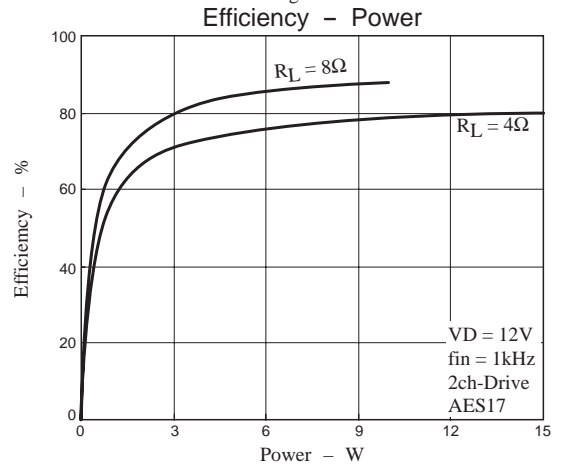
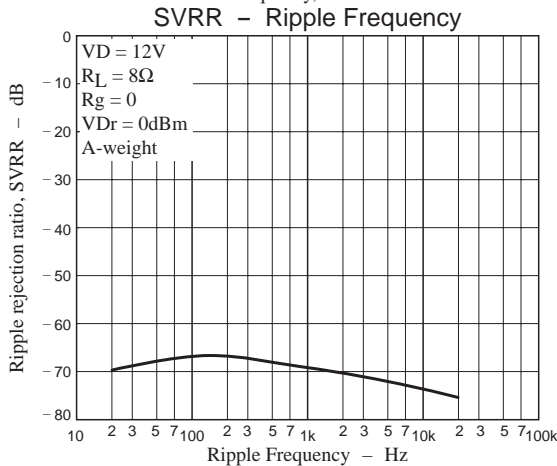
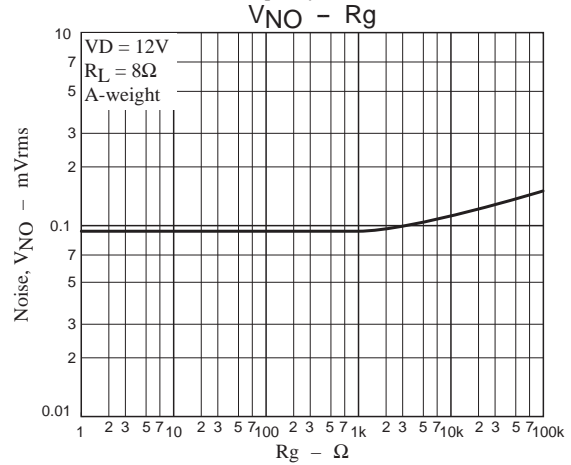
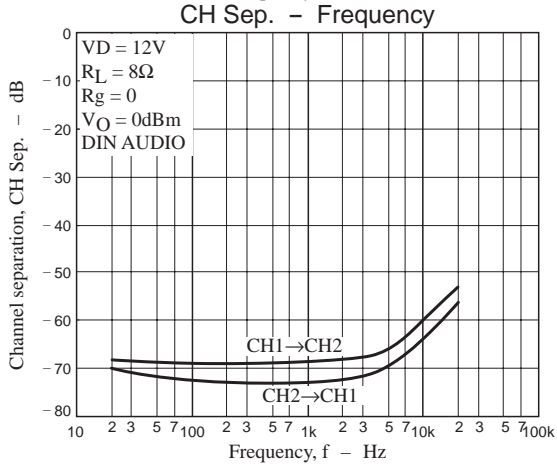
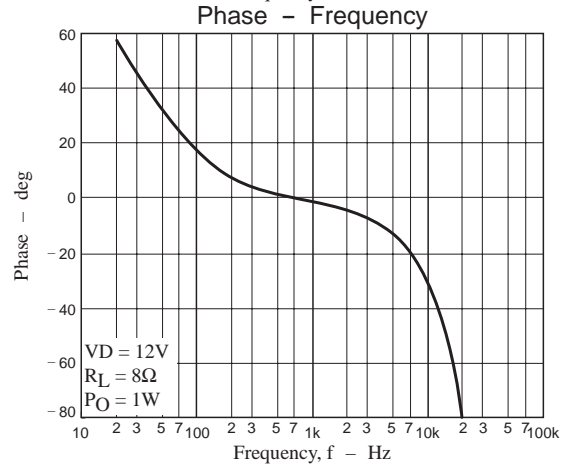
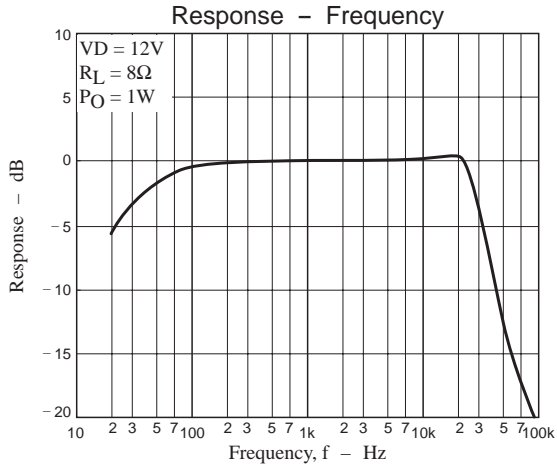
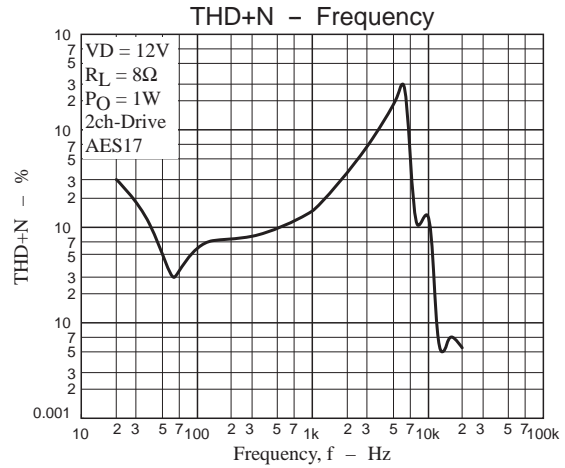
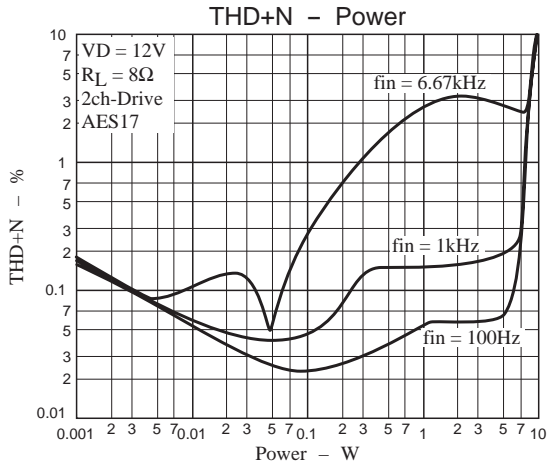
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Components

| Symbol | Part No. | Function |
|----------------------|--------------------|--|
| ----- | SW1 | Standby switch. Lower position: standby state |
| ----- | SW2 | Mute switch. Lower position: mute state |
| C _{VCC} | C1 | Internal power supply (V _{CC}) output coupling capacitor |
| C _{BIASCAP} | C2 | Internal power supply (V _{BIAS}) input coupling capacitor |
| C _{VBIAS} | C3 | Internal power supply (V _{BIAS}) output coupling capacitor |
| C _{MUTE} | C4 | Soft muting time constant adjustment capacitor |
| C _{IN} | C5, C6, C7, C8 | Input capacitors |
| * C _{VDD} | C9, C10 | Internal power supply (V _{DD}) output coupling capacitors |
| * C _{VD} | C11, C12 | VD high-frequency attenuation capacitors |
| * C _{BOOT} | C13, C14, C15, C16 | Bootstrap capacitor |
| L _O | L1, L2, L3, L4 | Output low-pass filter coils: $f_c = 1 / (2\pi\sqrt{L_oC_o})$ |
| C _O | C17, C18, C19, C20 | Output low-pass filter capacitors |
| C _{VD} | C21 | VD power supply capacitors |

* C_{VDD}, C_{VD} and C_{BOOT}, Each capacitor is arranged in the neighborhood of IC as much as possible.





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