OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

MSM5265

80-DOT LCD DRIVER

GENERAL DESCRIPTION

The MSM5265 is an LCD driver which can directly drive up to 80 segments in the static display mode and up to 160 segments in the 1/2 duty dynamic display mode.

The MSM5265 is fabricated with low power CMOS metal gate technology. The MSM5265 consists of a 160-stage shift register, 160-bit data latch, 80 pairs of LCD drivers and a common signal generator.

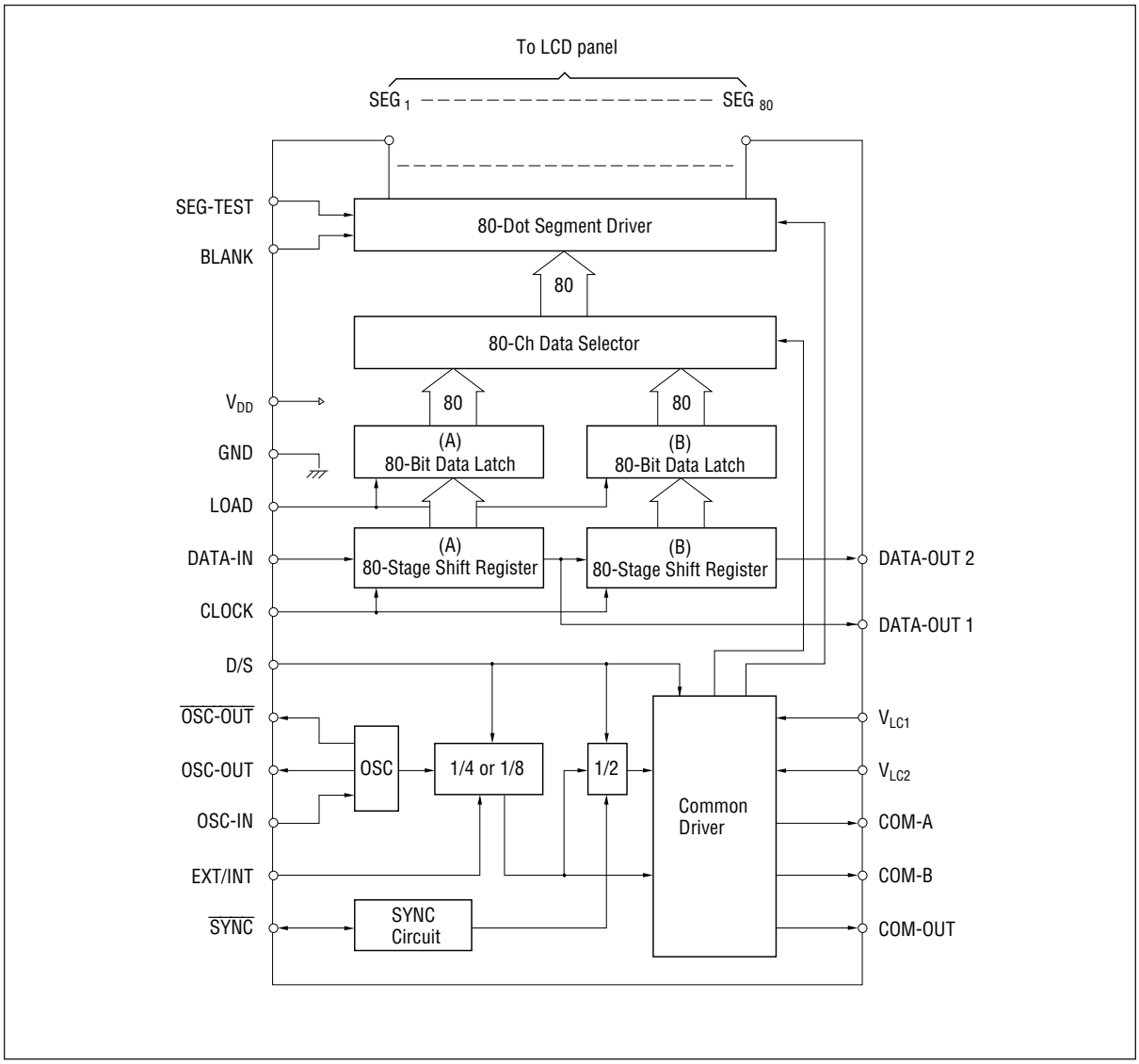
The display data is serially input from the DATA-IN pin to the 160-stage shift register synchronized with the CLOCK pulse. The data is shifted into the 160-bit data latch by the LOAD signal. Then the latched data is directly output to the LCD from the 80 pairs of LCD drivers as a serial output.

The common signal can be generated by the built-in generator, or externally input. The common synchronization circuit which is used in the dynamic display mode is integrated on the chip.

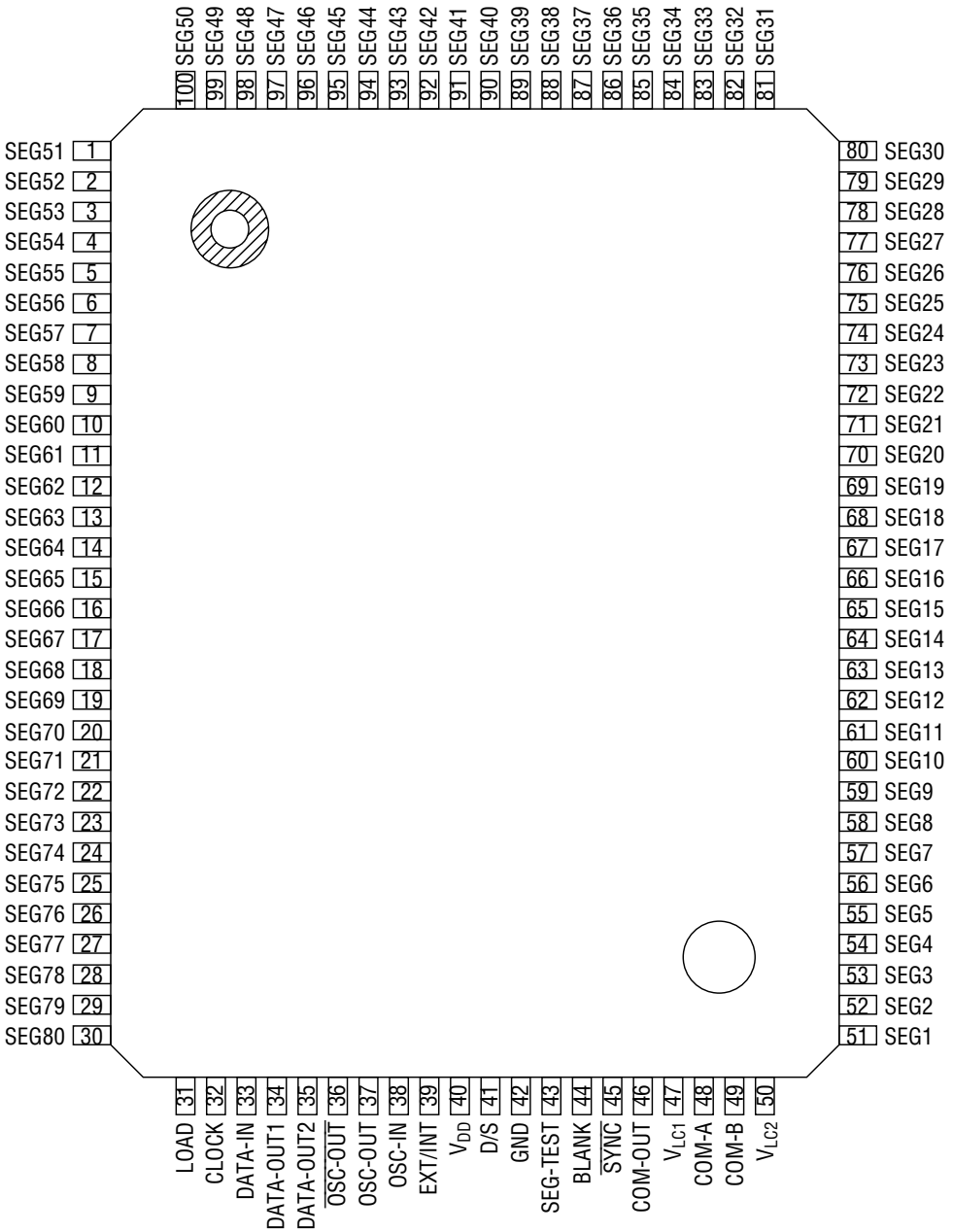
FEATURES

- Supply voltage : 3.0 to 6.0 V
- Drives LCD of up to 80 segments (in the static display mode)
- Drives LCD of up to 160 segments (in the 1/2 duty dynamic display mode)
- Simple interface with microcomputer
- Bit-to-bit correspondence between input data and output data
  H: Display ON L: Display OFF
- Can be cascade-connected
- Built-in common signal generator
- Can be synchronized with the external common signal
- Testing pins for all-on (SEG-TEST) and all-off (BLANK)
- Applicable as an output expander
- LCD driving voltage can be adjusted by the combination of V_{LC1} and V_{LC2}
- Package options:
  100-pin plastic QFP (QFP100-P-1420-0.65-K) (Product name : MSM5265GS-K)
  100-pin plastic QFP (QFP100-P-1420-0.65-BK) (Product name : MSM5265GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



100-Pin Plastic QFP

ABSOLUTE MAXIMUM RATINGS

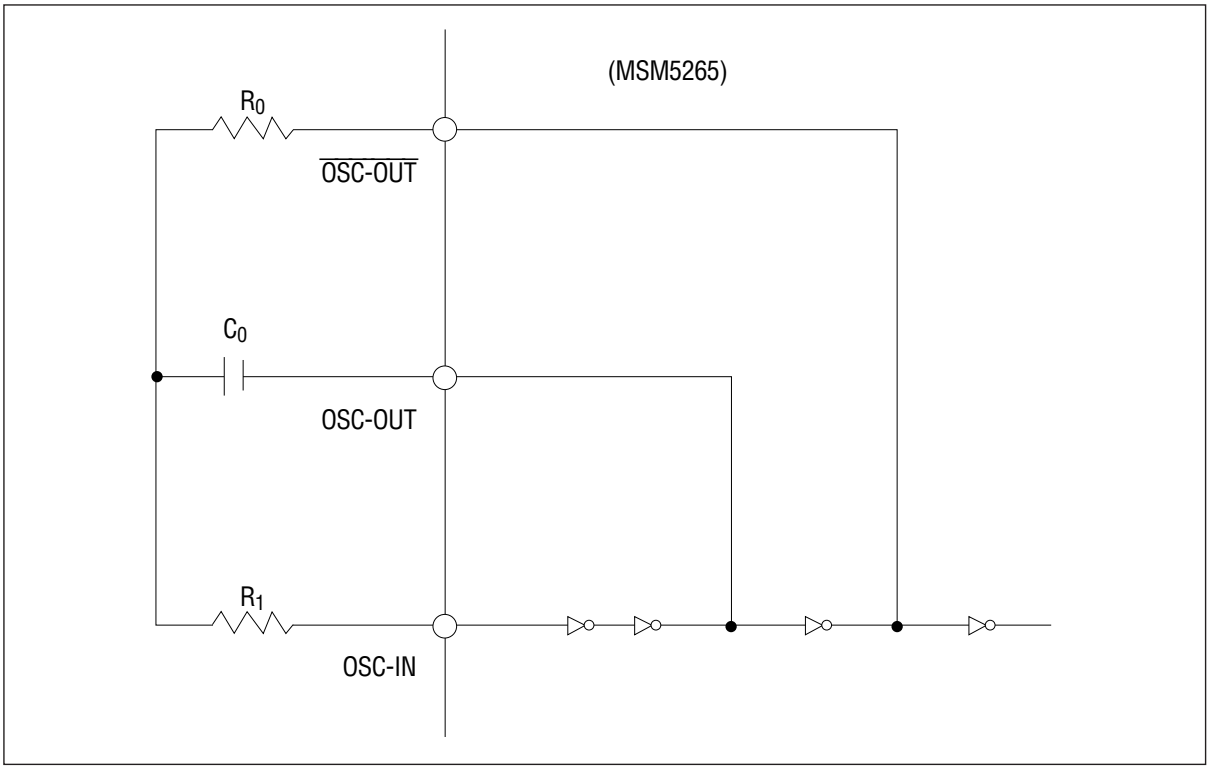
Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	T_a = 25°C	–0.3 to +6.5	V
Input Voltage	V_I	T_a = 25°C	GND–0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	—	3 to 6	V
Operating Temperature	T_{op}	—	–40 to +85	°C
LCD Driving Voltage	V_{LCD}	V_{DD}–V_{LC2}	3 to V_{DD}	V

• Oscillation circuit

Parameter	Symbol	Corresponding pin	Condition	Min.	Typ.	Max.	Unit
Oscillator Resistance	R_0	$\overline{\text{OSC-OUT}}$	—	56	100	220	kΩ
Oscillator Capacitance	C_0	OSC-OUT	Film capacitor	0.001	—	0.047	µF
Current Limiting Resistance	R_1	OSC-IN	$R_1 \geq 10\ R_0$	0.56	1	2.2	MΩ
Common Signal Frequency	f_{COM}	COM-A COM-B	—	25	—	150	Hz



ELECTRICAL CHARACTERISTICS
DC Characteristics

(V_{DD} = 5.0 V Ta =–40 to +85°C)

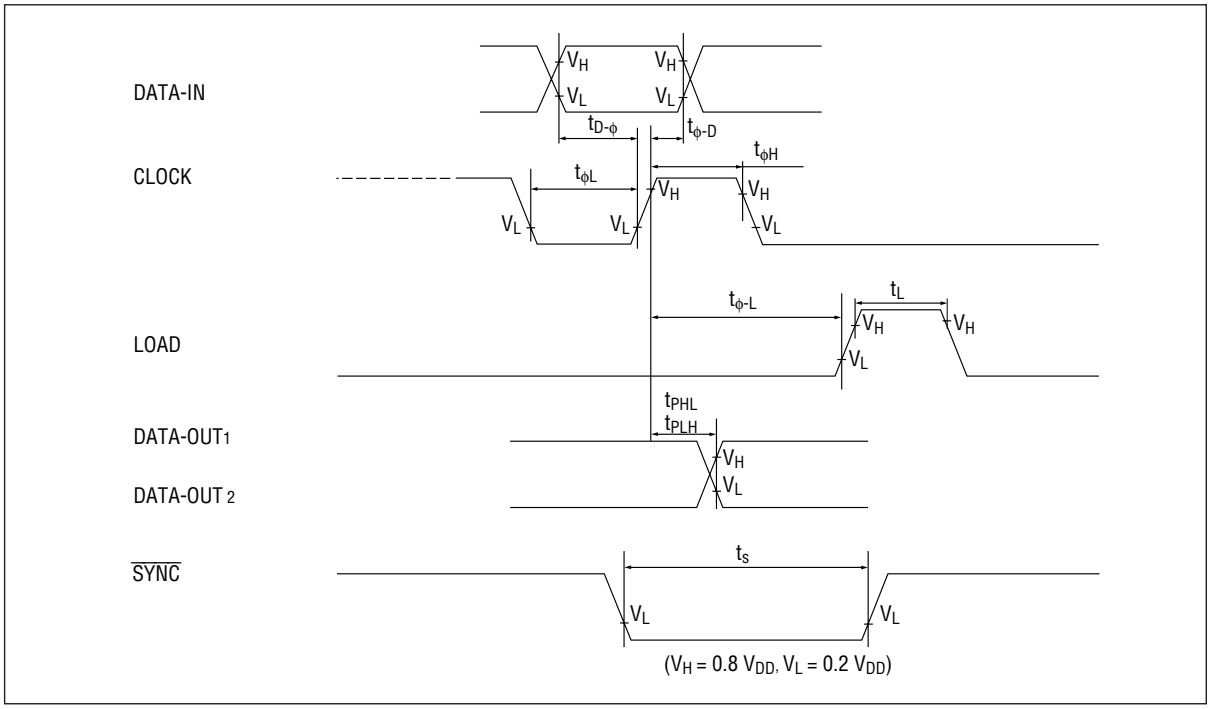
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" Input Voltage	V_{IH}	—	36	—	V_{DD}	V	SEG-TEST, BLANK, LOAD, DATA-IN, CLOCK, D/S, EXT/INT, OSC-IN
"L" Input Voltage	V_{IL}	—	GND	—	1.0	V	
Input Leakage Current	I_{IL}	V_I = 5.0 V/0 V	—	—	±1	µA	
"H" Output Voltage	V_{OH}	I_O = –100 µA	4.5	—	—	V	DATA-OUT1 DATA-OUT2 COM-OUT
		I_O = –200 µA	4.5	—	—	V	OSC-OUT $\overline{\text{OSC-OUT}}$
		V_{LC1} = 2.5 V, V_{LC2} = 0 V I_O = –30 µA	4.8	—	—	V	SEG_1-SEG_{80}
		V_{LC1} = 2.5 V, V_{LC2} = 0 V I_O = –150 µA	4.8	—	—	V	COM-A COM-B
"M" Output Voltage	V_{OM}	V_{LC1} = 2.5 V, V_{LC2} = 0 V I_O = ±150 µA	2.3	—	2.7	V	COM-A COM-B
"L" Output Voltage	V_{OL}	I_O = 100 µA	—	—	0.5	V	DATA-OUT1 DATA-OUT2 COM-OUT
		I_O = 200 µA	—	—	0.5	V	OSC-OUT $\overline{\text{OSC-OUT}}$
		V_{LC1} = 2.5 V, V_{LC2} = 0 V I_O = 30 µA	—	—	0.2	V	SEG_1 - SEG_{80}
		V_{LC1} = 2.5 V, V_{LC2} = 0 V I_O = 150 µA	—	—	0.2	V	COM-A COM-B
		I_O = 250 µA	—	—	0.8	V	$\overline{\text{SYNC}}$
Output Leakage Current	I_{LO}	V_O = 5 V when internal Tr is off	—	—	5	µA	$\overline{\text{SYNC}}$
Segment Output Impedance	R_{SEG}	V_{LC1} = (5+V_{LC2})/2 V_{LC2} = 0 to 2 V	—	—	10	kΩ	SEG_1 - SEG_{80}

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin
Common Output Impedance	R_{COM}	$V_{LC1} = (5+V_{LC2})/2$ V_{LC2} = 0 to 2 V	—	—	1.5	kΩ	COM-A COM-B
Static Supply Current	I_{DD1}	Fix all input levels at either V_{DD} or GND	—	—	100	µA	V_{DD}
Dynamic Supply Current	I_{DD2}	No load. R_0 = 100 kΩ, C_0 = 0.01 µF, R_1 = 1 MΩ	—	0.12	0.5	mA	

Switching Characteristics

(V_{DD} = 3.0 to 6.0 V Ta = –40 to +85°C)

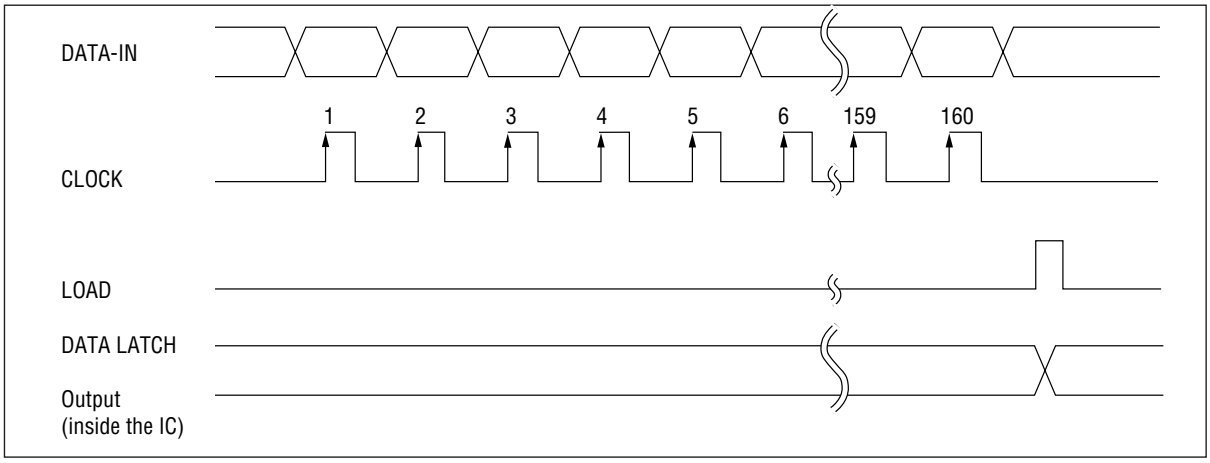
Parameter	Symbol	Condition	Min.	Max.	Unit	Applicable Pin
Clock Frequency	f_ϕ	—	—	1	MHz	CLOCK
Clock Pulse "H" Time	$f_{\phi H}$	—	0.3	—	µs	
Clock Pulse "L" Time	$f_{\phi L}$	—	0.5	—	µs	
Data Setup Time	$f_{D-\phi}$	—	0.1	—	µs	DATA-IN
Data Hold Time	$f_{\phi-D}$	—	0.1	—	µs	CLOCK
"H", "L" Propagation Delay Time	t_{PHL} t_{PLH}	Load capacitance of DATA-OUT1, DATA-OUT2: 15 pF	—	0.8	µs	DATA-OUT1 DATA-OUT2 CLOCK
LOAD Pulse "H" Time	t_L	—	0.2	—	µs	LOAD
Clock → LOAD Time	$t_{\phi-L}$	—	0.1	—	µs	CLOCK LOAD
OSC-IN Input Frequency	f_{OSC}	—	—	5	kHz	OSC-IN
$\overline{SYNC}$ Pulse "L" Time	t_s	—	0.2	—	µs	$\overline{SYNC}$



FUNCTIONAL DESCRIPTION

Operational Description

The MSM5265 consists of a 160-stage shift register, 160-bit data latch, and 80 pairs of LCD drivers. The display data is input from the DATA-IN pin to the 160-stage shift register at the rising edge of the CLOCK pulse and it is shifted to the 160-bit data latch when the LOAD signal is set at "H" level, then it is directly output from the 80 pairs of LCD drivers to the LCD panel. Input the display data in the order of SEG80, SEG79, SEG78, ..., SEG2, SEG1.



Pin Functional Description

- **OSC-IN, OSC-OUT, $\overline{\text{OSC-OUT}}$**

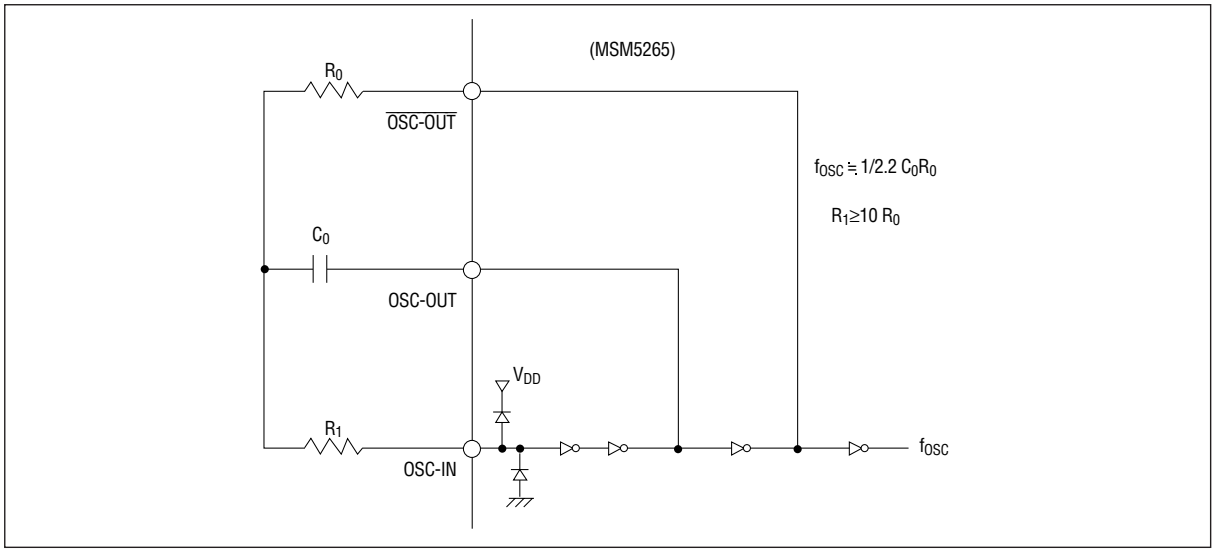
As shown in the figure below, by connecting the external resistors R_0, R_1 and external capacitor C_0 with OSC-IN, OSC-OUT and $\overline{\text{OSC-OUT}}$ respectively, an oscillating circuit to generate the common signal is formed.

This frequency is divided into either 1/8 or 1/4 by the internal dividing circuit. The 1/8 divided frequency is used in the static display mode, while the 1/4 divided frequency is used as the common signal in the 1/2 duty dynamic display mode which is output from the COM-OUT pin. (EXT/INT should be set at low level.)

The resistor R_1 is used to limit the current on the OSC-IN pin's protecting diodes. The value of the R_1 should be more than 10 times that of R_0.

When the external common signal is used, the EXT/INT pin should be set at high level and the external common signal should be input from the OSC-IN pin.

Keep the wiring between the OSC-IN pin and R_1 as short as possible, because the OSC-IN pin becomes susceptible to external noise if the value of R_1 is large.



- **D/S**
  When this pin is set at high level, the MSM5265 operates in the 1/2 duty dynamic display mode, the MSM5265 operates in the static display mode when this pin is set at low level.

- **EXT/INT**
  When the external common signal is used, fix this pin at high level and input the external common signal from the OSC-IN pin. The input common signal is used as the internal common signal and is output from the COM-OUT pin through the buffer. When the built-in common signal generator is used, fix this pin at low level. When the MSM5265 is used as an output expander, fix this pin at high level and the OSC-IN pin at low level. The output logic can be reveresed in respect to the input data by setting OSC-IN to "H" level.

- **COM-OUT**
  When two or more MSM5265s are connected in series (cascade connection), this pin should be connected with all of the slave MSM5265's OSC-IN pins.

- **$\overline{\text{SYNC}}$**
  This pin is an input/output pin which is used when two or more MSM5265s are connected in series (cascade connection) in the 1/2 duty dynamic display mode. All of the involved MSM5265's $\overline{\text{SYNC}}$ pins should be connected by the same line and they should be pulled up with a common resistor, which makes a phase level of all involved MSM5265's COM-A and COM-B pins equal. When a single MSM5265 is used in the dynamic display mode, $\overline{\text{SYNC}}$ should be pulled up with a resistor.
  Connect this pin to GND if any of the following conditions is true:
  – the MSM5265 is operated in the static display mode
  – two or more MSM5265 devices are cascade connected
  – a single MSM5265 device is used
  – the MSM5265 is used as an output expander

- **DATA-IN, CLOCK**
  The display data is serially input from the DATA-IN pin to the 160-stage shift register at the rising edge of the CLOCK pulse. The high level of the display data is used to turn the display on, while low level of the display data is used to turn off the display.

- **DATA-OUT1**
  The 80th stage of the shift register contents is output from this pin.
  When two or more MSM5265s are connected in series (cascade connection) in the static display mode, this pin should be connected to the next MSM5265's DATA-IN pin.

- **DATA-OUT2**
  The 160th stage of the shift register contents is output from this pin.
  When two or more MSM5265s are connected in series (cascade connection) in the 1/2 duty dynamic display mode, this pin should be connected to the next MSM5265's DATA-IN pin.

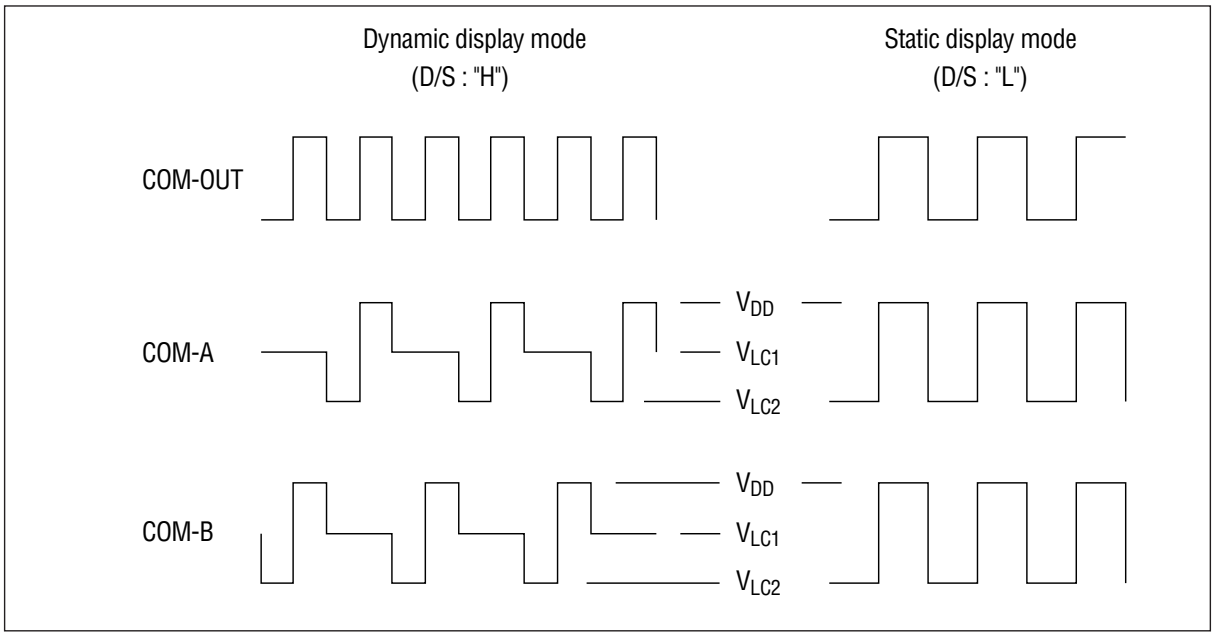
- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at high level, the shift register contents are shifted to the 80 sets of LCD drivers. When this pin is set at low level, the last display data is held which was transfered to the 80 sets of LCD drivers when LOAD pin was set at high level.

- **V_{LC2}**
  Supply voltage pin for the 80 sets of LCD drivers. The input level to this pin should be the low level output voltage of segment outputs (SEG_1 to SEG_{80}) and common outputs (COM-A, COM-B).
  In this case, the high level of segment outputs and common outputs is the V_{DD} level, while low level of segment outputs and common outputs is V_{LC2} level. V_{LC2} should be set at higher level than ground level.

- **V_{LC1}**
  Supply voltage pin for the middle level voltage of the common outputs. The input level of this pin is the middle level output voltage of the common outputs (COM-A, COM-B) in the 1/2 duty dynamic display mode.
  The value of V_{LC1} is calculated by the following formula:
  $$V_{LC1} = (V_{DD} + V_{LC2})/2$$
  In the static display mode, this pin should be open.

- **COM-A, COM-B**
  LCD driving common signals are output from these pins. These pins should be connected to the common side of the LCD panel.
  – In the static display mode
    A pulse in phase with the COM-OUT output is output from both COM-A and COM-B. In this case, the high level is V_{DD}, and the low level is V_{LC2}.
  – In the 1/2 duty dynamic display mode
    The COM-A and COM-B output signals are alternately changed within each COM-OUT output cycle, resulting in alternate repetition of select and non-select modes.

    In the select mode, a signal in phase with the COM-OUT signal is output at "H" (V_{DD}) and "L" (V_{LC2}).
    In the non-select mode, a voltage is output at "M" (V_{LC1}). In the select mode of COM-A (non-select mode of COM-B), signals that correspond to the 1st- to 80th-bit data of the data latch are output to the segment outputs.
    In the select mode of COM-B (non-select mode of COM-A), signals that correspond to the 81st- to 160th-bit data of the data latch are output to the segment outputs.



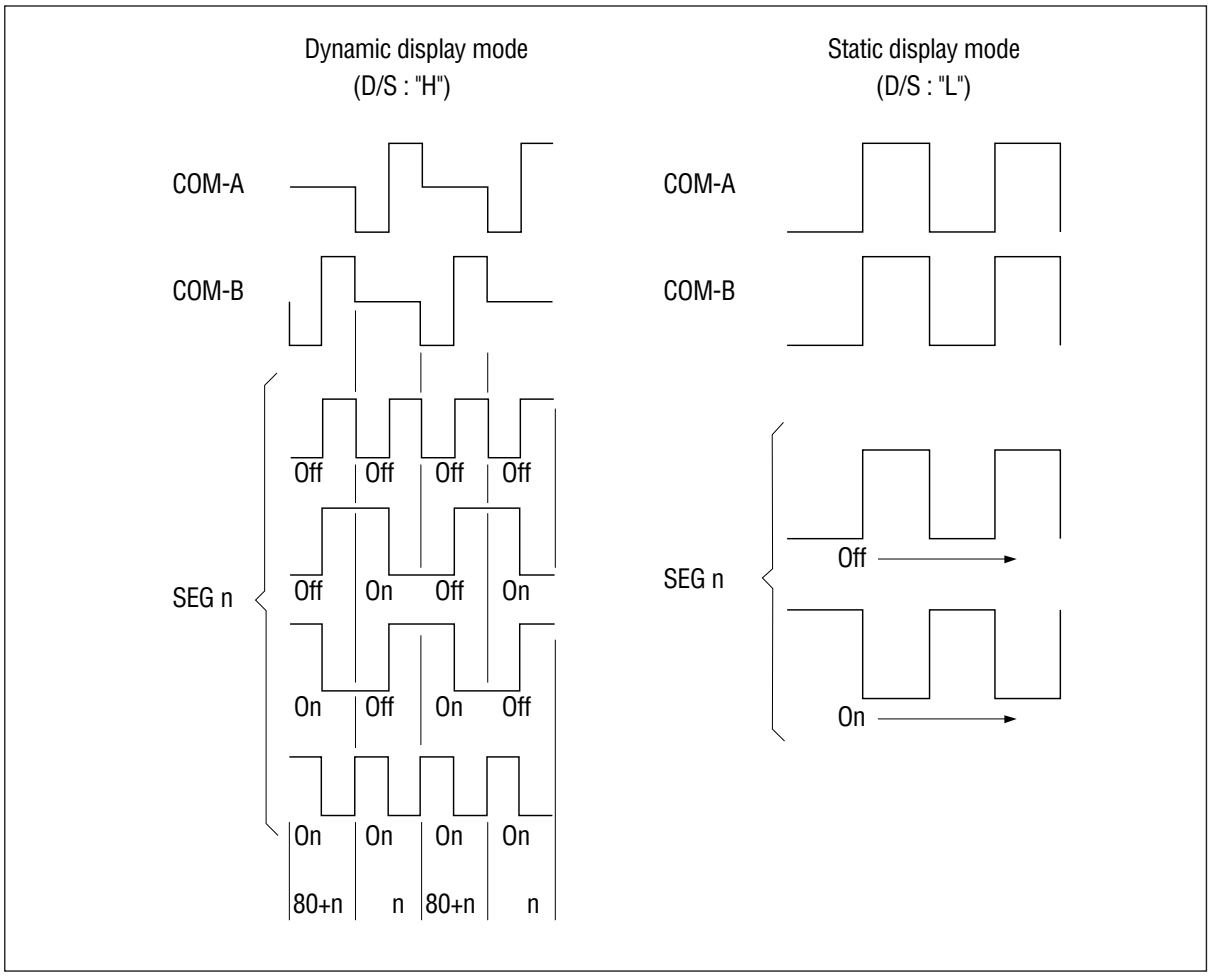
- **SEG_1 to SEG_{80}**
  LCD segment driving signals are output from these pins and they should be connected to the segment side of the LCD panel.
  "H" level : V_{DD}, "L" level : V_{LC2}
  – In the static display mode
  The nth-bit data of the data latch (A) corresponds to the SEG n. The data of the data latch (B) is invalid .
  A signal out of phase with the COM-OUT signal is output to the segment outputs when the display is turned on, while a signal in phase with it is output when the display is turned off.

  – In the 1/2 duty dynamic display mode
  Output of the SEG n corresponds to as follows.

  When COM-A is in select mode:
  nth-bit data of the data latch (A)

  When COM-B is in select mode:
  nth-bit data of the data latch (B)

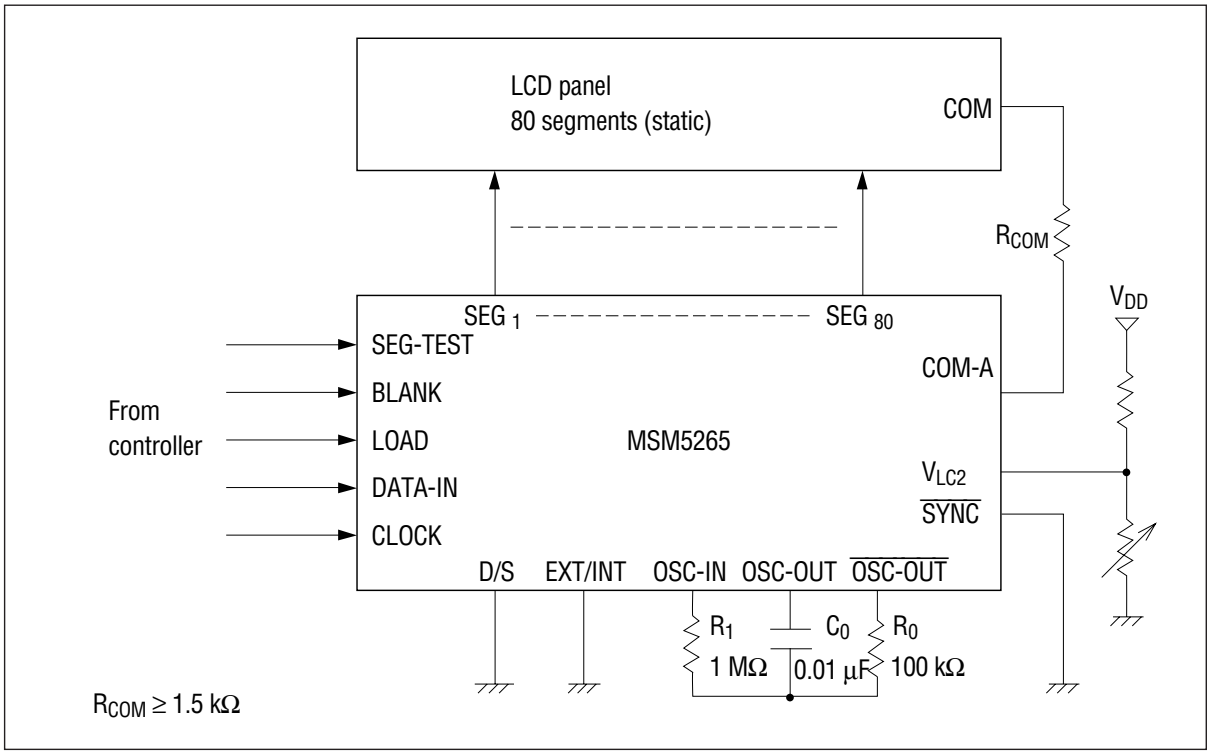
  When the display is turned on, a signal out of phase with the common signal corresponding to the data is output, while a signal in phase with the common signal is output when the display is turned off.



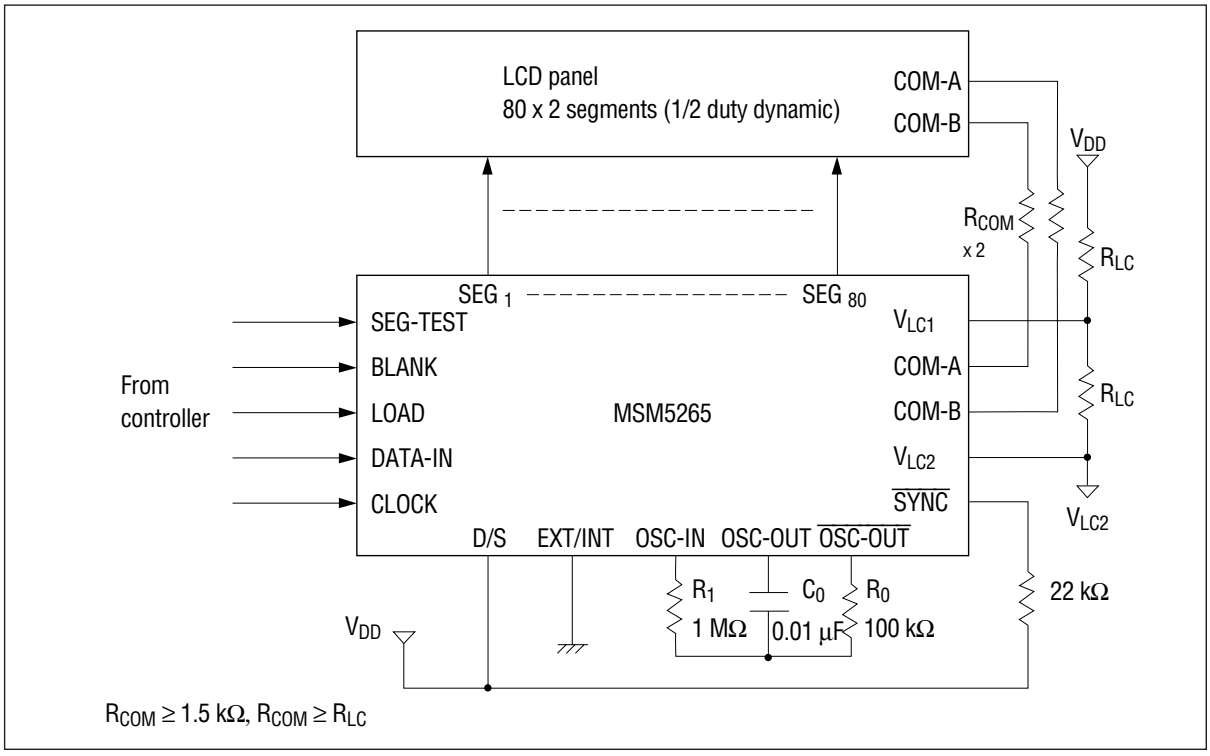
- **SEG-TEST**
  This pin is used to test the segment outputs (SEG_1 to SEG_{80}). All displays are turned on when this pin is set to high level. The display returns to the condition before the pin was set to high level. When this pin is at high level, the input on the BLANK pin is disabled.
- **BLANK**
  This pin is also used to test the segment outputs (SEG_1 to SEG_{80}). All displays are turned off when this pin is set to high level. The display returns to the condition before the pin was set to high level.
  When SEG-TEST pin is at high level, the input on this pin is disabled.

APPLICATION CIRCUITS

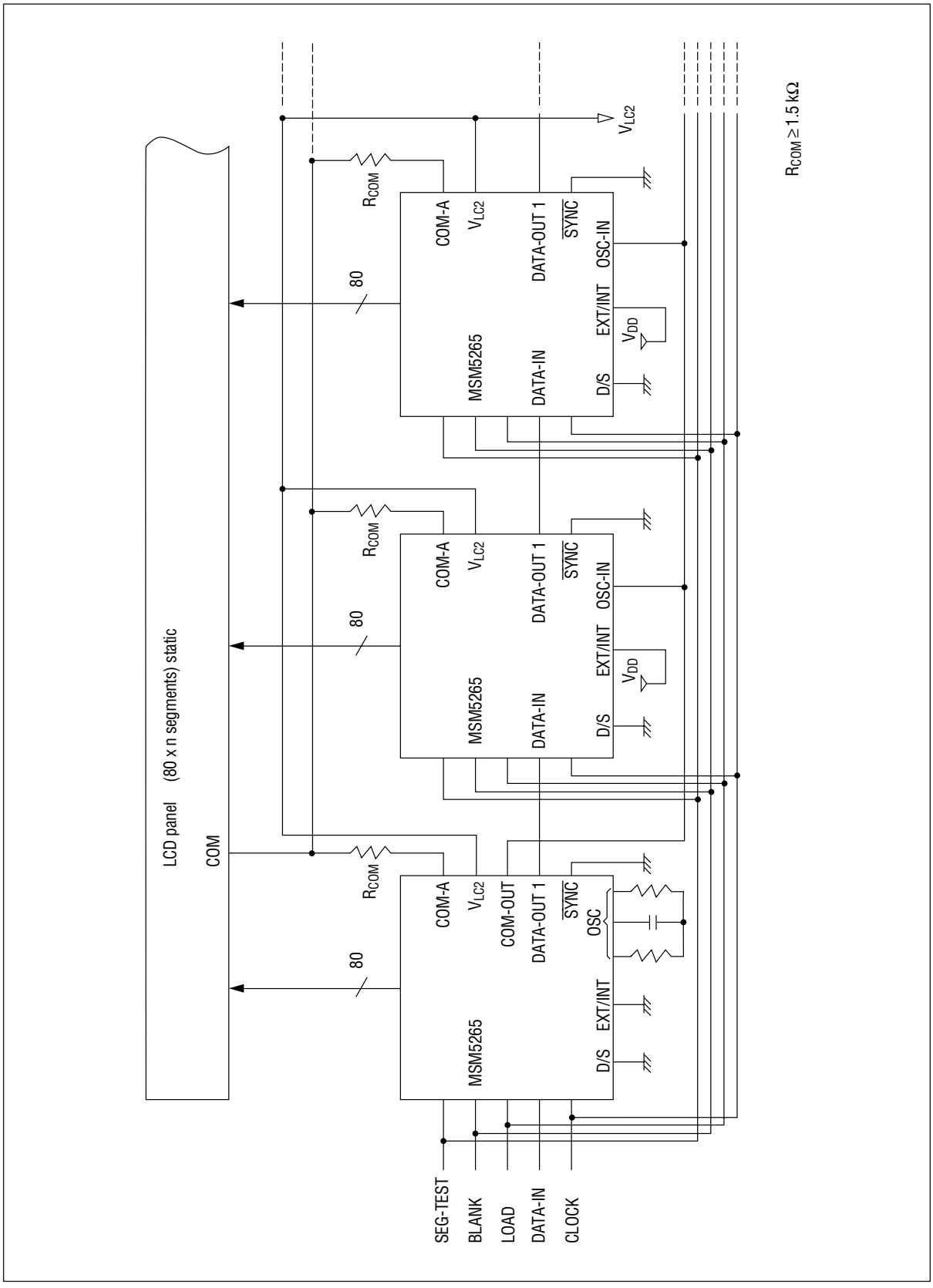
1) Single MSM5265 operation in the static display mode



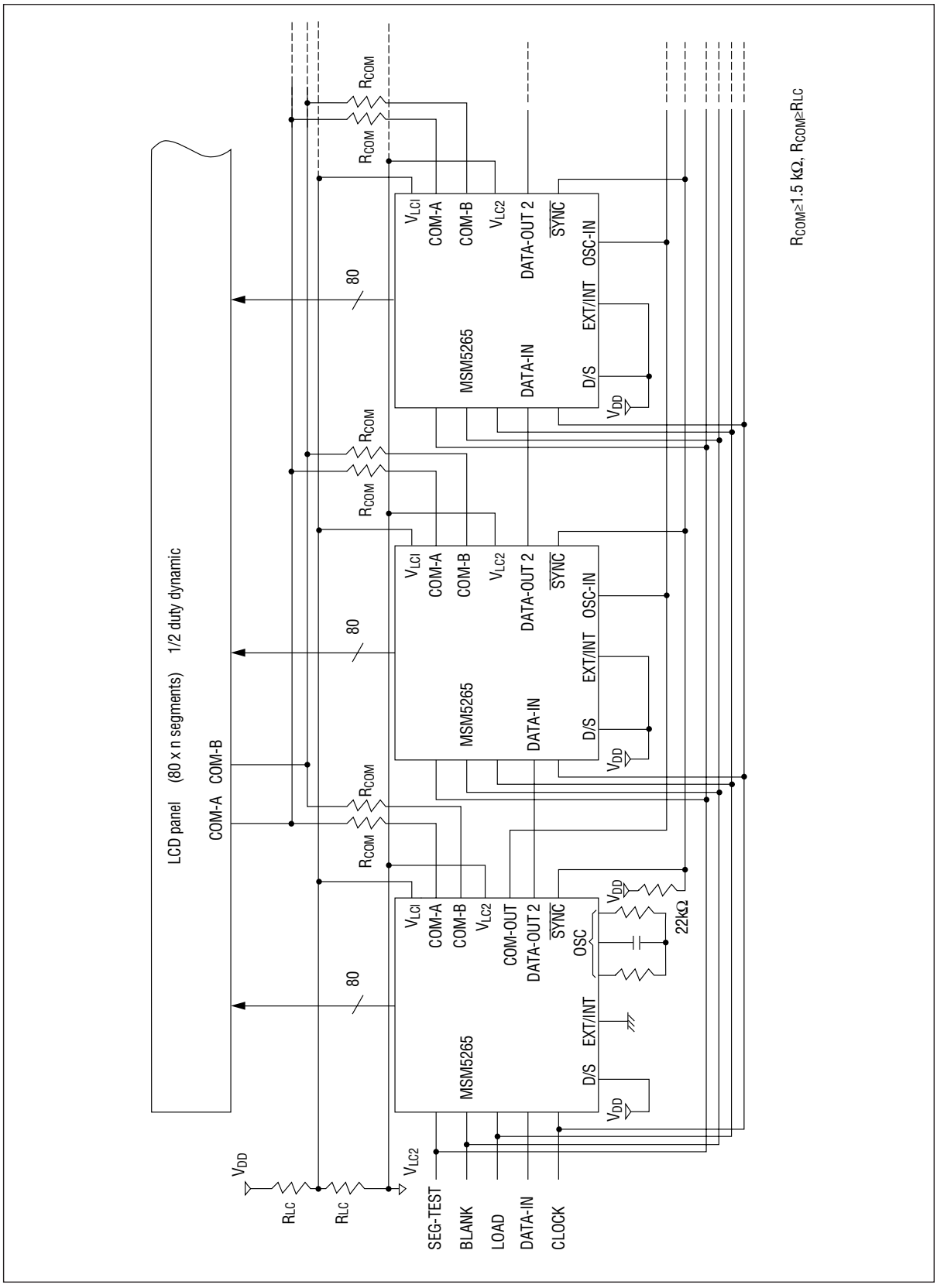
2) Single MSM5265 operation in the 1/2 duty dynamic display mode



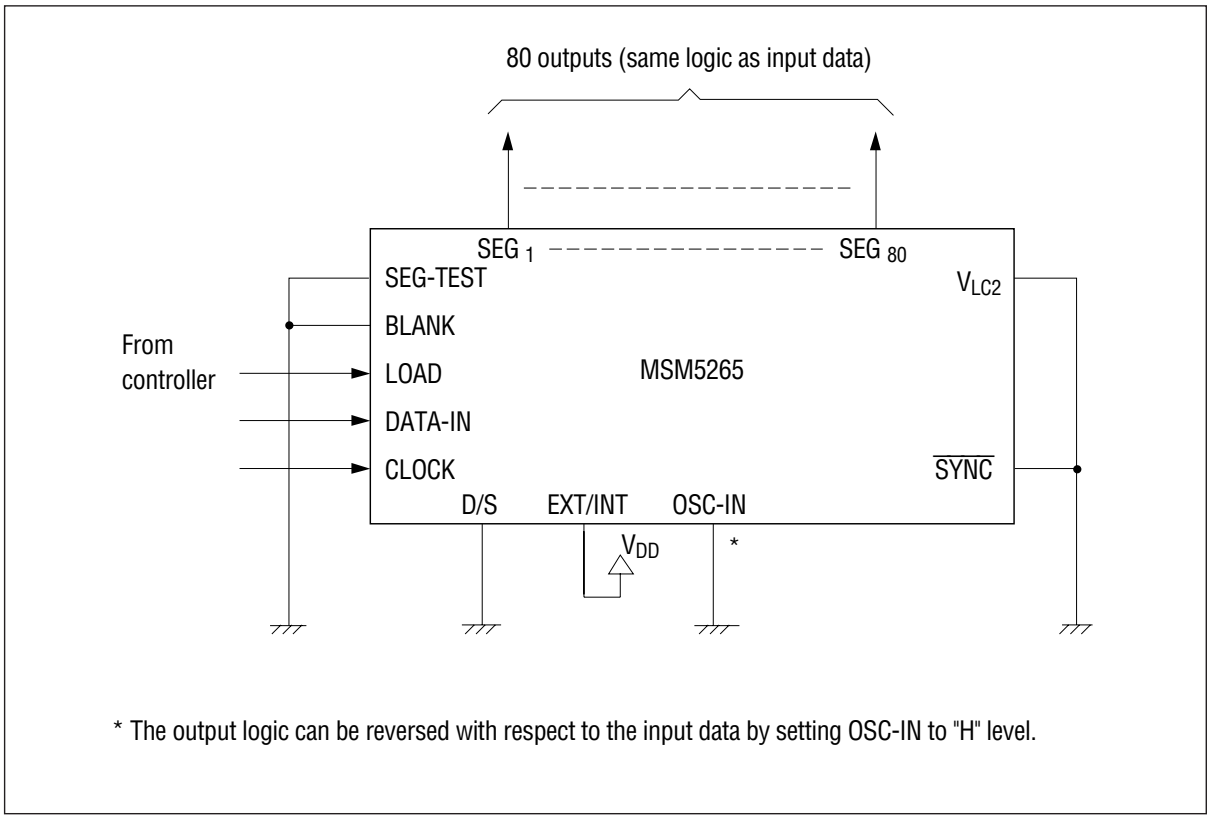
3) Cascade connections for MSM5265s in the static display mode



4) Cascade connections for MSM5265s in the 1/2 duty dynamic display mode



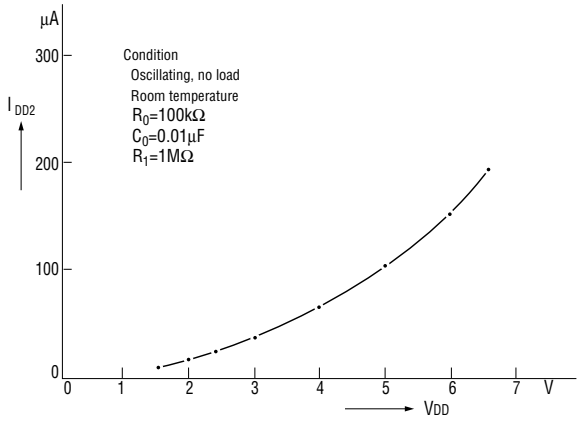
5) Output-expander



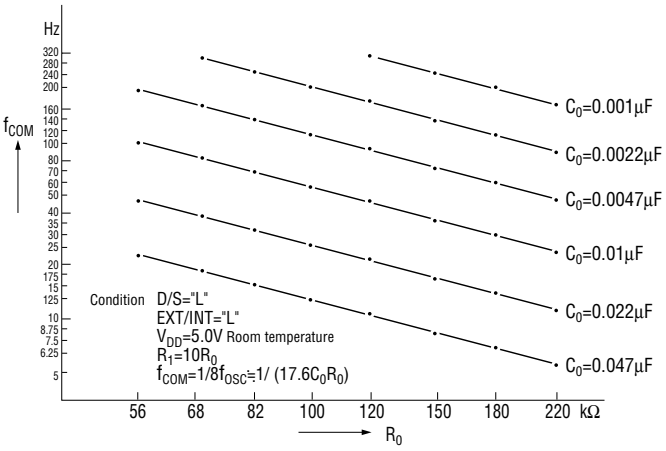
* The output logic can be reversed with respect to the input data by setting OSC-IN to "H" level.

REFERENCE DATA

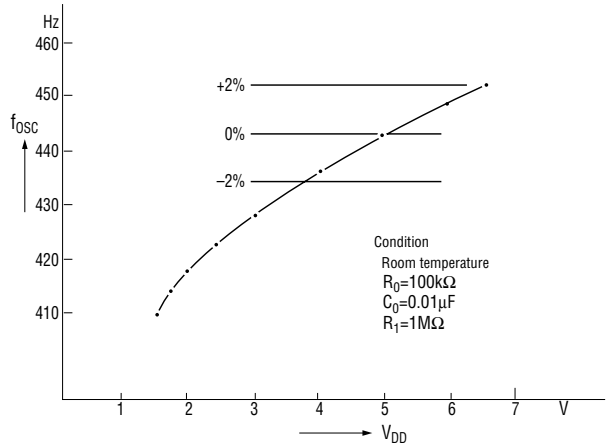
I_{DD2} vs. V_{DD}



f_{COM} vs. R_0, C_0



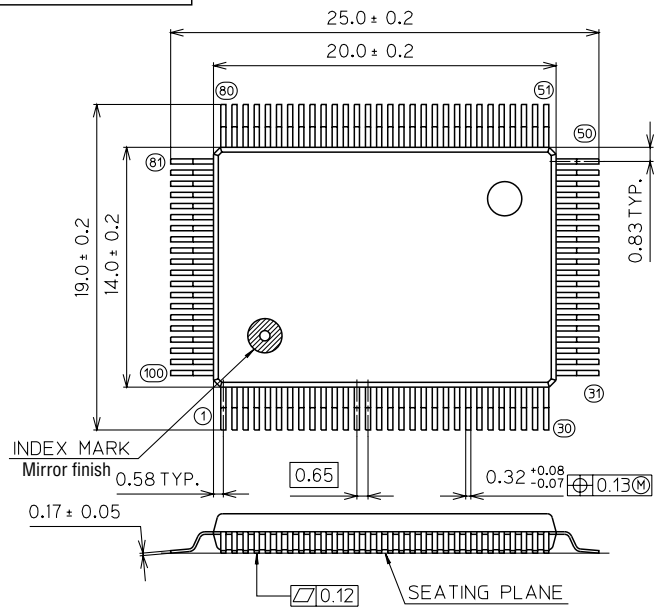
f_{OSC} vs. V_{DD}

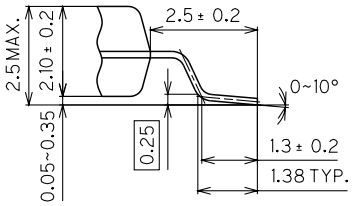


PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-K





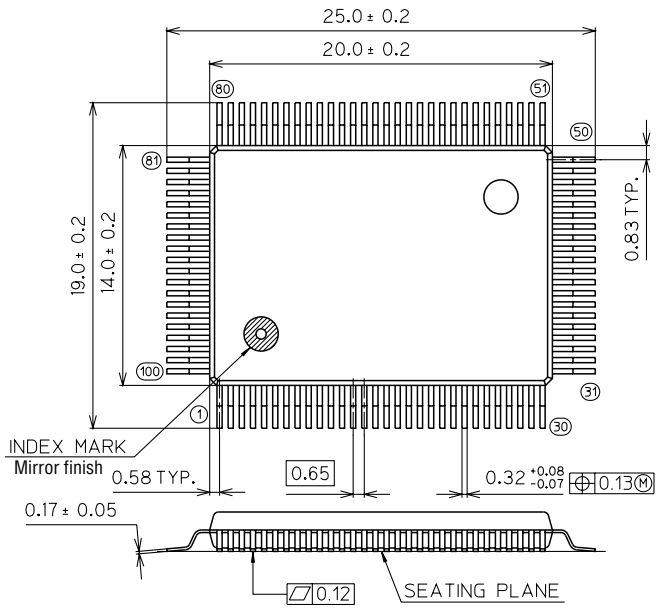
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	1.29 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP100-P-1420-0.65-BK



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