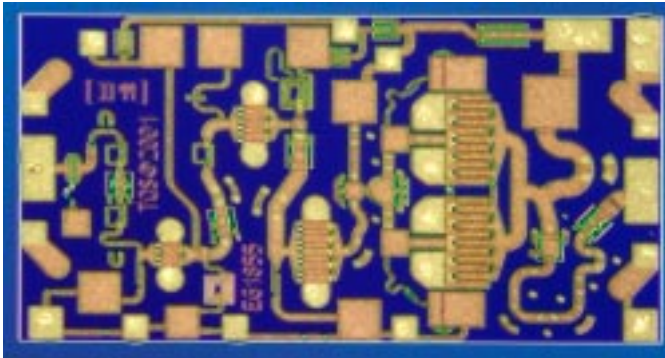


12-19 GHz VSAT Amplifier

TGA2508-EPU

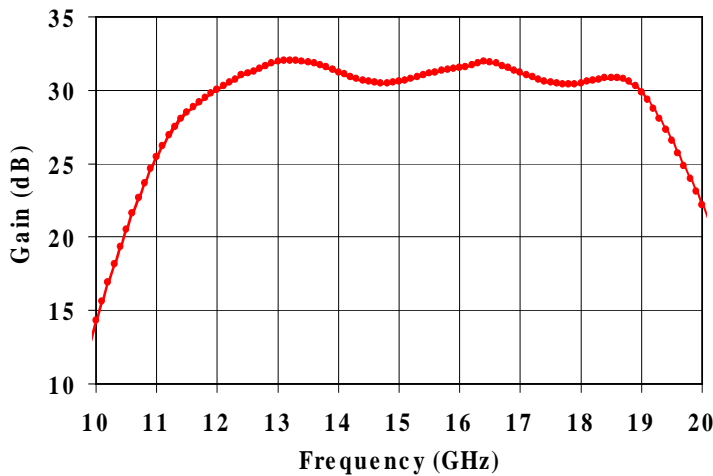


Key Features

- 0.50 um pHEMT Technology
- 30 dB Nominal Gain
- 30 dBm P1dB @ 15 GHz
- Bias Conditions: 7 V, 433 mA
- Chip Dimensions: 2.1 x 1.1 x 0.1 mm

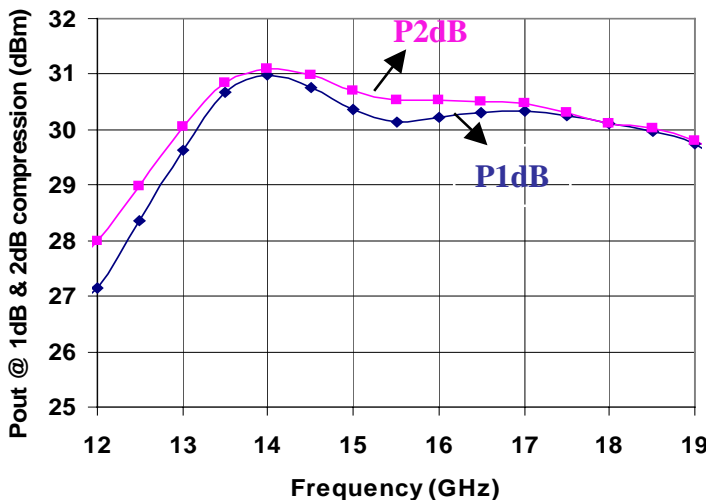
Preliminary Measured Data

Bias Conditions: Vd = 7 V, Id = 433 mA



Primary Applications

- VSAT Ground Terminals
- Point to Point Radio
- Military Ku Band



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

TABLE I
MAXIMUM RATINGS 5/

SYMBOL	PARAMETER	VALUE	NOTES
V ⁺	Positive Supply Voltage	8 V	<u>4/</u>
V ⁻	Negative Supply Voltage Range	-2 to 0 V	
I ⁺	Positive Supply Current (Quiescent)	591 mA	<u>4/</u>
I _G	Gate Supply Current	16 mA	
P _{IN}	Input Continuous Wave Power	17 dBm	
P _D	Power Dissipation	6.75 W	<u>3/ 4/</u>
T _{CH}	Operating Channel Temperature	150 °C	<u>1/ 2/</u>
T _M	Mounting Temperature (30 Seconds)	320 °C	
T _{STG}	Storage Temperature	-65 to 150 °C	

- 1/ These ratings apply to each individual FET.
- 2/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 3/ When operated at this bias condition with a base plate temperature of 70 °C, the median life is reduced from 6.4E+7 to 1E+6 hrs.
- 4/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.
- 5/ These ratings represent the maximum operable values for this device.

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TABLE II
ELECTRICAL CHARACTERISTICS

(Ta = 25°C ± 5°C)

PARAMETER	TYPICAL	UNITS
Drain Operating	7	V
Quiescent Current	433	mA
Small Signal Gain	30	dB
Input Return Loss (Linear Small Signal)	17	dB
Output Return Loss (Linear Small Signal)	7	dB
Output Power @ 1 dB Compression Gain @ 15GHz	30	dBm

TABLE III
THERMAL INFORMATION*

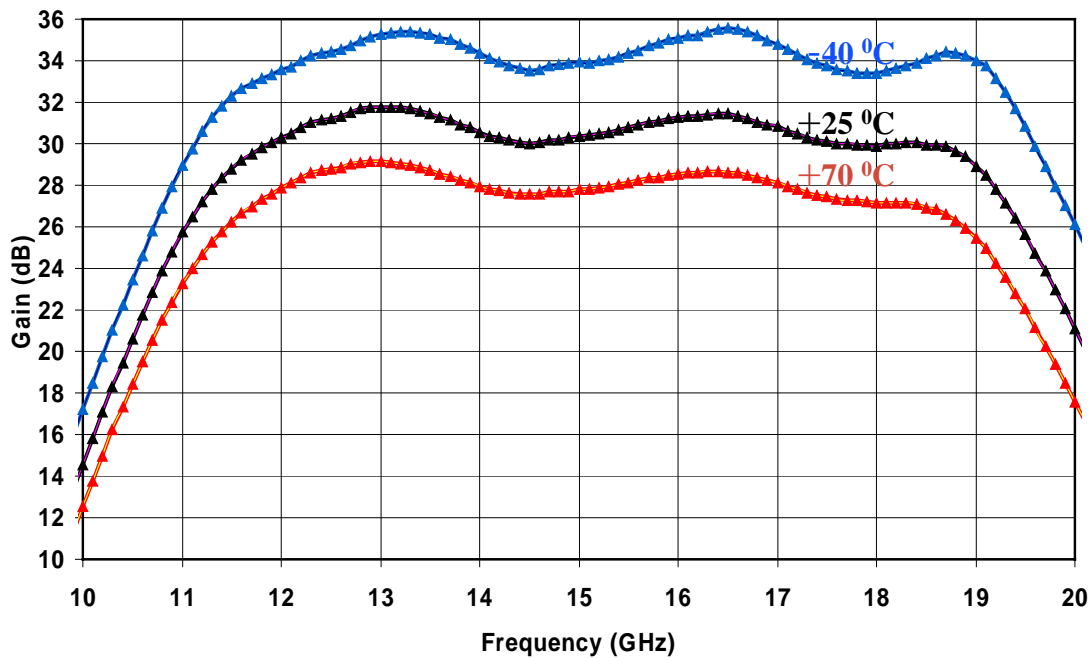
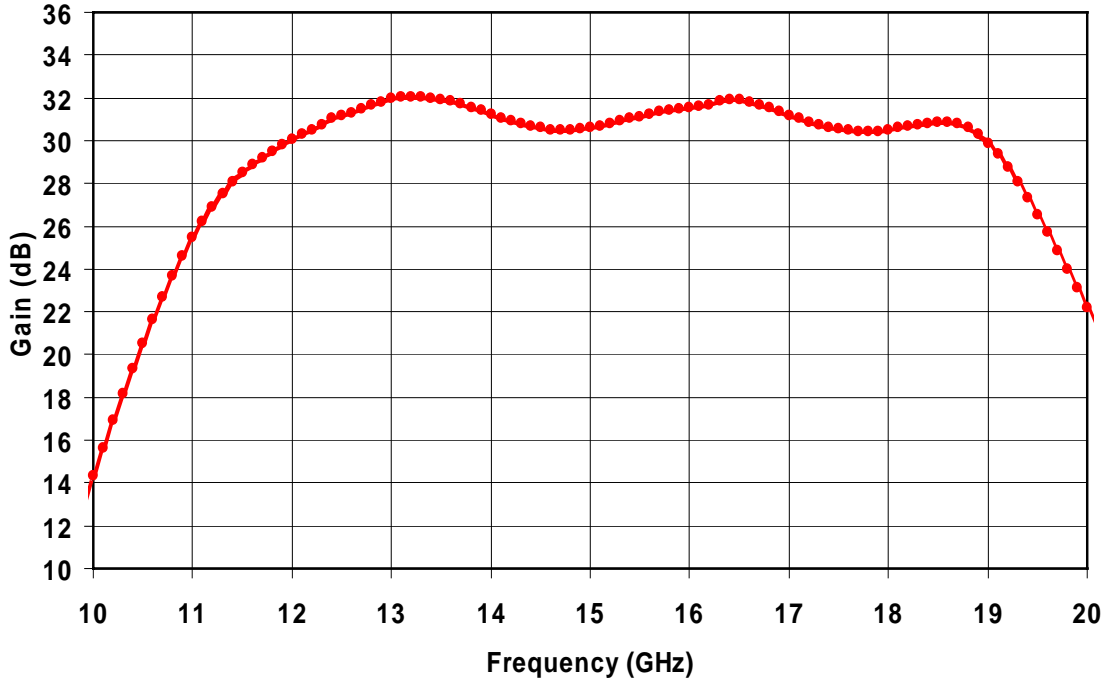
PARAMETER	TEST CONDITIONS	T _{CH} (°C)	R _{θJC} (°C/W)	T _M (HRS)
R _{θJC} Thermal Resistance (channel to backside of carrier)	Vd = 7 V I _D = 433 mA P _{diss} = 3.031 W	105.92	11.85	6.4E+7

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

* This information is a result of a thermal model.

Preliminary Measured Data

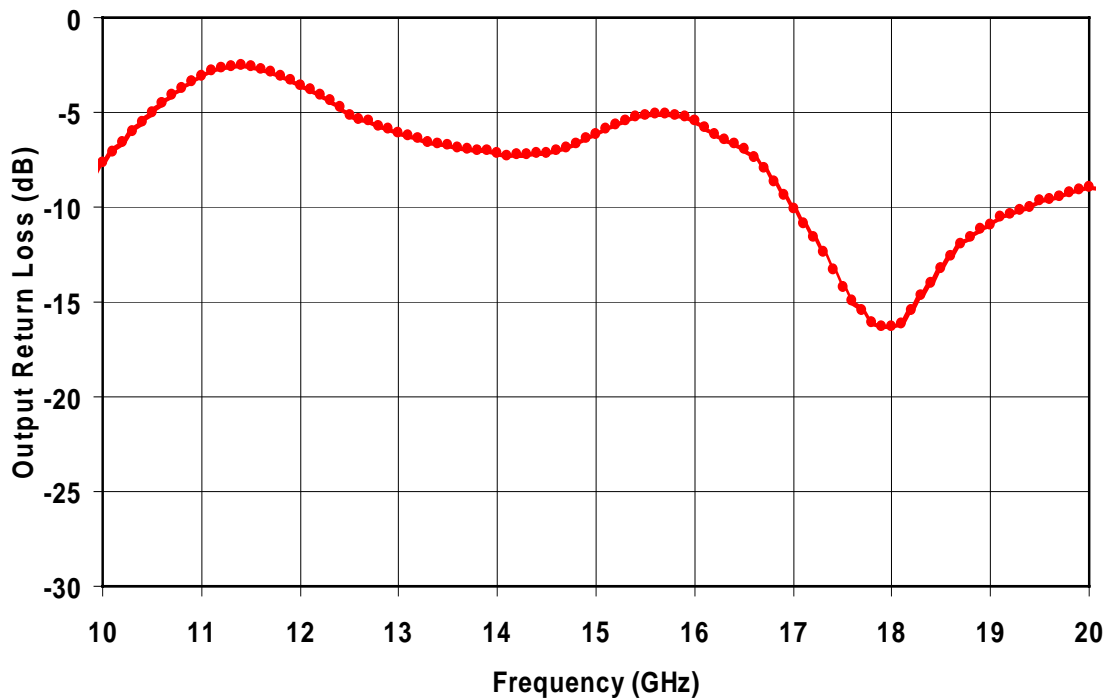
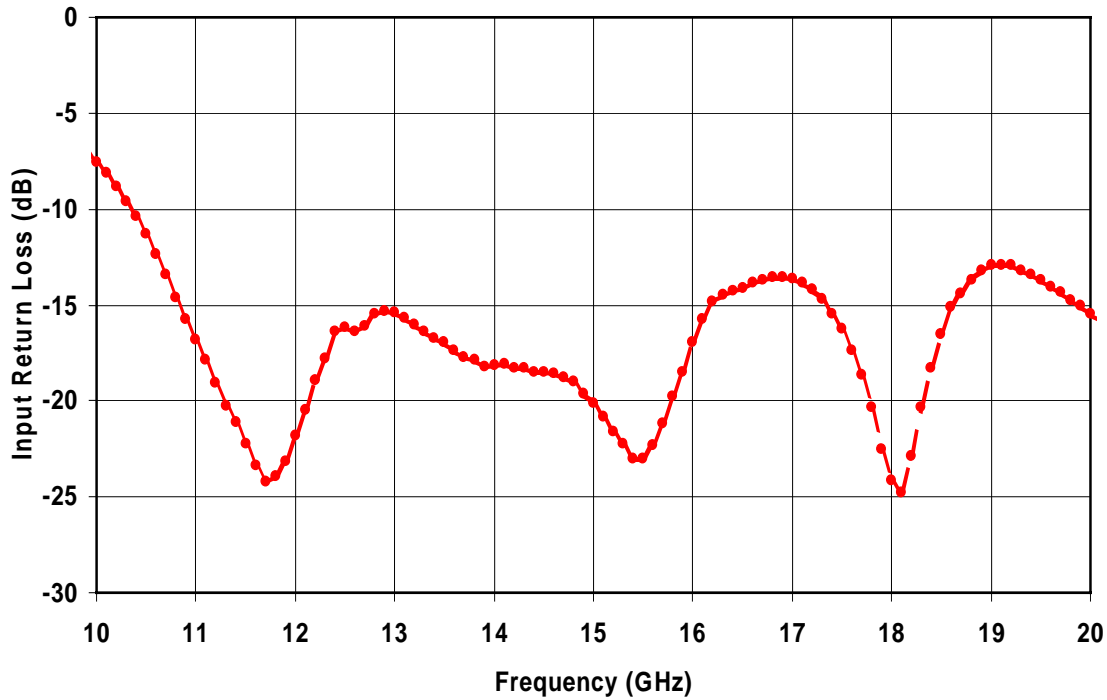
Bias Conditions: $V_d = 7\text{ V}$, $I_d = 433\text{ mA}$



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Preliminary Measured Data

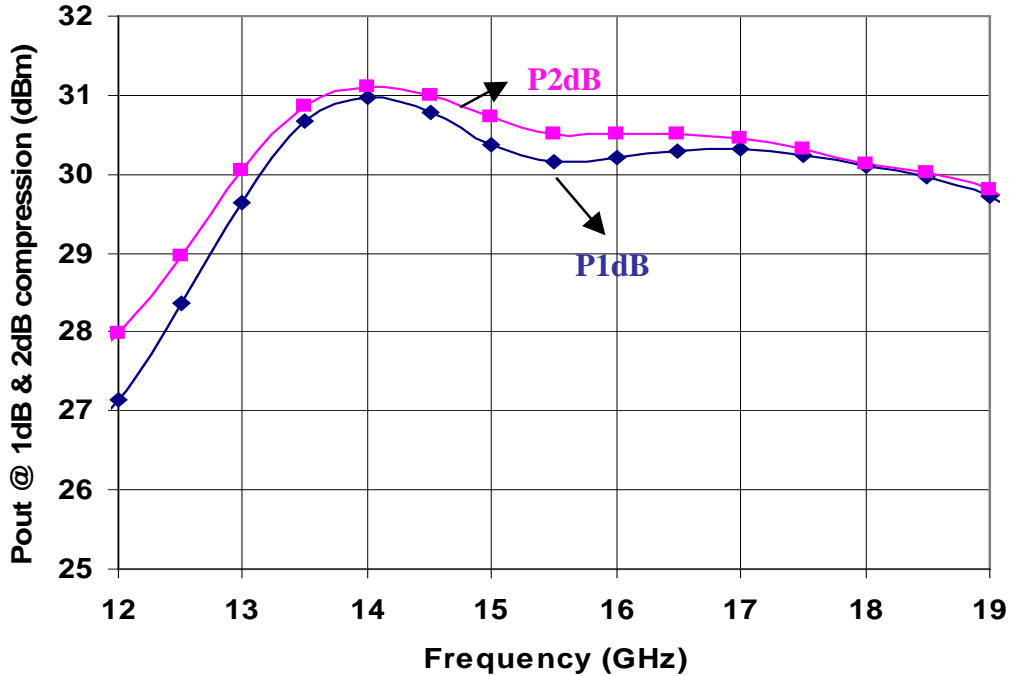
Bias Conditions: $V_d = 7\text{ V}$, $I_d = 433\text{ mA}$



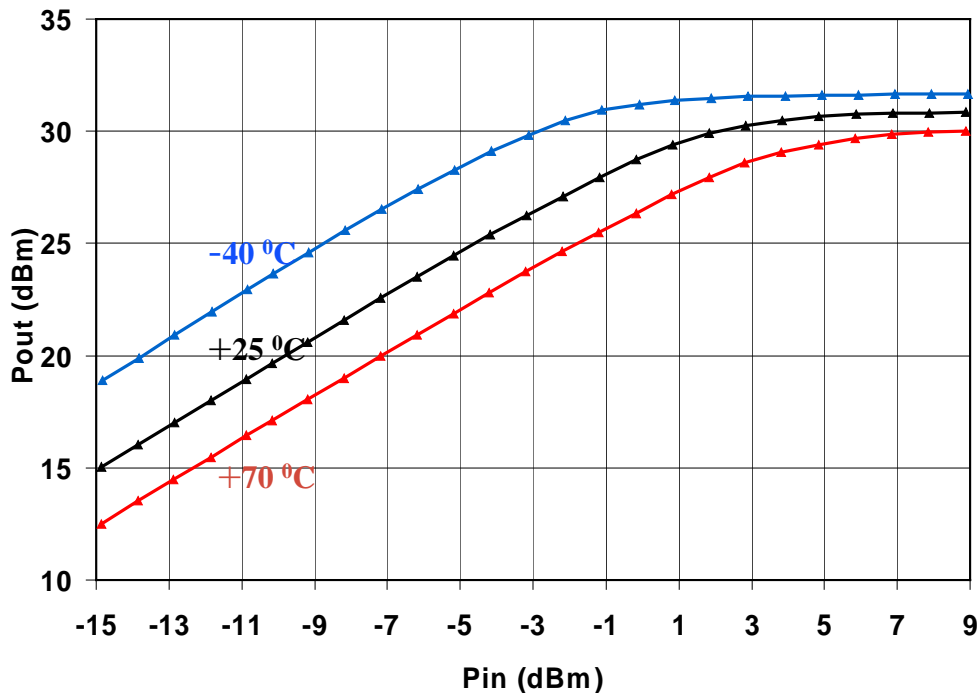
Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Preliminary Measured Data

Bias Conditions: $V_d = 7\text{ V}$, $I_d = 433\text{ mA}$



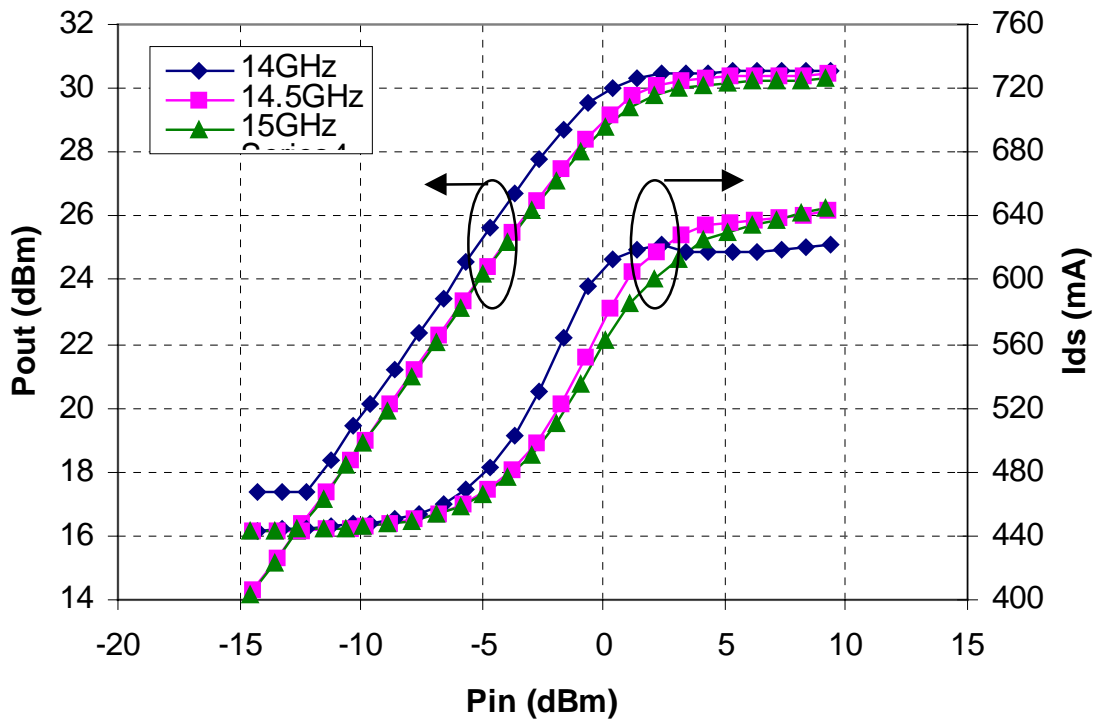
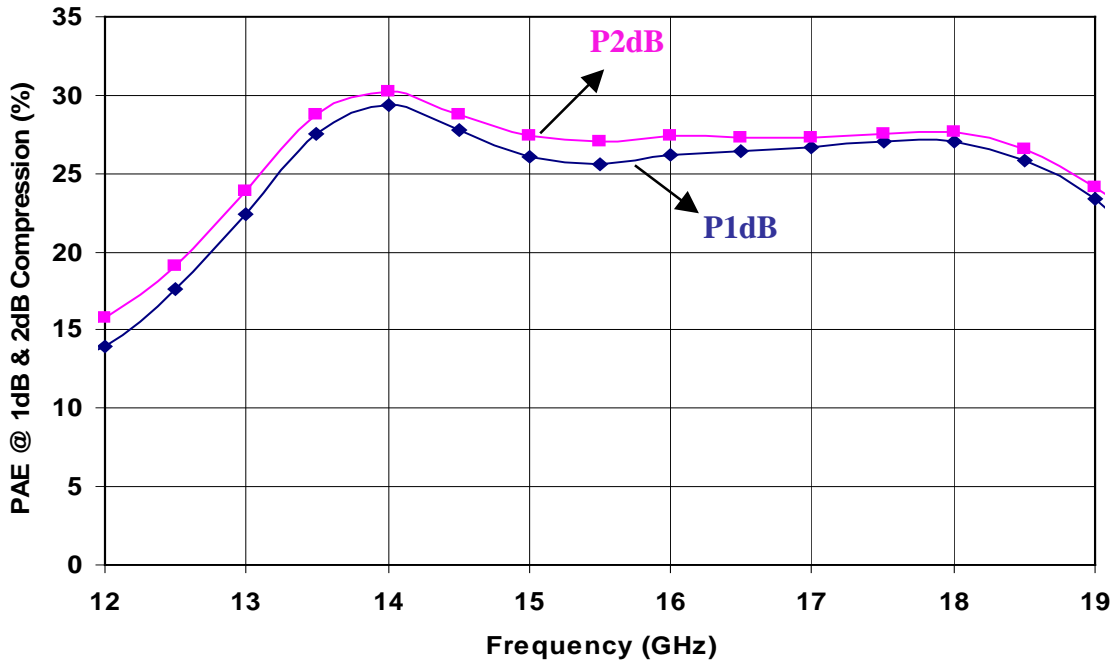
Frequency @ 15 GHz



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

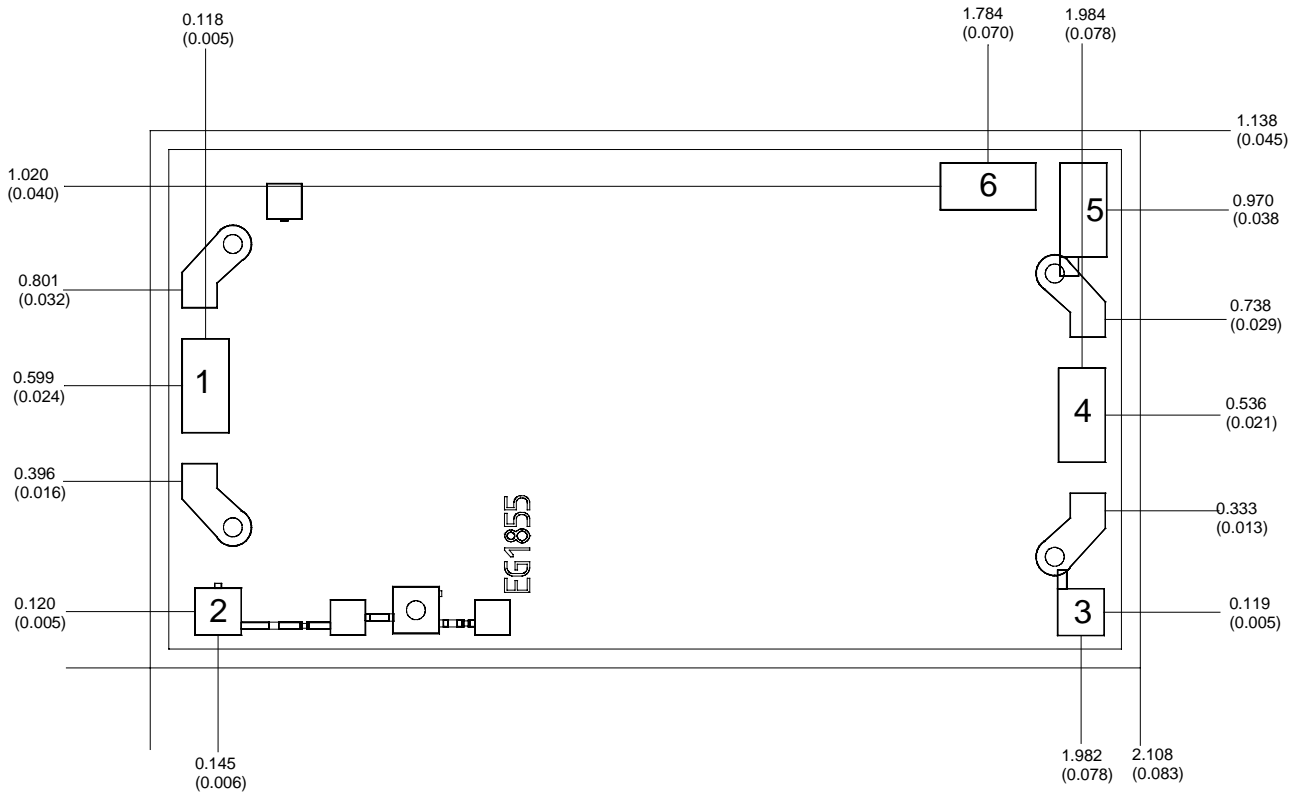
Preliminary Measured Data

Bias Conditions: $V_d = 7\text{ V}$, $I_d = 433\text{ mA}$



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Mechanical Drawing



Units: millimeters (inches)

Thickness: 0.100 (0.004)

Chip edge to bond pad dimensions are shown to center of bond pad

Chip size tolerance: +/- 0.051 (0.002)

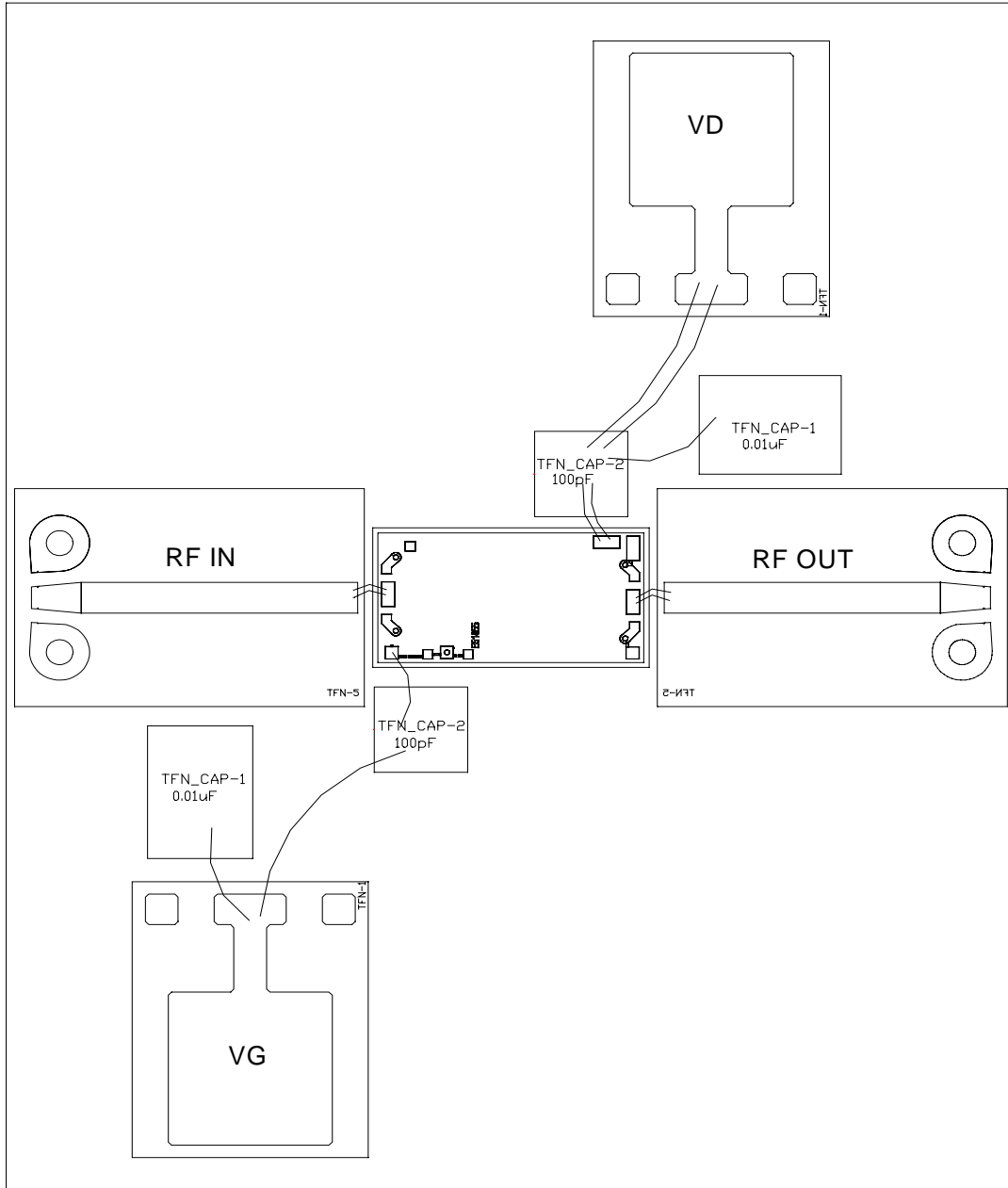
Bond pad #1:	(RF In)	0.098 x 0.199	(0.004 x 0.008)
Bond pad #2:	(Vg)	0.099 x 0.099	(0.004 x 0.004)
Bond pad #3:	(DC GND)*	0.098 x 0.099	(0.004 x 0.004)
Bond pad #4:	(RF Out)	0.099 x 0.198	(0.004 x 0.008)
Bond pad #5:	(DC GND)*	0.098 x 0.198	(0.004 x 0.008)
Bond pad #6:	(Vd)	0.202 x 0.098	(0.008 x 0.004)

* Note: RF GND is back side of MMIC.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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Chip Assembly Diagram



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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

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