

# NTMS5P02R2

## Power MOSFET -5.4 Amps, -20 Volts

### P-Channel Enhancement-Mode Single SOIC-8 Package

#### Features

- High Density Power MOSFET with Ultra Low  $R_{DS(on)}$  Providing Higher Efficiency
- Miniature SOIC-8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed with Soft Recovery
- $I_{DSS}$  Specified at Elevated Temperature
- Drain-to-Source Avalanche Energy Specified
- Mounting Information for the SOIC-8 Package is Provided
- Pb-Free Package is Available

#### Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

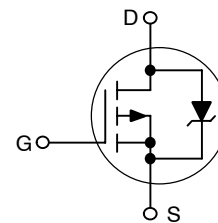


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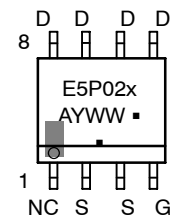
<http://onsemi.com>

$V_{DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
-20 V	26 mΩ @ -4.5 V	-5.4 A

#### Single P-Channel



#### MARKING DIAGRAM & PIN ASSIGNMENT



E5P02 = Specific Device Code  
 x = Blank or S  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

Device	Package	Shipping†
NTMS5P02R2	SOIC-8	2500/Tape & Reel
NTMS5P02R2G	SOIC-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

# NTMS5P02R2

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-20	V
Drain-to-Gate Voltage ( $R_{GS} = 1.0\text{ m}\Omega$ )	$V_{DGR}$	-20	V
Gate-to-Source Voltage - Continuous	$V_{GS}$	$\pm 10$	V
Thermal Resistance - Junction-to-Ambient (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Continuous Drain Current @ $25^\circ\text{C}$ Continuous Drain Current @ $70^\circ\text{C}$ Maximum Operating Power Dissipation Maximum Operating Drain Current Pulsed Drain Current (Note 4)	$R_{\theta JA}$ $P_D$ $I_D$ $I_D$ $P_D$ $I_D$ $I_{DM}$	50 2.5 -7.05 -5.62 1.2 -4.85 -28	$^\circ\text{C/W}$ W A A W A A
Thermal Resistance - Junction-to-Ambient (Note 2) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Continuous Drain Current @ $25^\circ\text{C}$ Continuous Drain Current @ $70^\circ\text{C}$ Maximum Operating Power Dissipation Maximum Operating Drain Current Pulsed Drain Current (Note 4)	$R_{\theta JA}$ $P_D$ $I_D$ $I_D$ $P_D$ $I_D$ $I_{DM}$	85 1.47 -5.40 -4.30 0.7 -3.72 -20	$^\circ\text{C/W}$ W A A W A A
Thermal Resistance - Junction-to-Ambient (Note 3) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Continuous Drain Current @ $25^\circ\text{C}$ Continuous Drain Current @ $70^\circ\text{C}$ Maximum Operating Power Dissipation Maximum Operating Drain Current Pulsed Drain Current (Note 4)	$R_{\theta JA}$ $P_D$ $I_D$ $I_D$ $P_D$ $I_D$ $I_{DM}$	159 0.79 -3.95 -3.15 0.38 -2.75 -12	$^\circ\text{C/W}$ W A A W A A
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = -20\text{ Vdc}$ , $V_{GS} = -5.0\text{ Vdc}$ , Peak $I_L = -8.5\text{ Apk}$ , $L = 10\text{ mH}$ , $R_G = 25\ \Omega$ )	$E_{AS}$	360	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided),  $t \leq 10$  seconds.
2. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided),  $t =$  steady state.
3. Minimum FR-4 or G-10 PCB,  $t =$  Steady State.
4. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 2%.

# NTMS5P02R2

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted) (Note 5)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = -250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	-20 -	- -15	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = -16 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 25°C) (V <sub>DS</sub> = -16 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C) (V <sub>DS</sub> = -20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 25°C)	I <sub>DSS</sub>	- - -	- - -0.2	-1.0 -10 -	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = -10 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	-100	nAdc
Gate-Body Leakage Current (V <sub>GS</sub> = +10 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	100	nAdc

### ON CHARACTERISTICS

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μAdc) Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	-0.65 -	-0.9 2.9	-1.25 -	Vdc mV/°C
Static Drain-to-Source On-State Resistance (V <sub>GS</sub> = -4.5 Vdc, I <sub>D</sub> = -5.4 Adc) (V <sub>GS</sub> = -2.5 Vdc, I <sub>D</sub> = -2.7 Adc)	R <sub>DS(on)</sub>	- -	0.026 0.037	0.033 0.048	Ω
Forward Transconductance (V <sub>DS</sub> = -9.0 Vdc, I <sub>D</sub> = -5.4 Adc)	g <sub>FS</sub>	-	15	-	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = -16 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>ISS</sub>	-	1375	1900	pF
Output Capacitance		C <sub>OSS</sub>	-	510	900	
Reverse Transfer Capacitance		C <sub>RSS</sub>	-	200	380	

### SWITCHING CHARACTERISTICS (Notes 6 & 7)

Turn-On Delay Time	(V <sub>DD</sub> = -16 Vdc, I <sub>D</sub> = -1.0 Adc, V <sub>GS</sub> = -4.5 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	18	35	ns
Rise Time		t <sub>r</sub>	-	25	50	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	70	125	
Fall Time		t <sub>f</sub>	-	55	100	
Turn-On Delay Time	(V <sub>DD</sub> = -16 Vdc, I <sub>D</sub> = -5.4 Adc, V <sub>GS</sub> = -4.5 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	22	-	ns
Rise Time		t <sub>r</sub>	-	70	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	65	-	
Fall Time		t <sub>f</sub>	-	90	-	
Total Gate Charge	(V <sub>DS</sub> = -16 Vdc, V <sub>GS</sub> = -4.5 Vdc, I <sub>D</sub> = -5.4 Adc)	Q <sub>tot</sub>	-	20	35	nC
Gate-Source Charge		Q <sub>gs</sub>	-	4.0	-	
Gate-Drain Charge		Q <sub>gd</sub>	-	7.0	-	

### BODY-DRAIN DIODE RATINGS (Note 6)

Diode Forward On-Voltage	(I <sub>S</sub> = -5.4 Adc, V <sub>GS</sub> = 0 V) (I <sub>S</sub> = -5.4 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- -	-0.95 -0.72	-1.25 -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = -5.4 Adc, V <sub>GS</sub> = 0 Vdc, diS/dt = 100 A/μs)	t <sub>rr</sub>	-	40	75	ns
		t <sub>a</sub>	-	20	-	
		t <sub>b</sub>	-	20	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.03	-	μC

5. Handling precautions to protect against electrostatic discharge is mandatory.
6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

# NTMS5P02R2

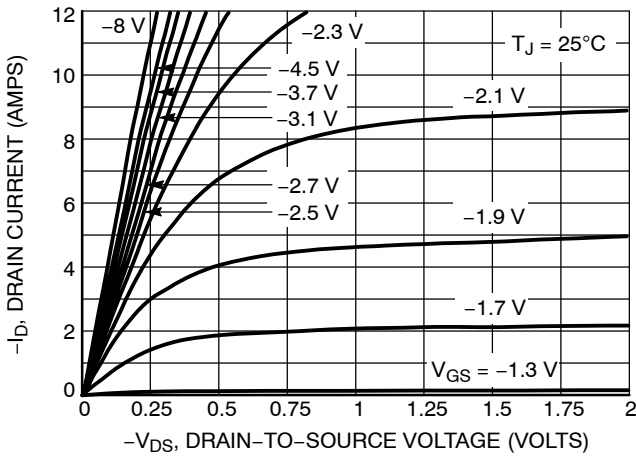


Figure 1. On-Region Characteristics

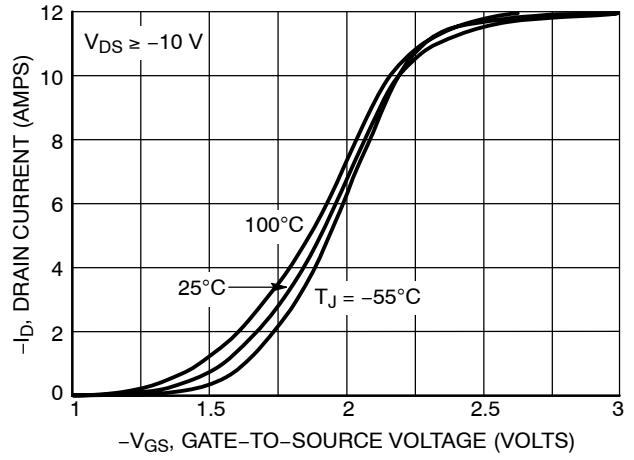


Figure 2. Transfer Characteristics

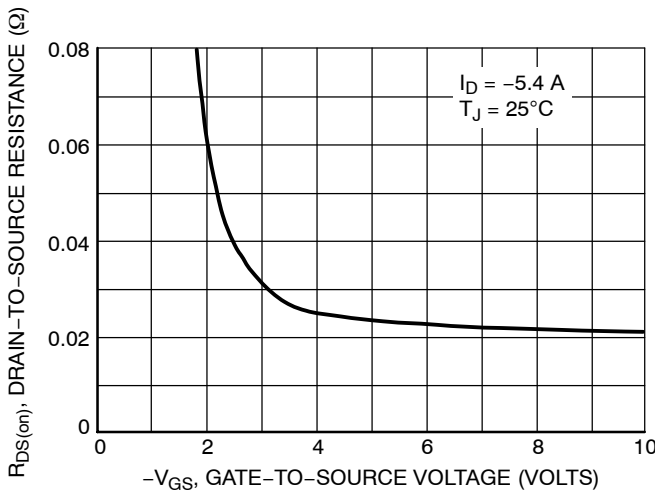


Figure 3. On-Resistance versus Gate-to-Source Voltage

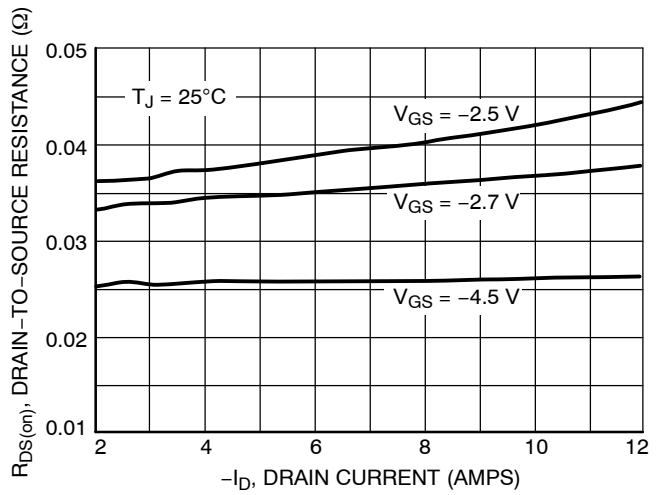


Figure 4. On-Resistance versus Drain Current and Gate Voltage

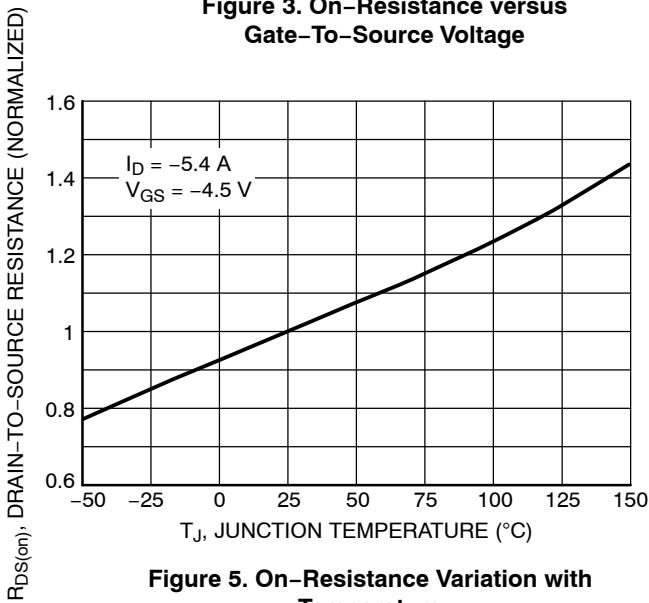


Figure 5. On-Resistance Variation with Temperature

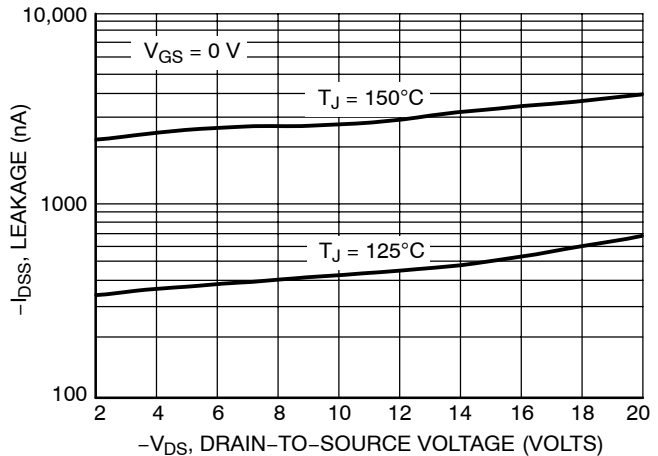


Figure 6. Drain-to-Source Leakage Current versus Voltage

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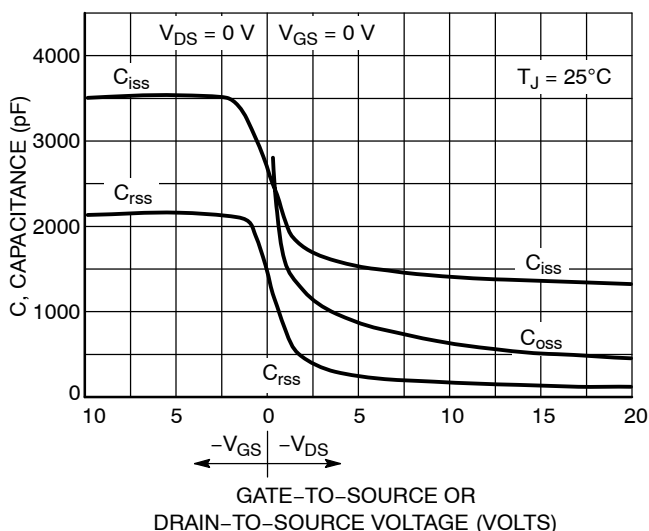


Figure 7. Capacitance Variation

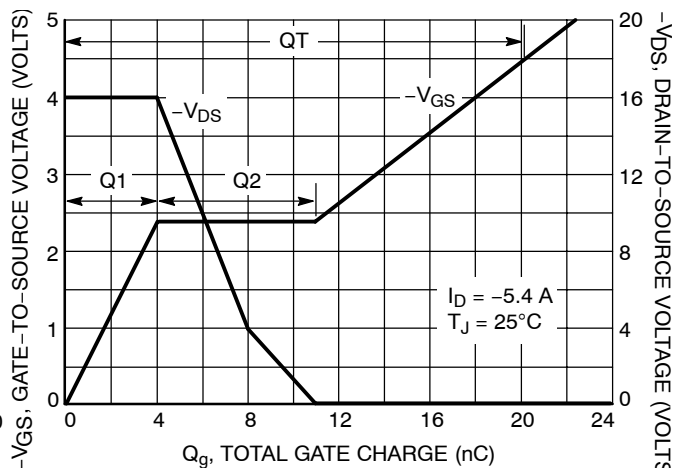


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

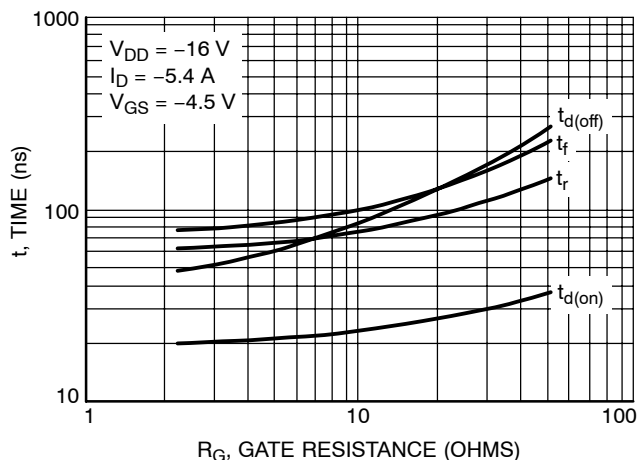


Figure 9. Resistive Switching Time Variation versus Gate Resistance

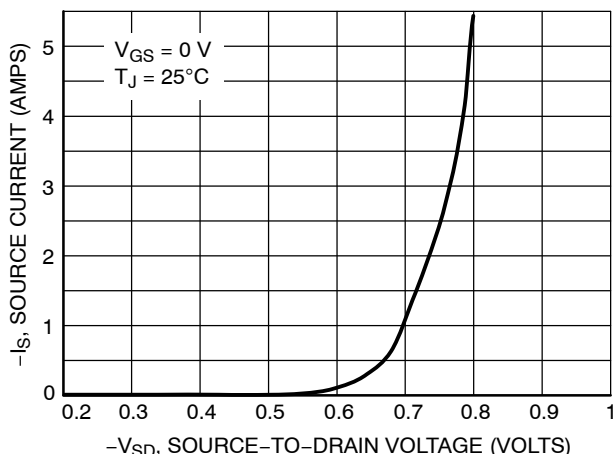


Figure 10. Diode Forward Voltage versus Current

## DRAIN-TO-SOURCE DIODE CHARACTERISTICS

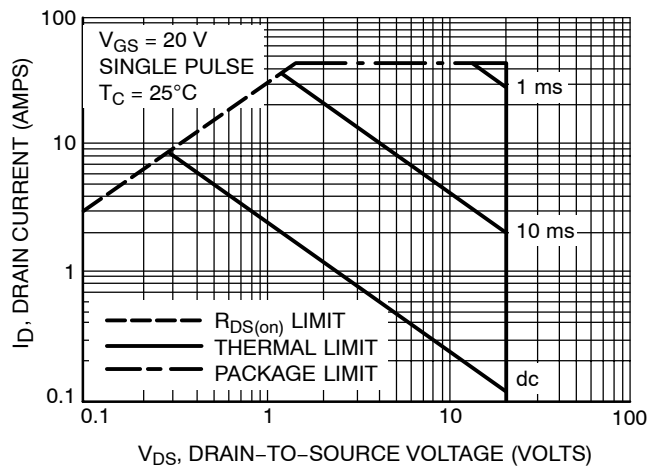


Figure 11. Maximum Rated Forward Biased Safe Operating Area

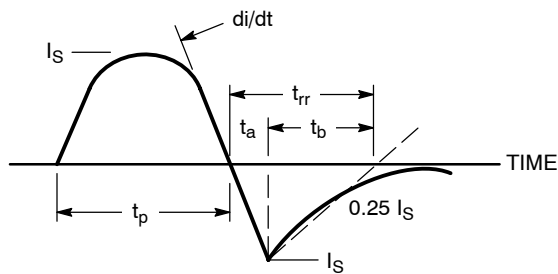


Figure 12. Diode Reverse Recovery Waveform

# NTMS5P02R2

## TYPICAL ELECTRICAL CHARACTERISTICS

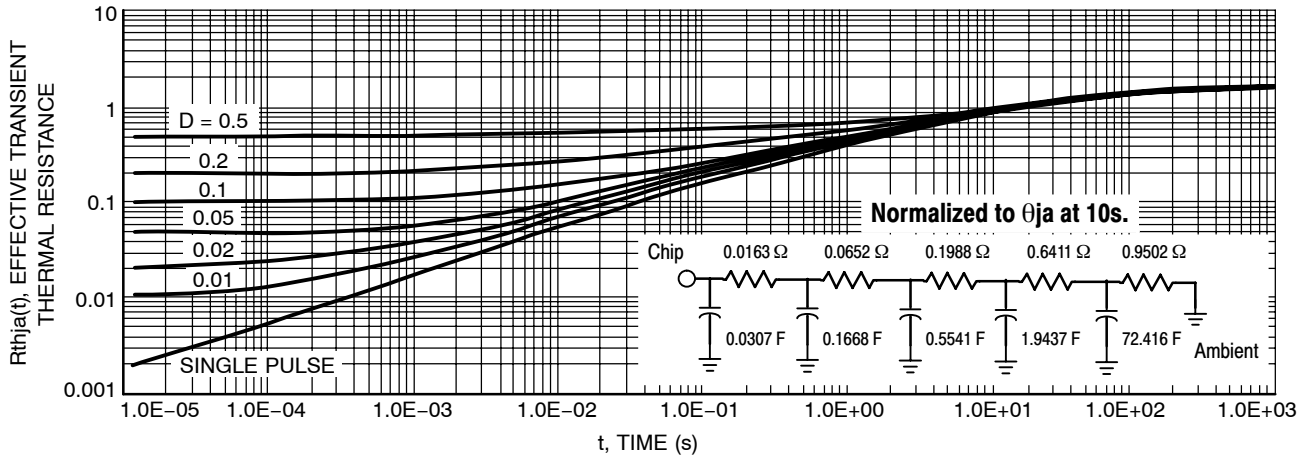
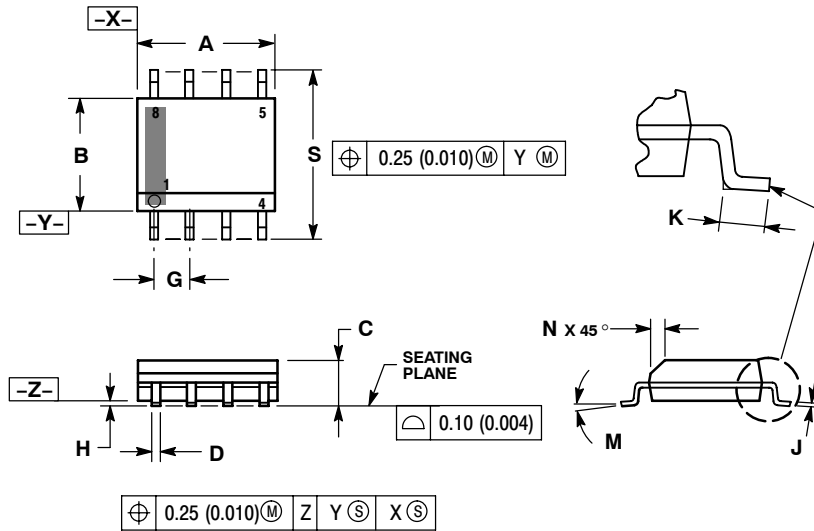


Figure 13. Thermal Response

# NTMS5P02R2

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AG



**NOTES:**

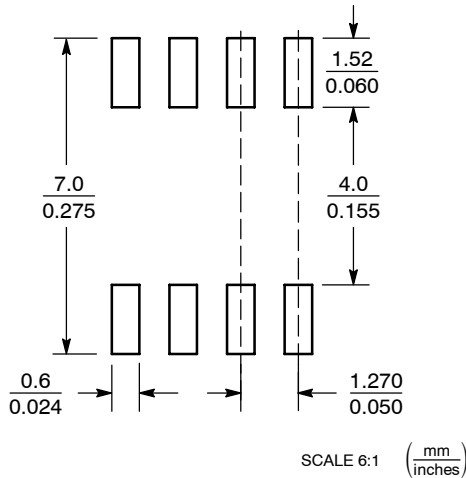
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

**STYLE 13:**

- PIN 1. N.C.
- 2. SOURCE
- 3. SOURCE
- 4. GATE
- 5. DRAIN
- 6. DRAIN
- 7. DRAIN
- 8. DRAIN

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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NTMS5P02R2/D