

# NTMS4404N

## Power MOSFET

30 V, 12 A, Single N-Channel, SO-8



ON Semiconductor®

<http://onsemi.com>

### Features

- High Density Power MOSFET with Ultra Low  $R_{DS(on)}$  for Higher Efficiency
- Miniature SO-8 Surface Mount Package Saving Board Space
- $I_{DSS}$  Specified at Elevated Temperature
- Diode Exhibits High Speed, Soft Recovery

### Applications

- Power Management for Battery Power Products
- Portable Products
- Computers, Printers, PCMCIA Cards
- Cell Phones, Cordless Telephones

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
30 V	9.7 m $\Omega$ @ 10 V	12 A
	15.5 m $\Omega$ @ 4.5 V	

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

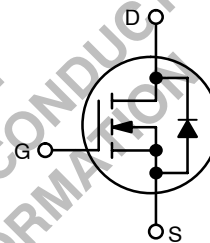
Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	30	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ 9.6	A
		$T_A = 70^\circ\text{C}$	7.6	
	$tp \leq 10$ s	$T_A = 25^\circ\text{C}$	12	
Power Dissipation (Note 1)	Steady State		$P_D$ 1.56	W
	$tp \leq 10$ s		2.5	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ 7.0	A
		$T_A = 70^\circ\text{C}$	5.6	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	$P_D$ 0.83	W
Pulsed Drain Current	$tp = 10$ $\mu\text{s}$ , DC = 2 %	$I_{DM}$ 50	A	
Operating Junction and Storage Temperature	$T_J$	-55 to	$^\circ\text{C}$	
	$T_{STG}$	150		
Source Current (Body Diode)	$I_S$	6.0	A	
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 20$ V, $V_{GS} = 5$ V, $I_{PK} = 7.25$ A, $L = 19$ mH, $R_G = 25$ $\Omega$ )	$E_{AS}$	500	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	80	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - $t = 10$ s (Note 1)	$R_{\theta JA}$	50	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	150	

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412 in sq.)

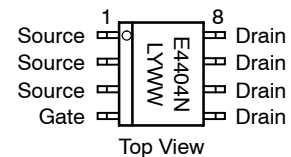
### N-Channel



### MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8  
CASE 751  
STYLE 12



Top View

E4404N = Device Code  
L = Assembly Location  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping†
NTMS4404NR2	SO-8	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTMS4404N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			25		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 100°C		5.0	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0	2.2	3.0	V
Gate Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-5.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A		9.7	11.5	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.0 A		15.5	17.5	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 12 A		17.5		S

## CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 24 V		1975	2500	pF
Output Capacitance	C <sub>OSS</sub>			575	750	
Reverse Transfer Capacitance	C <sub>RSS</sub>			180	300	
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 12 A		50	70	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			2.4		
Gate-to-Source Charge	Q <sub>GS</sub>			7.5		
Gate-to-Drain Charge	Q <sub>GD</sub>			16		

## SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 10 V (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 12 A, R <sub>G</sub> = 2.5 Ω		15	25	ns
Rise Time	t <sub>r</sub>			25	50	
Turn-Off Delay Time	t <sub>d(OFF)</sub>			35	55	
Fall Time	t <sub>f</sub>			15	30	

## SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 4.5 V (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 6.0 A, R <sub>G</sub> = 2.5 Ω		20		ns
Rise Time	t <sub>r</sub>			80		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			25		
Fall Time	t <sub>f</sub>			15		

## DRAIN-SOURCE DIODE CHARACTERISTICS (Note 4)

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 6.0 A	T <sub>J</sub> = 25°C	0.80	1.1	V
			T <sub>J</sub> = 125°C	0.65		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>SD</sub> /dt = 100 A/μs, I <sub>S</sub> = 6.0 A		40	55	ns
Charge Time	t <sub>a</sub>			23		
Discharge Time	t <sub>b</sub>			17		
Reverse Recovery Charge	Q <sub>RR</sub>			0.05		

## NOTES:

- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

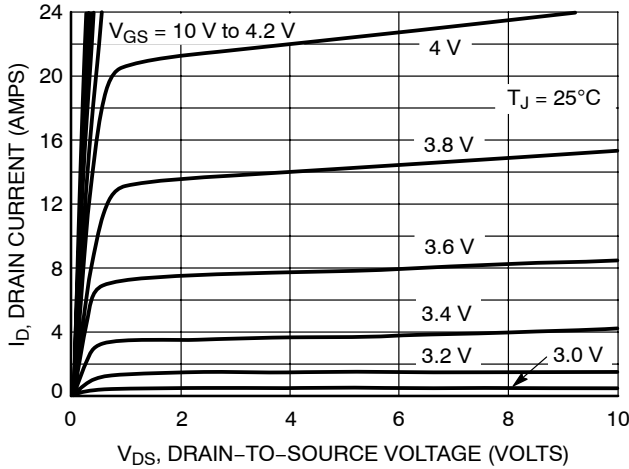


Figure 1. On-Region Characteristics

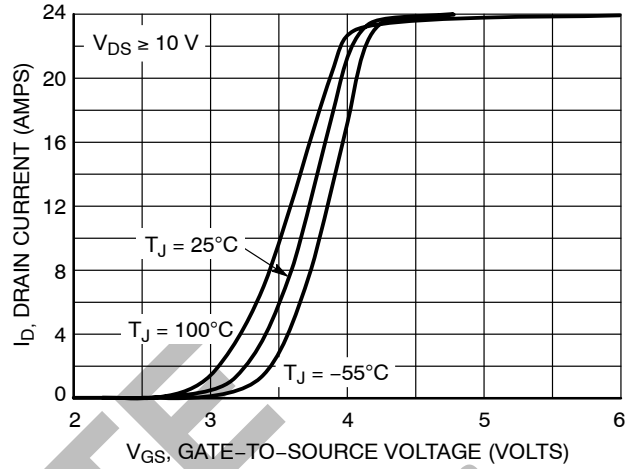


Figure 2. Transfer Characteristics

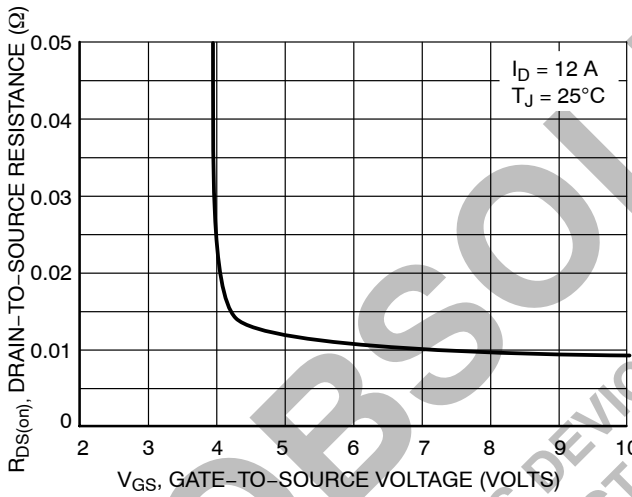


Figure 3. On-Resistance vs. Gate-to-Source Voltage

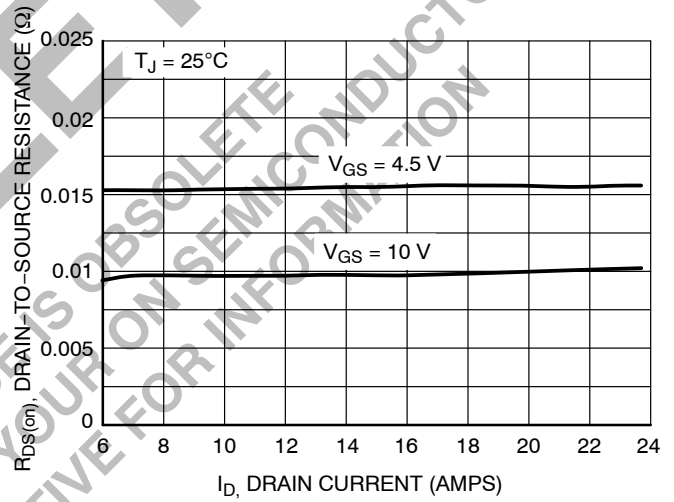


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

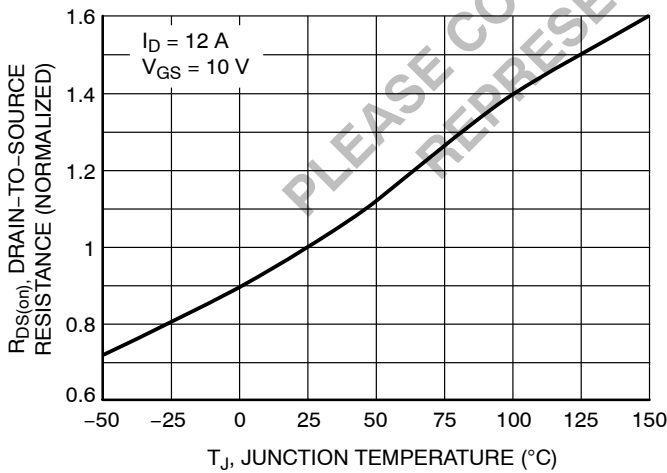


Figure 5. On-Resistance Variation with Temperature

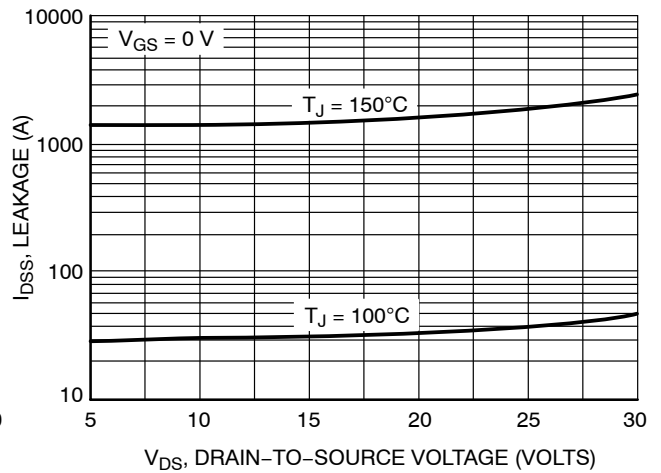
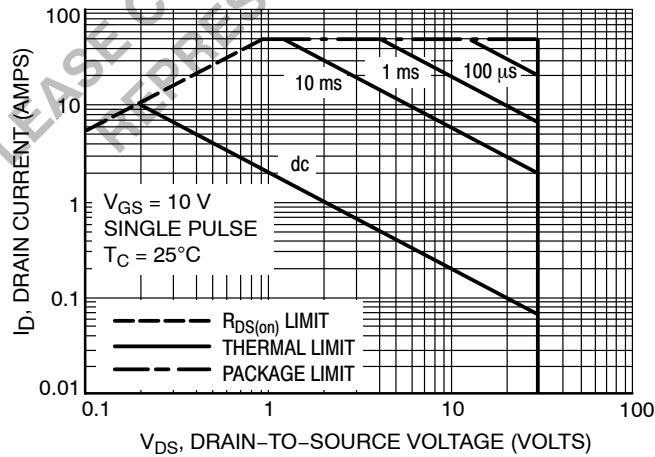
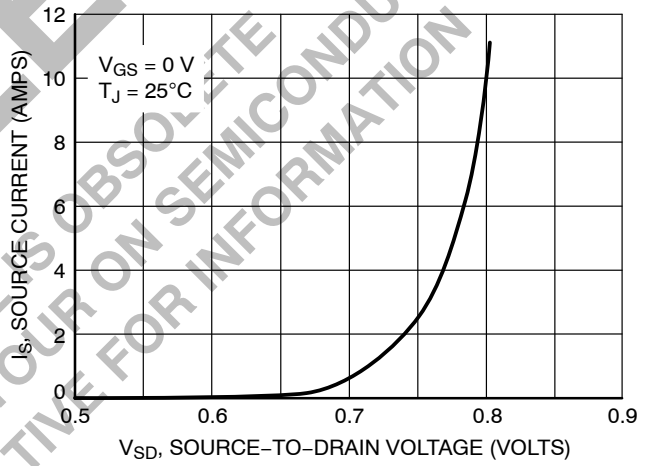
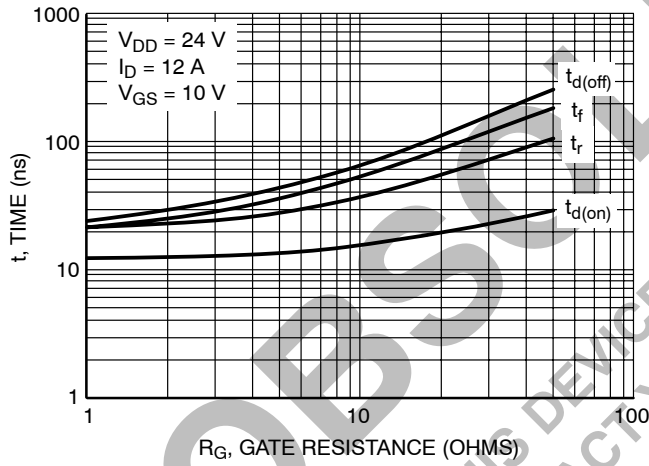
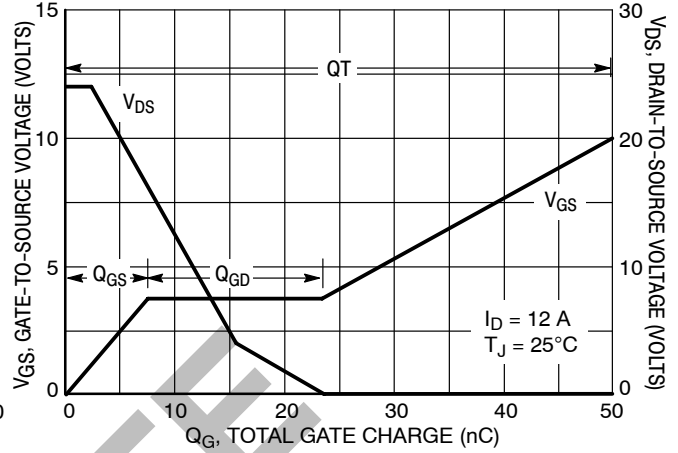
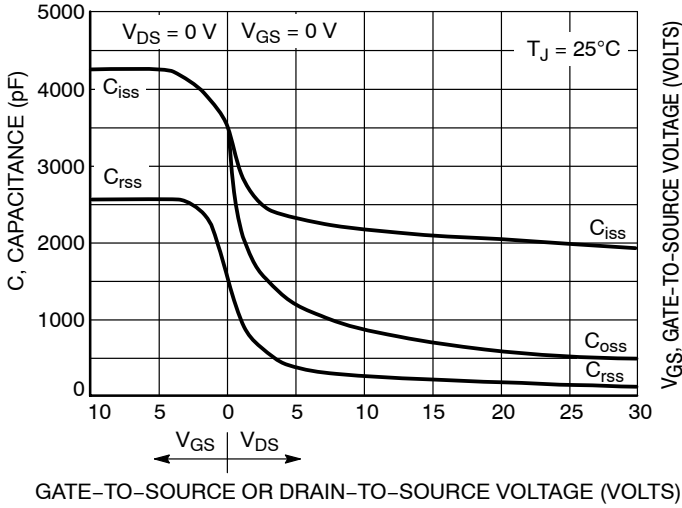


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES



# NTMS4404N

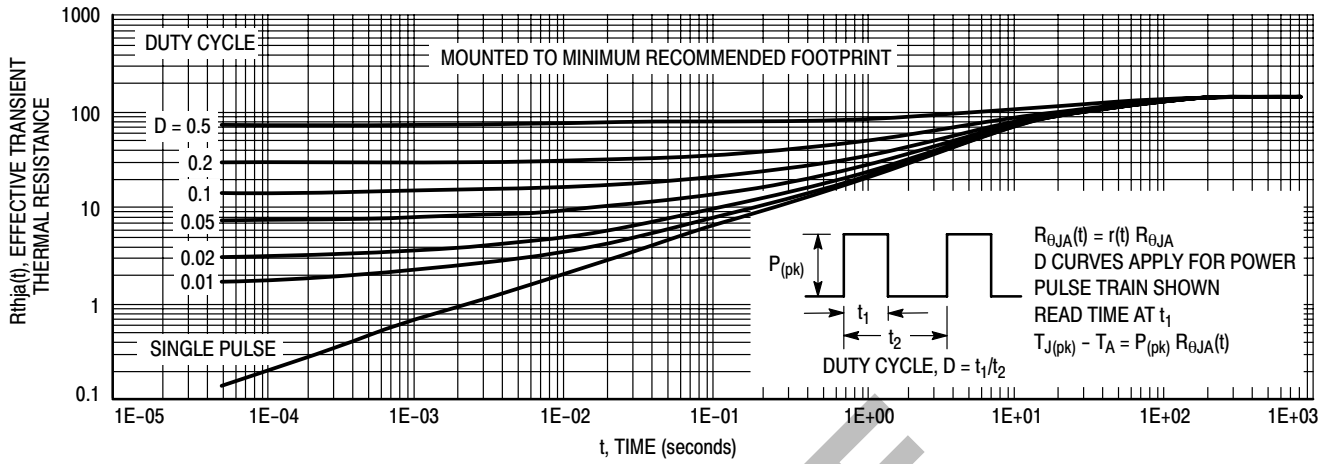


Figure 12. Thermal Response – Various Duty Cycles

OBSOLETE

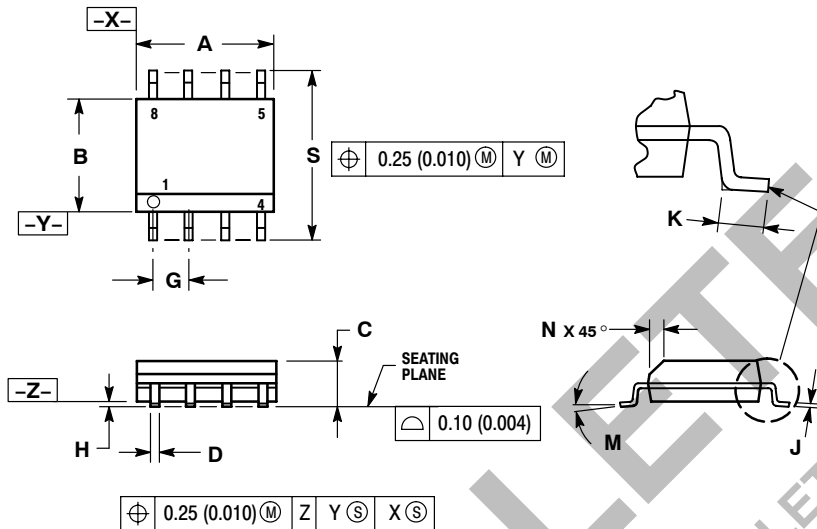
THIS DEVICE IS OBSOLETE

PLEASE CONTACT YOUR ON SEMICONDUCTOR REPRESENTATIVE FOR INFORMATION

# NTMS4404N

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AA



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

**STYLE 12:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.

**NTMS4404N/D**