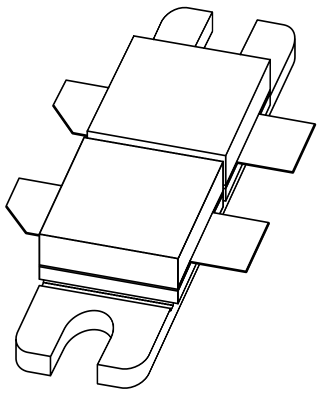
DATA SHEET



BLF278
VHF push-pull power MOS transistor

Product Specification
Supersedes data of 1996 Oct 21

2003 Sep 19

Philips
Semiconductors

PHILIPS

VHF push-pull power MOS transistor BLF278

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Broadcast transmitters in the VHF frequency range.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor encapsulated in a 4-lead, SOT262A1 balanced flange package with two ceramic caps. The mounting flange provides the common source connection for the transistors.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

PINNING - SOT262A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

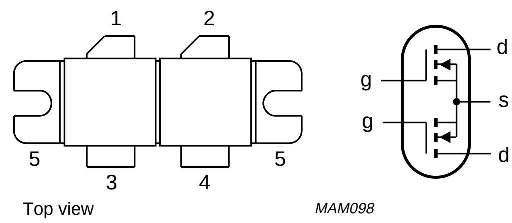


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	300	>20	>60
CW, class-C	108	50	300	typ. 18	typ. 80
CW, class-AB	225	50	250	>14 typ. 16	>50 typ. 55

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

VHF push-pull power MOS transistor BLF278

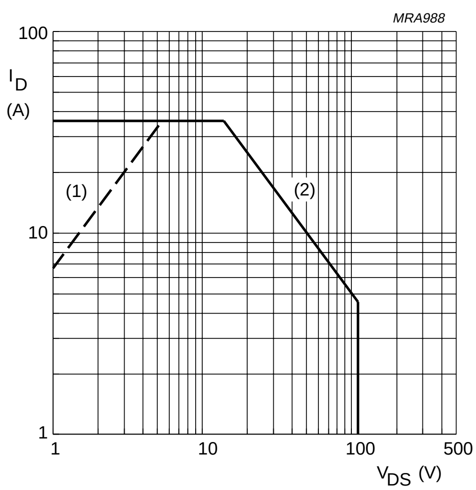
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section					
V_{DS}	drain-source voltage		–	125	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	18	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C; total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded.	max. 0.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded.	max. 0.15	K/W

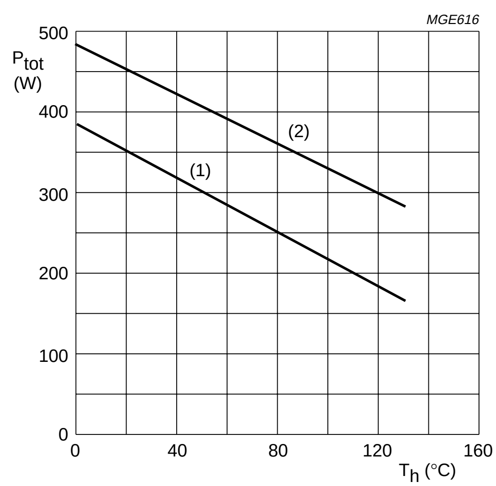


Total device; both sections equally loaded.

(1) Current is this area may be limited by R_{DSon}.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



Total device; both sections equally loaded.

(1) Continuous operation.

(2) Short-time operation during mismatch.

Fig.3 Power derating curves.

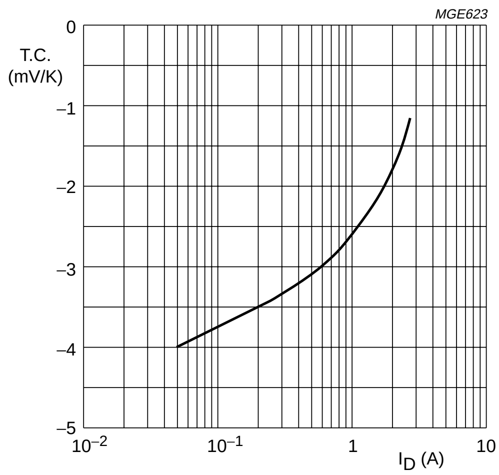
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 100 mA	125	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 50 mA	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both sections	V_{DS} = 10 V; I_D = 50 mA	–	–	100	mV
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5 A	4.5	6.2	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both sections	V_{DS} = 10 V; I_D = 5 A	0.9	–	1.1	
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	0.2	0.3	Ω
I_{DSX}	drain cut-off current	V_{GS} = 10 V; V_{DS} = 10 V	–	25	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	14	–	pF
C_{d-f}	drain-flange capacitance		–	5.4	–	pF

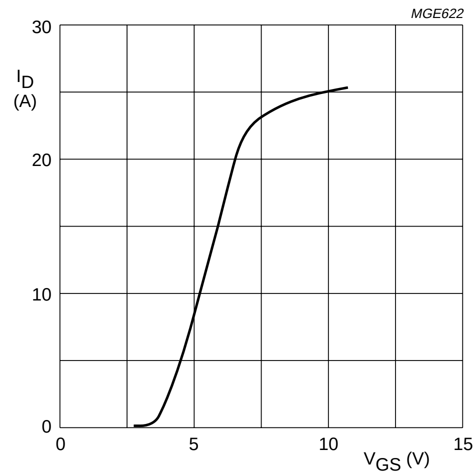
V_{GS} group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			



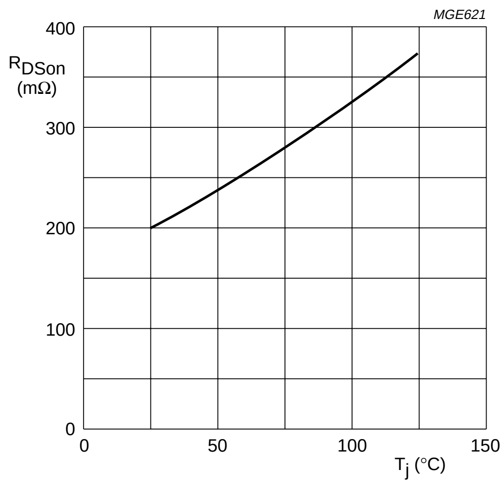
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values per section.



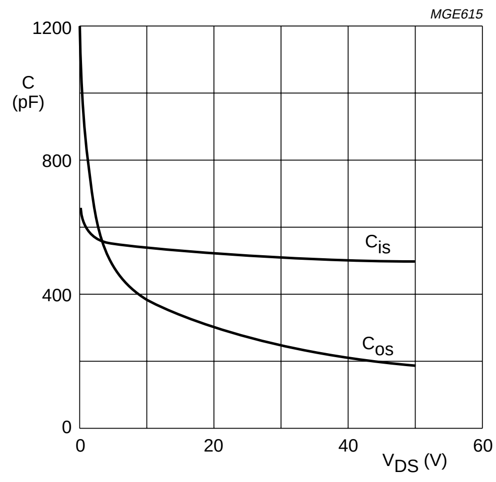
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values per section.



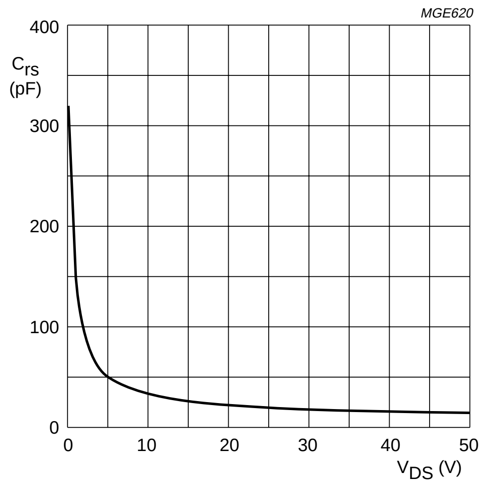
V_{GS} = 10 V; I_D = 5 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values per section.

APPLICATION INFORMATION

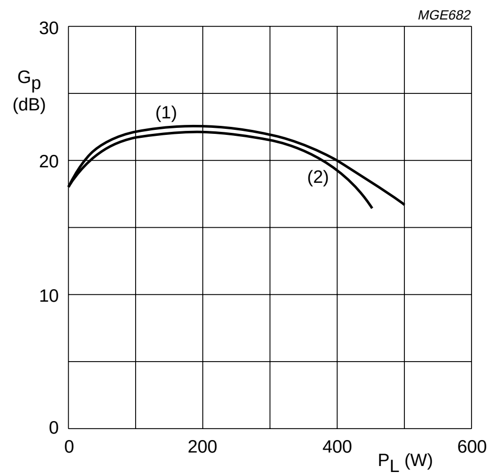
Class-B operation

RF performance in CW operation in a common source push-pull test circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W unless otherwise specified. R_{GS} = 4 Ω per section; optimum load impedance per section = 3.2 + j4.3 Ω (V_{DS} = 50 V).

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	2 × 0.1	300	>20 typ. 22	>60 typ. 70
CW, class-C	108	50	V_{GS} = 0	300	typ. 18	typ. 80

Ruggedness in class-B operation

The BLF278 is capable of withstanding a load mismatch corresponding to VSWR = 7:1 through all phases under the following conditions: V_{DS} = 50 V; f = 108 MHz at rated load power.

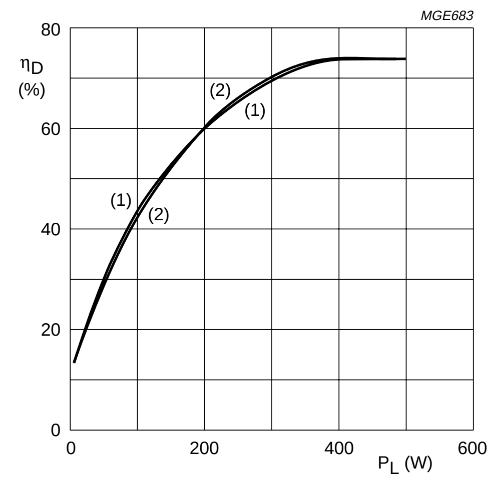


Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A; f = 108 MHz;
Z_L = 3.2 + j4.3 Ω (per section); R_{GS} = 4 Ω (per section).

(1) T_h = 25 °C.

(2) T_h = 70 °C.

Fig.9 Power gain as a function of load power; typical values.

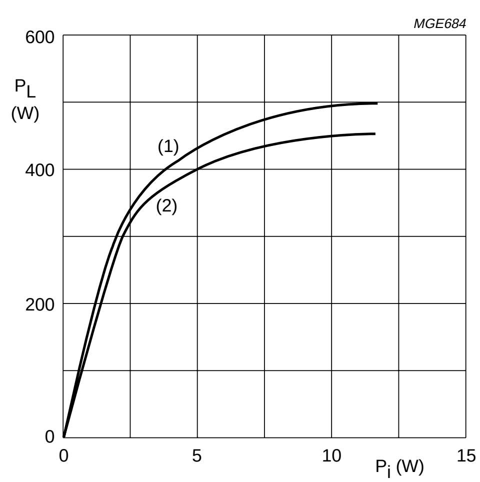


Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A; f = 108 MHz;
Z_L = 3.2 + j4.3 Ω (per section); R_{GS} = 4 Ω (per section).

(1) T_h = 25 °C.

(2) T_h = 70 °C.

Fig.10 Efficiency as a function of load power; typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A; f = 108 MHz;
Z_L = 3.2 + j4.3 Ω (per section); R_{GS} = 4 Ω (per section).

(1) T_h = 25 °C.

(2) T_h = 70 °C.

Fig.11 Load power as a function of input power; typical values.

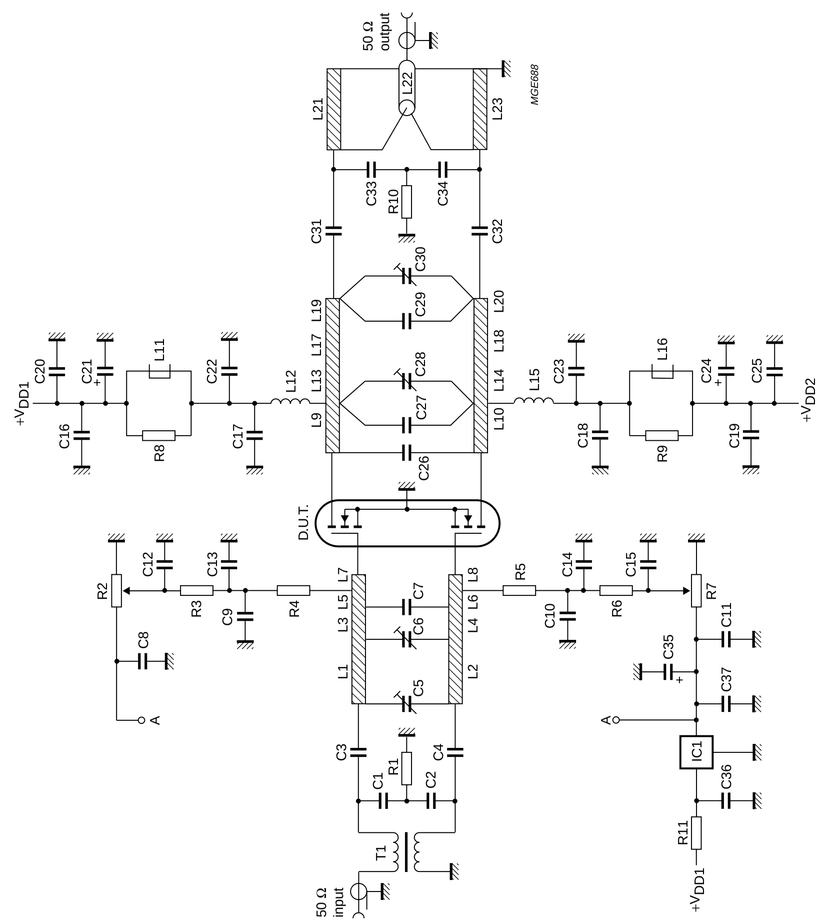


Fig.12 Class-B test circuit at f = 108 MHz.

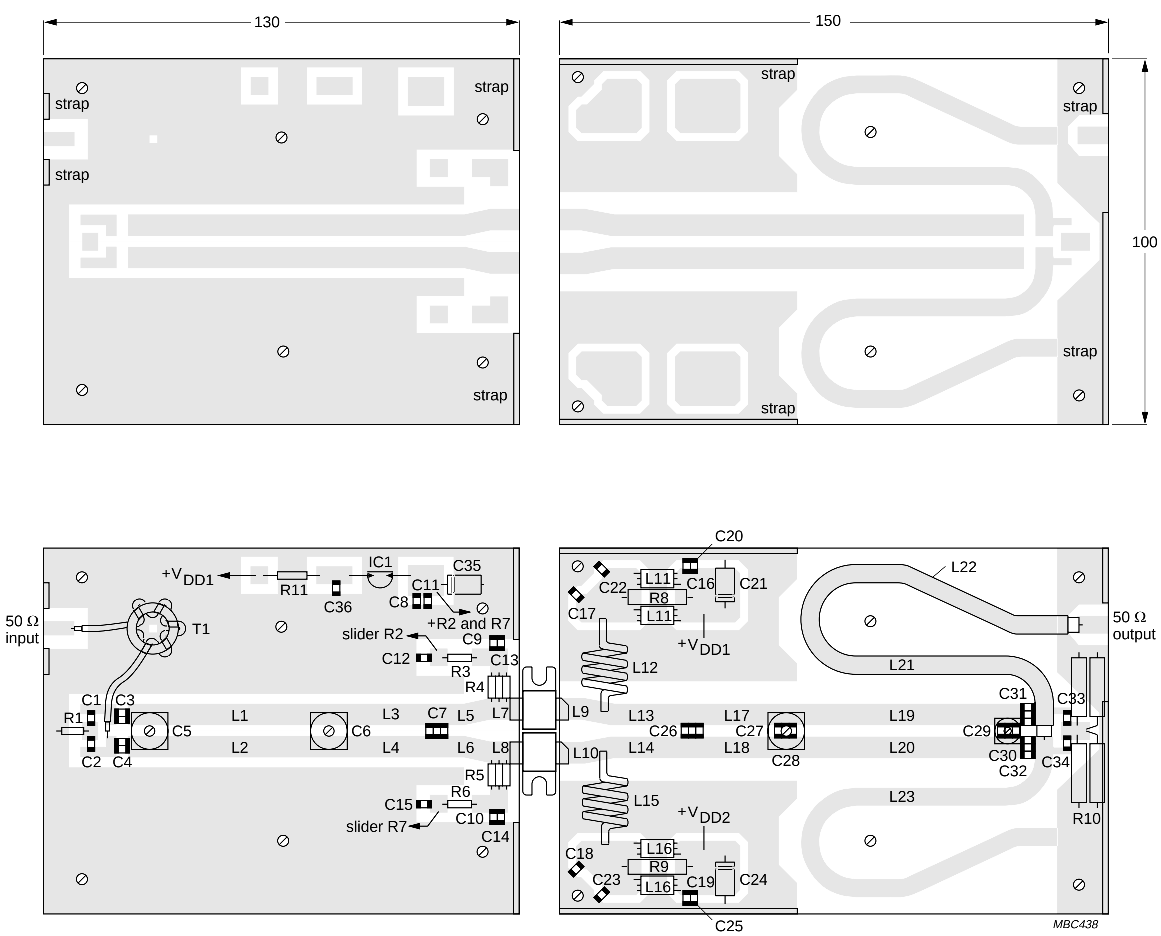
List of components (see Figs 12 and 13)**.**

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C33, C34	multilayer ceramic chip capacitor; note 1	22 pF, 500 V		
C3, C4	multilayer ceramic chip capacitor; note 1	100 pF + 68 pF in parallel, 500 V		
C5, C6, C28	film dielectric trimmer	5 to 60 pF		2222 809 08003
C7	multilayer ceramic chip capacitor; note 1	2 × 100 pF + 1 × 120 pF in parallel, 500 V		
C8, C11, C12, C15, C16, C19, C36	multilayer ceramic chip capacitor	100 nF, 500 V		2222 852 47104
C9, C10, C13, C14, C20, C25	multilayer ceramic chip capacitor; note 1	1 nF, 500 V		
C17, C18, C22, C23	multilayer ceramic chip capacitor; note 1	470 pF, 500 V		
C21, C24, C35	electrolytic capacitor	10 μF, 63 V		
C26	multilayer ceramic chip capacitor; note 1	2 × 15 pF + 1 × 18 pF in parallel, 500 V		
C27	multilayer ceramic chip capacitor; note 1	3 × 15 pF in parallel, 500 V		
C29	multilayer ceramic chip capacitor; note 1	2 × 18 pF + 1 × 15 pF in parallel, 500 V		
C30	film dielectric trimmer	2 to 18 pF		2222 809 09006
C31, C32	multilayer ceramic chip capacitor; note 1	3 × 43 pF in parallel, 500 V		
L1, L2	stripline; note 2	43 Ω	length 57.5 mm width 6 mm	
L3, L4	stripline; note 2	43 Ω	length 29.5 mm width 6 mm	
L5, L6	stripline; note 2	43 Ω	length 14 mm width 6 mm	
L7, L8	stripline; note 2	43 Ω	length 6 mm width 6 mm	
L9, L10	stripline; note 2	43 Ω	length 17.5 mm width 6 mm	
L11, L16	2 × grade 3B Ferroxcube wideband HF chokes in parallel			4312 020 36642
L12, L15	4 turns enamelled 2 mm copper wire	85 nH	length 13.5 mm int. dia. 10 mm leads 2 × 7 mm	
L13, L14	stripline; note 2	43 Ω	length 19.5 mm width 6 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L17, L18	stripline; note 2	43 Ω	length 24.5 mm width 6 mm	
L19, L20	stripline; note 2	43 Ω	length 66 mm width 6 mm	
L21, L23	stripline; note 2	50 Ω	length 160 mm width 4.8 mm	
L22	semi-rigid cable; note 3	50 Ω	ext. dia. 3.6 mm outer conductor length 160 mm	
R1	metal film resistor	10 Ω, 0.4 W		
R2, R7	10 turn potentiometer	50 kΩ		
R3, R6	metal film resistor	3 × 12.1 Ω in parallel, 0.4 W		
R4, R5	metal film resistor	10 Ω; 0.4 W		
R8, R9	metal film resistor	10 Ω ±5%, 1 W		
R10	metal film resistor	4 × 10 Ω in parallel, 1 W		
R11	metal film resistor	5.11 kΩ, 1 W		
IC1	voltage regulator 78L05			
T1	1:1 Balun; 7 turns type 4C6 50 Ω coaxial cable wound around toroid		14 × 9 × 5 mm	4322 020 90770

Notes

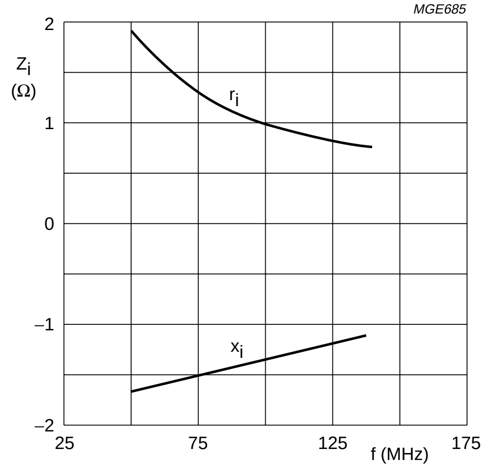
1. American Technical Ceramics capacitor, type 100B or capacitor of same quality.
2. L1 to L10, L13, L14, L17 to L21 and L23 are striplines on a double copper-clad printed-circuit board, with fibre-glass PTFE dielectric (ε_r = 2.2), thickness $^1/_{16}$ inch; thickness of copper sheet 2 × 35 μm.
3. L22 is soldered on to stripline L21.



Dimensions in mm.

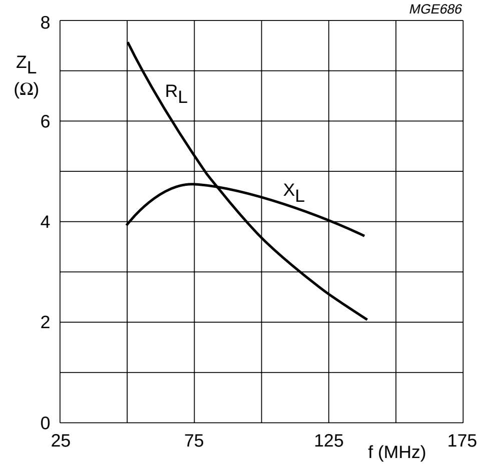
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by means of copper straps for a direct contact between upper and lower sheets.

Fig.13 Printed-circuit board and component layout for 108 MHz class-B test circuit.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A;
R_{GS} = 4 Ω (per section); P_L = 300 W.

Fig.14 Input impedance as a function of frequency (series components); typical values per section.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A;
R_{GS} = 4 Ω (per section); P_L = 300 W.

Fig.15 Load impedance as a function of frequency (series components); typical values per section.

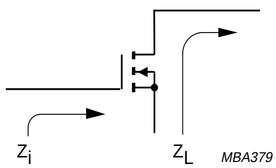
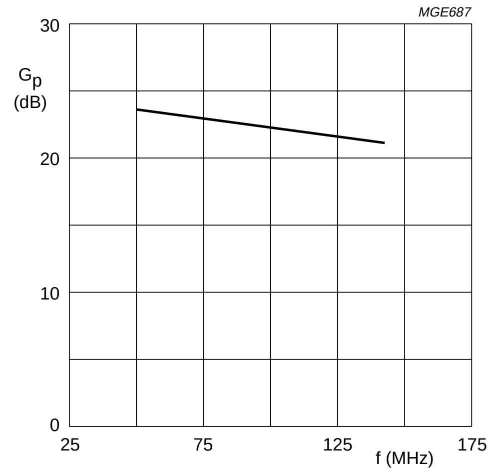


Fig.16 Definition of MOS impedance.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.1 A;
R_{GS} = 4 Ω (per section); P_L = 300 W.

Fig.17 Power gain as a function of frequency; typical values per section.

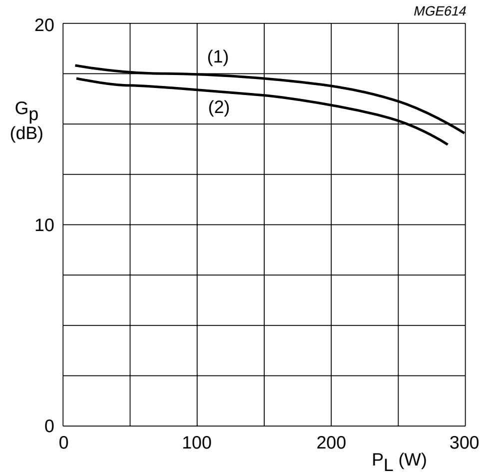
Class-AB operation

RF performance in CW operation in a common source push-pull test circuit. T_h = 25 °C; $R_{th\ mb-h}$ = 0.15 K/W unless otherwise specified. R_{GS} = 2.8 Ω per section; optimum load impedance per section = 0.74 + j2 Ω; (V_{DS} = 50 V).

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	225	50	2 × 0.5	250	>14 typ. 16	>50 typ. 55

Ruggedness in class-AB operation

The BLF278 is capable of withstanding a load mismatch corresponding to VSWR = 7:1 through all phases under the following conditions: V_{DS} = 50 V; f = 225 MHz at rated output power.

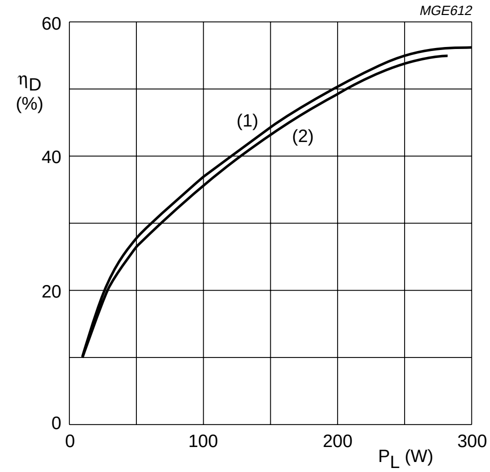


Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A; f = 225 MHz;
Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section).

(1) T_h = 25 °C.

(2) T_h = 70 °C.

Fig.18 Power gain as a function of load power; typical values.

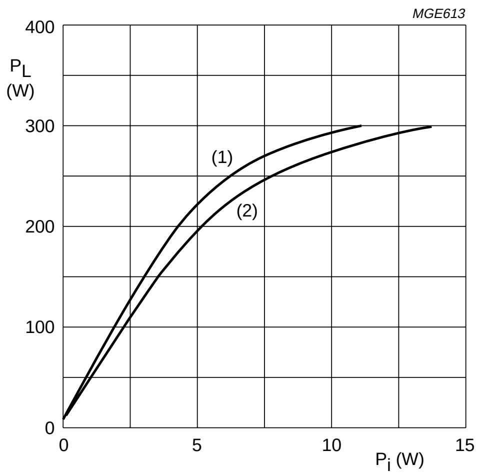


Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A; f = 225 MHz;
Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section).

(1) T_h = 25 °C.

(2) T_h = 70 °C.

Fig.19 Efficiency as a function of load power; typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A; f = 225 MHz;
Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section).

(1) T_h = 25 °C.

(2) T_h = 70 °C.

Fig.20 Load power as a function of input power; typical values.

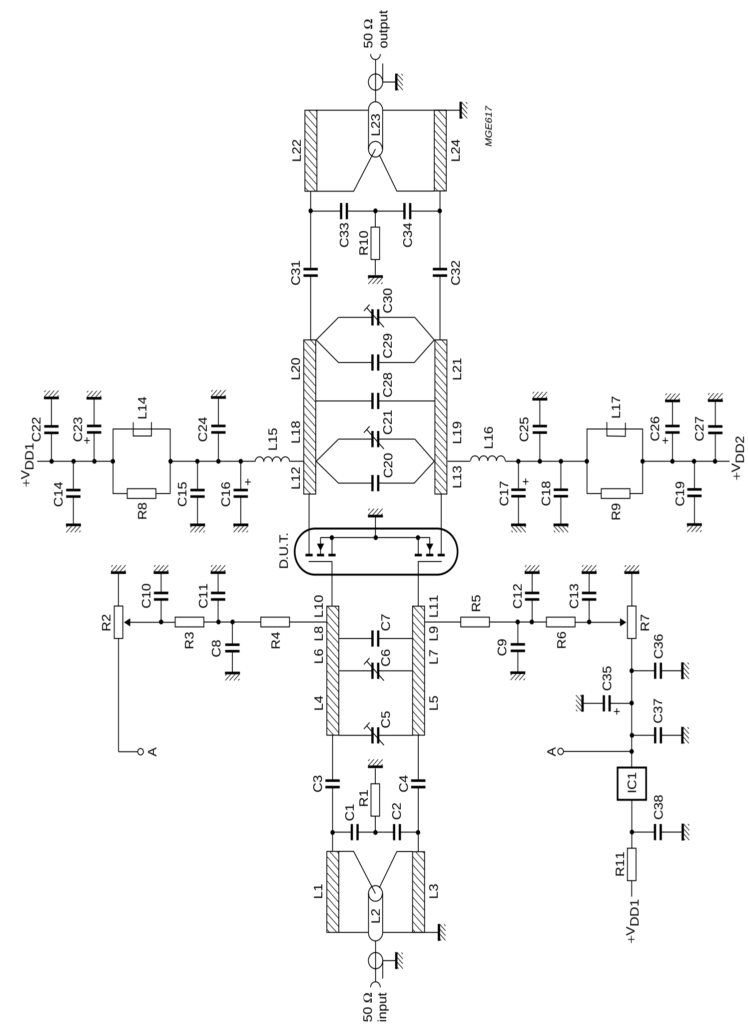


Fig.21 Class-AB test circuit at f = 225 MHz.

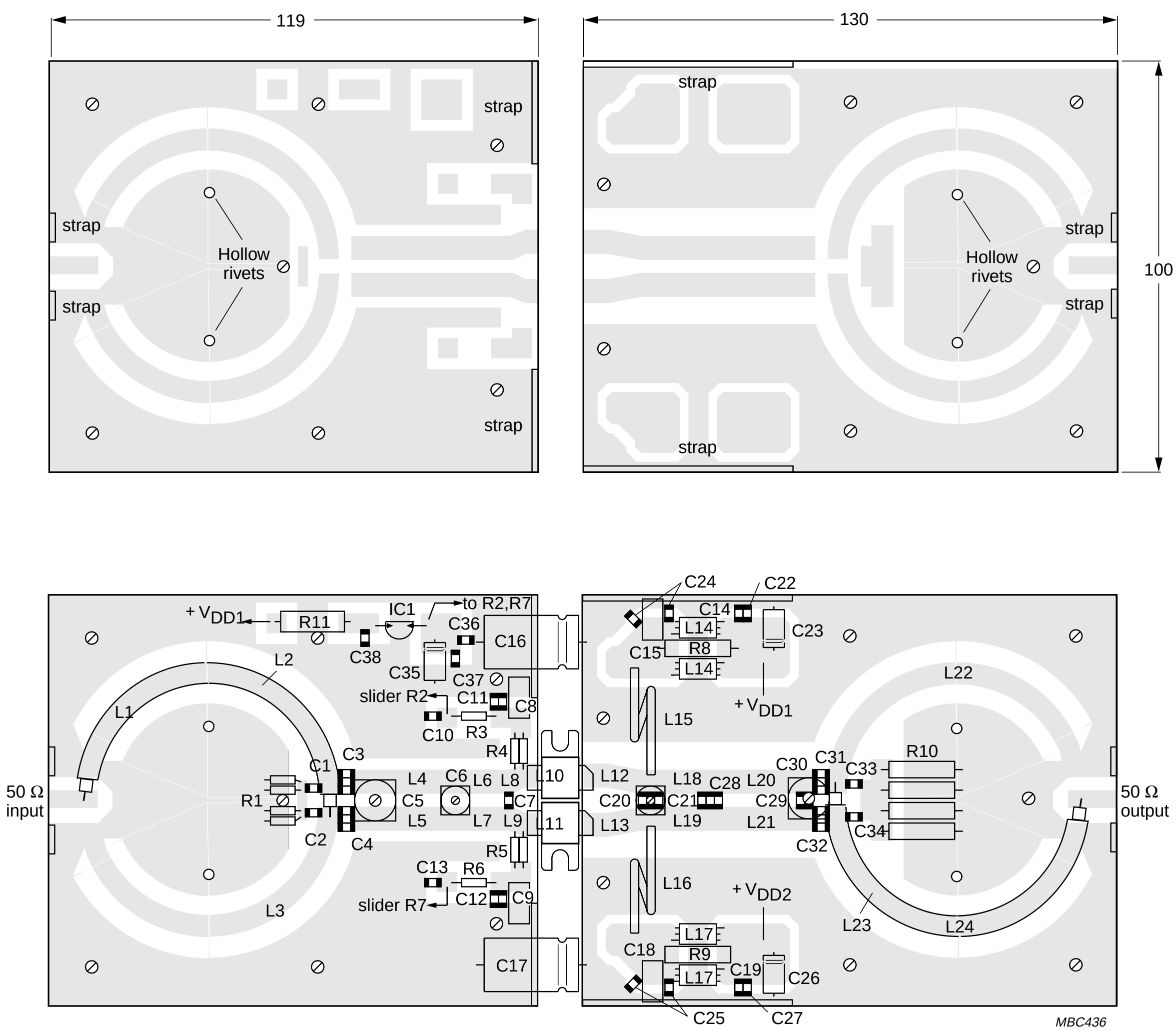
List of components (see Figs 21 and 22).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	27 pF, 500 V		
C3, C4, C31, C32	multilayer ceramic chip capacitor; note 1	3 × 18 pF in parallel, 500 V		
C5	film dielectric trimmer	4 to 40 pF		2222 809 08002
C6, C30	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7	multilayer ceramic chip capacitor; note 1	100 pF, 500 V		
C8, C9, C15, C18	MKT film capacitor	1 μF, 63 V		2222 371 11105
C10, C13, C14, C19, C36	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C11, C12	multilayer ceramic chip capacitor; note 1	2 × 1 nF in parallel, 500 V		
C16, C17	electrolytic capacitor	220 μF, 63 V		
C20	multilayer ceramic chip capacitor; note 1	3 × 33 pF in parallel, 500 V		
C21	film dielectric trimmer	2 to 9 pF		2222 809 09005
C22, C27, C37, C38	multilayer ceramic chip capacitor; note 1	1 nF, 500 V		
C23, C26, C35	electrolytic capacitor	10 μF, 63 V		
C24, C25	multilayer ceramic chip capacitor; note 1	2 × 470 pF in parallel, 500 V		
C28	multilayer ceramic chip capacitor; note 1	2 × 10 pF + 1 × 18 pF in parallel, 500 V		
C29	multilayer ceramic chip capacitor; note 1	2 × 5.6 pF in parallel, 500 V		
C33, C34	multilayer ceramic chip capacitor; note 1	5.6 pF, 500 V		
L1, L3, L22, L24	stripline; note 2	50 Ω	length 80 mm width 4.8 mm	
L2, L23	semi-rigid cable; note 3	50 Ω	ext. dia. 3.6 mm outer conductor length 80 mm	
L4, L5	stripline; note 2	43 Ω	length 24 mm width 6 mm	
L6, L7	stripline; note 2	43 Ω	length 14.5 mm width 6 mm	
L8, L9	stripline; note 2	43 Ω	length 4.4 mm width 6 mm	
L10, L11	stripline; note 2	43 Ω	length 3.2 mm width 6 mm	
L12, L13	stripline; note 2	43 Ω	length 15 mm width 6 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L14, L17	2 × grade 3B Ferroxcube wideband HF chokes in parallel			4312 020 36642
L15, L16	1¾ turns enamelled 2 mm copper wire	40 nH	int. dia. 10 mm leads 2 × 7 mm space 1 mm	
L18, L19	stripline; note 2	43 Ω	length 13 mm width 6 mm	
L20, L21	stripline; note 2	43 Ω	length 29.5 mm width 6 mm	
R1	metal film resistor	10 Ω, 0.4 W		
R2, R7	10 turns potentiometer	50 kΩ		
R3, R6	metal film resistor	1 kΩ, 0.4 W		
R4, R5	metal film resistor	2 × 5.62 Ω, in parallel, 0.4 W		
R8, R9	metal film resistor	10 Ω ±5%, 1 W		
R10	metal film resistor	4 × 42.2 Ω in parallel, 1 W		
R11	metal film resistor	5.11 kΩ, 1 W		
IC1	voltage regulator 78L05			

Notes

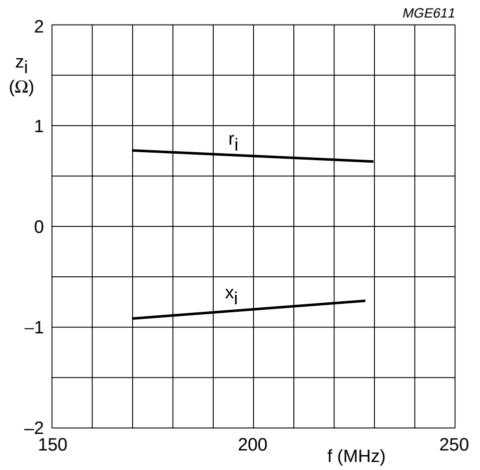
1. American Technical Ceramics capacitor, type 100B or other capacitor of the same quality.
2. L1, L3 to L13, L18 to L22 and L24 are microstriplines on a double copper-clad printed-circuit board, with fibre-glass reinforced PTFE dielectric (ε_r = 2.2), thickness $^1/_{16}$ inch; thickness of copper sheet 2 × 35 μm.
3. L2 and L23 are soldered on to striplines L1 and L24 respectively.



Dimensions in mm.

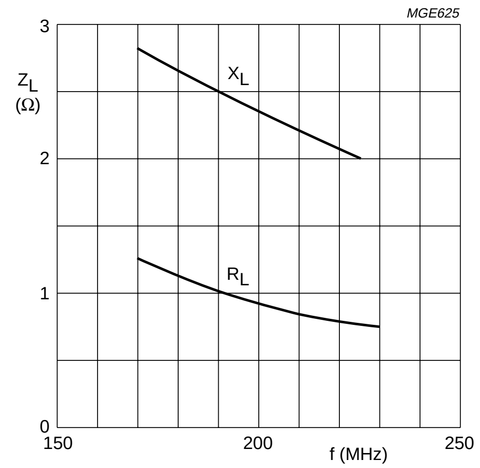
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by means of copper straps for a direct contact between upper and lower sheets.

Fig.22 Printed-circuit board and component layout for 225 MHz class-AB test circuit.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A;
R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.23 Input impedance as a function of frequency (series components); typical values per section.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A;
R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.24 Load impedance as a function of frequency (series components); typical values per section.

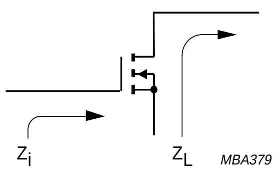
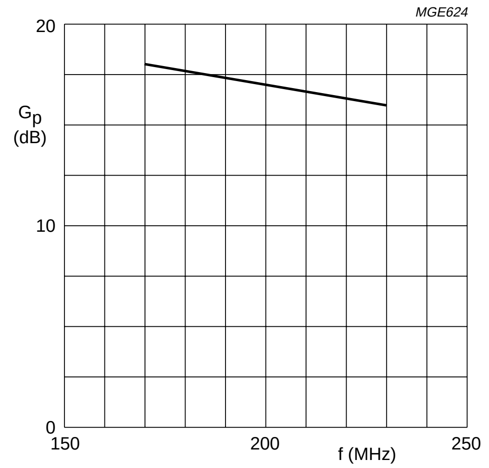


Fig.25 Definition of MOS impedance.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 × 0.5 A;
R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.26 Power gain as a function of frequency; typical values per section.

BLF278 scattering parameters

V_{DS} = 50 V; I_D = 500 mA; note 1

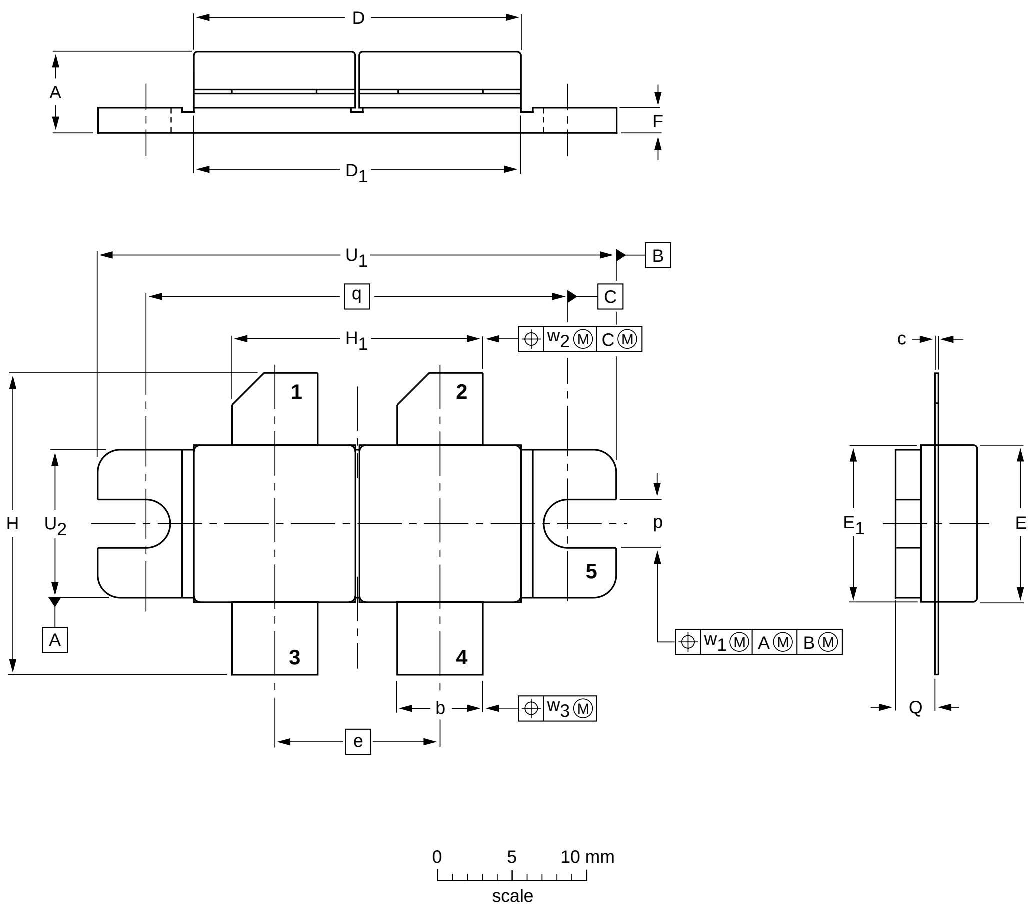
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	$\lvert s_{11}\rvert$	∠ Φ	$\lvert s_{21}\rvert$	∠ Φ	$\lvert s_{12}\rvert$	∠ Φ	$\lvert s_{22}\rvert$	∠ Φ
5	0.87	–142.1	60.05	104.3	0.00	–19.4	0.83	160.9
10	0.88	–159.8	32.09	91.4	0.00	0.68	167.5	165.8
20	0.88	–169.0	15.70	77.3	0.01	13.4	0.62	177.6
30	0.88	–171.2	9.98	68.4	0.01	3.4	0.64	–175.8
40	0.89	–172.2	6.99	61.0	0.01	–4.4	0.66	–171.2
50	0.91	–172.9	5.24	55.0	0.01	–10.3	0.70	–168.1
60	0.92	–173.5	4.08	49.6	0.01	–15.0	0.74	–166.8
70	0.93	–174.1	3.26	44.9	0.01	–18.3	0.78	–166.5
80	0.94	–174.7	2.66	41.0	0.01	–19.8	0.80	–166.5
90	0.95	–175.2	2.22	37.5	0.00	–19.7	0.83	–166.7
100	0.95	–175.7	1.88	34.0	0.00	–18.0	0.85	–167.4
125	0.97	–176.9	1.27	26.8	0.00	–1.9	0.88	–169.4
150	0.97	–177.9	0.91	22.7	0.00	35.3	0.91	–170.0
175	0.98	–178.7	0.69	19.5	0.00	65.3	0.94	–170.8
200	0.98	–179.5	0.54	16.0	0.00	78.0	0.95	–172.4
250	0.99	179.2	0.35	12.1	0.01	86.7	0.96	–174.0
300	0.99	178.1	0.25	9.1	0.01	87.8	0.98	–175.5
350	0.99	177.1	0.19	8.2	0.01	90.3	0.98	–176.5
400	0.99	176.1	0.14	7.2	0.01	91.4	0.99	–177.6
450	0.99	175.1	0.11	8.1	0.02	92.2	0.99	–178.3
500	0.99	174.2	0.09	9.7	0.02	91.5	0.99	–179.2
600	0.99	172.4	0.07	14.8	0.02	91.4	0.99	179.5
700	0.99	170.7	0.05	24.0	0.03	91.6	0.99	178.3
800	0.99	168.9	0.04	35.6	0.03	92.5	1.00	177.1
900	0.99	167.1	0.04	46.0	0.04	93.1	1.00	176.0
1000	0.99	165.2	0.04	60.3	0.04	94.1	1.00	175.0

Note

1. For more extensive s-parameters see internet:
http://www.semiconductors.philips.com/markets/communications/wirelesscommunications/broadcast.

PACKAGE OUTLINE

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT262A1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.77 5.00	5.85 5.58	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	21.08 19.56	17.02 16.51	3.28 3.02	2.85 2.59	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.230 0.220	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.830 0.770	0.670 0.650	0.129 0.119	0.112 0.102	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A1						99-03-29

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