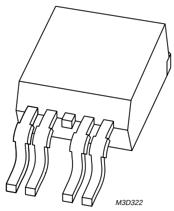


BUK9107-40ATC

TrenchPLUS logic level FET

Rev. 03 — 22 January 2002 **Product data**

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance and TrenchPLUS diodes for clamping, ElectroStatic Discharge (ESD) protection and temperature sensing.

Product availability:

BUK9107-40ATC in SOT426 (D^2-PAK).

2. Features

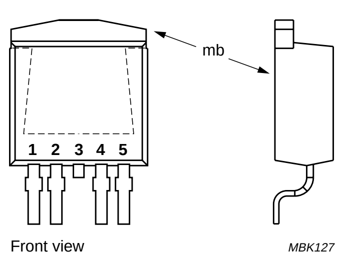
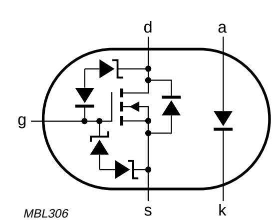
- Typical on-state resistance 5.8 mΩ
- Q101 compliant
- ESD and overvoltage protection
- Monolithically integrated temperature sensor for overload protection.

3. Applications

- Automotive and power switching:
  - 12 V and 24 V high power motor drives (e.g. Electrical Power Assisted Steering (EPAS))
  - Protected drive for lamps.

4. Pinning information

Table 1: Pinning - SOT426, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	anode (a)		
3	drain (d)		
4	cathode (k)		
5	source (s)		
mb	mounting base; connected to drain (d)		

SOT426 (D^2-PAK)

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DSR(CL)}$	drain-source clamping voltage	T_j = 25 °C; $I_{GS(CL)}$ = –2 mA; I_D = 1 A	50	-	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V	-	140	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	-	272	W
T_j	junction temperature		-	175	°C
R_{DSon}	drain-source on-state resistance	T_j = 25 °C; V_{GS} = 5 V; I_D = 50 A	5.8	7	mΩ
		T_j = 25 °C; V_{GS} = 4.5 V; I_D = 50 A	6	7.7	mΩ
		T_j = 25 °C; V_{GS} = 10 V; I_D = 50 A	5.2	6.2	mΩ
V_F	temperature sense diode forward voltage	T_j = 25 °C; I_F = 250 µA	658	668	mV
S_F	temperature sense diode temperature coefficient	–55 °C < T_j < +175 °C; I_F = 250 µA	–1.54	–1.68	mV/K

6. Limiting values

Table 3: Limiting values

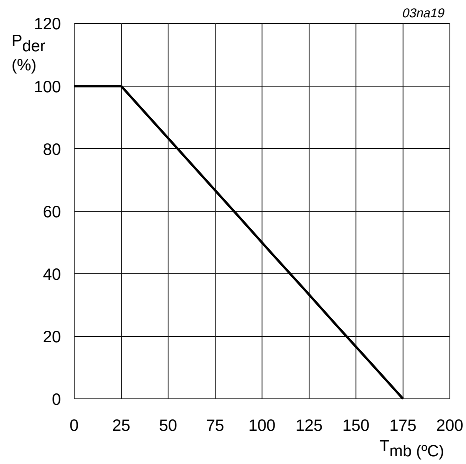
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)		[1]	-	40	V
V_{DGS}	drain-gate voltage (DC)	I_{DG} = 250 µA	[1]	-	40	V
V_{GS}	gate-source voltage (DC)		[1]	-	±15	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V; Figure 2 and 3	[2]	-	140	A
			[3]	-	75	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Figure 2	[3]	-	75	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; Figure 3		-	560	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1		-	272	W
$I_{DG(CL)}$	drain-gate clamping current	t_p = 5 ms; δ = 0.01		-	50	mA
$I_{GS(CL)}$	gate-source clamping current	continuous		-	10	mA
		t_p = 5 ms; δ = 0.01		-	50	mA
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage			-	±100	V
T_{stg}	storage temperature			–55	+175	°C
T_j	junction temperature			–55	+175	°C
Source-drain diode						
I_{DR}	reverse drain current (DC)	T_{mb} = 25 °C	[2]	-	140	A
			[3]	-	75	A
I_{DRM}	pulsed reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs		-	560	A
Clamping						
$E_{DS(CL)S}$	non-repetitive drain-source clamping energy	unclamped inductive load; I_D = 75 A; $V_{DS} \leq 40$ V; V_{GS} = 5 V; R_{GS} = 10 kΩ; starting T_j = 25 °C		-	1.4	J
Electrostatic discharge						
V_{esd}	electrostatic discharge voltage; pins 1, 3, 5	Human Body Model; C = 100 pF; R = 1.5 kΩ		-	6	kV

[1] Voltage is limited by clamping

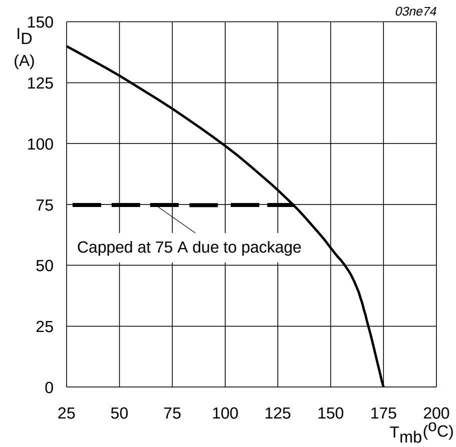
[2] Current is limited by power dissipation chip rating

[3] Continuous current is limited by package.



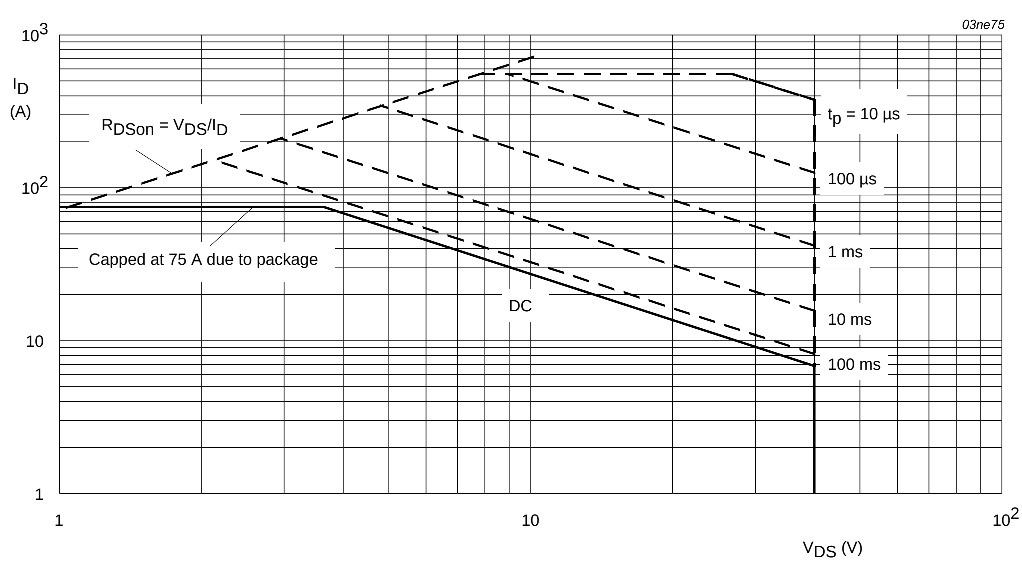
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 5$ V

Fig 2. Continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed circuit board; minimum footprint; SOT426 package	-	-	50	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.55	K/W

7.1 Transient thermal impedance

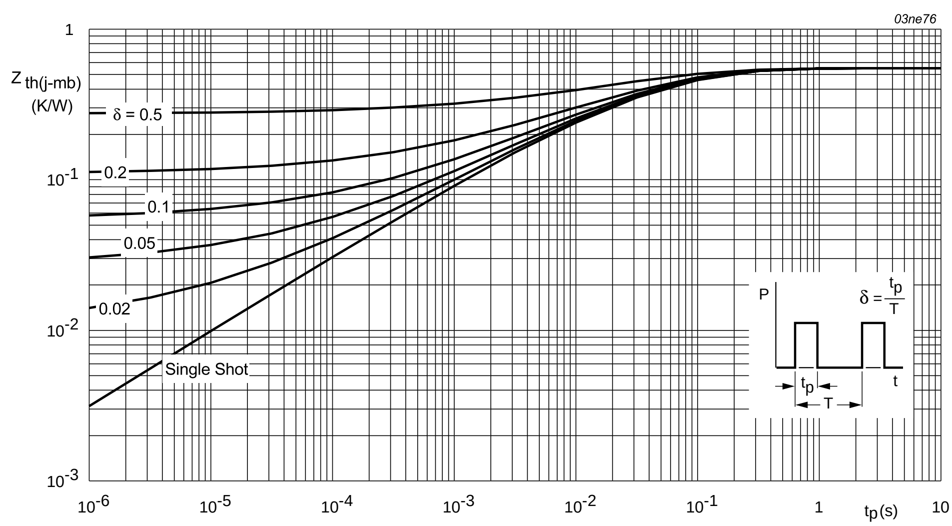


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

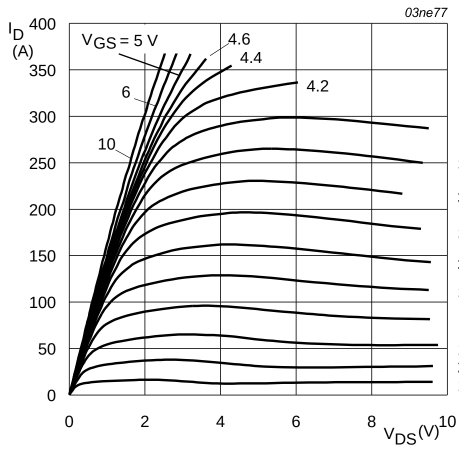
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DG}$	drain-gate zener breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	40	-	-	V
		T_j = –55 °C	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	1	1.5	2	V
		T_j = 175 °C	0.5	-	-	V
		T_j = –55 °C	-	-	2.3	V
I_{DSS}	drain-source leakage current	V_{DS} = 40 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.1	100	µA
		T_j = 175 °C	-	-	250	µA
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = ±1 mA; –55 °C < T_j < 175 °C	12	15	-	V
I_{GSS}	gate-source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	5	1000	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 50 A; Figure 7 and 8				
		T_j = 25 °C	-	5.8	7	mΩ
		T_j = 175 °C	-	-	14	mΩ
		V_{GS} = 4.5 V; I_D = 50 A	-	6	7.7	mΩ
		V_{GS} = 10 V; I_D = 50 A	-	5.2	6.2	mΩ
V_F	temperature sense diode forward voltage	I_F = 250 µA	648	658	668	mV
S_F	temperature sense diode temperature coefficient	I_F = 250 µA; –55 °C < T_j < 175 °C	–1.4	–1.54	–1.68	mV/K
V_{hys}	temperature sense diode forward voltage hysteresis	125 µA < I_F < 250 µA	25	32	50	mV
Dynamic characteristics						
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12	-	5836	-	pF
C_{oss}	output capacitance		-	958	-	pF
C_{rss}	reverse transfer capacitance		-	595	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; R_G = 1 kΩ	-	3	-	µs
t_r	rise time		-	10	-	µs
$t_{d(off)}$	turn-off delay time		-	17	-	µs
t_f	fall time		-	11	-	µs
L_d	internal drain inductance	measured from upper edge of drain mounting base to centre of die	-	2.5	-	nH

Table 5: Characteristics...*continued*

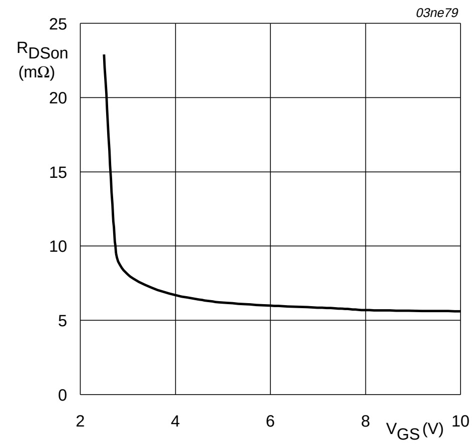
$T_j = 25\,°C$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L_s	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25$ A; $V_{GS} = 0$ V; Figure 19	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20$ A; $dI_S/dt = -100$ A/µs $V_{GS} = -10$ V; $V_{DS} = 30$ V	-	85	-	ns
Q_r	recovered charge		-	250	-	nC



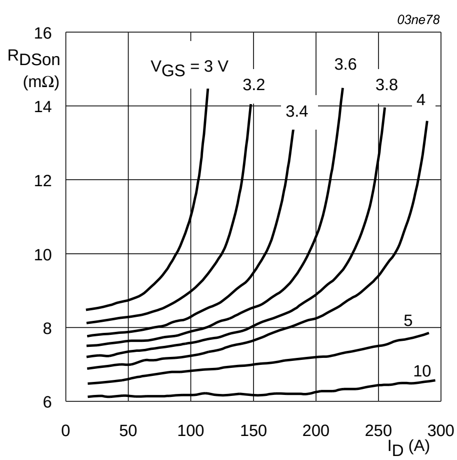
T_j = 25 °C; t_p = 300 µs

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



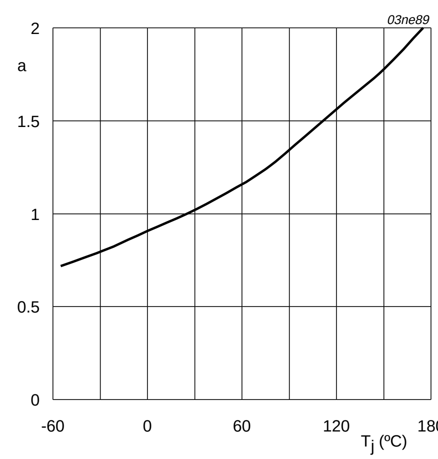
T_j = 25 °C; I_D = 50 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



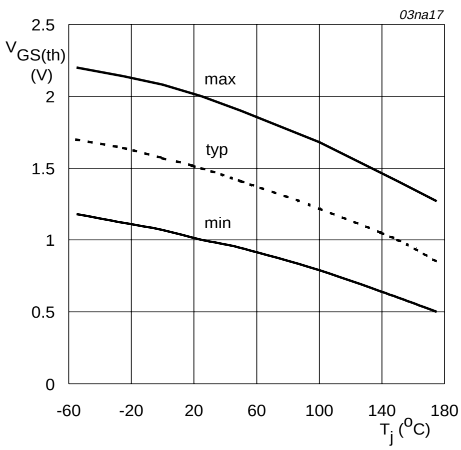
T_j = 25 °C; t_p = 300µs

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



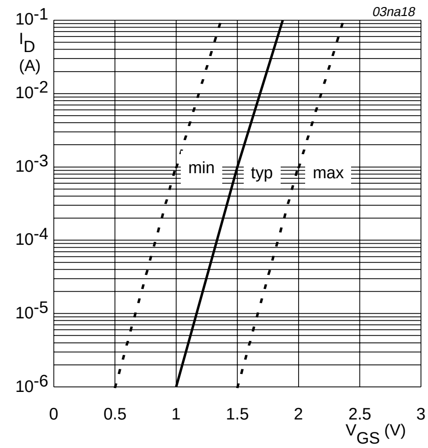
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



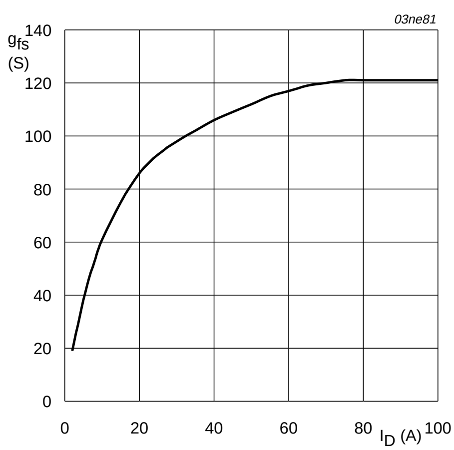
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



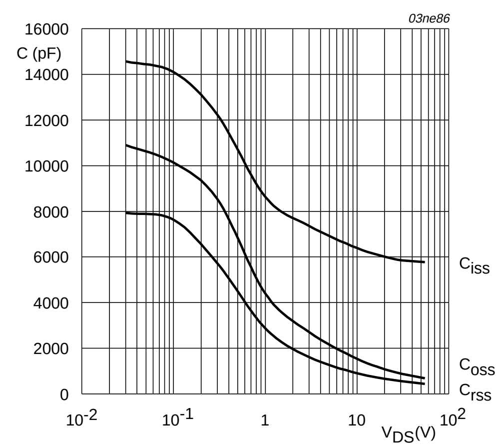
T_j = 25 °C; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



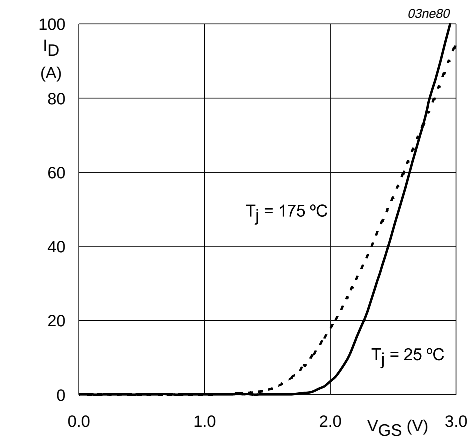
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values.



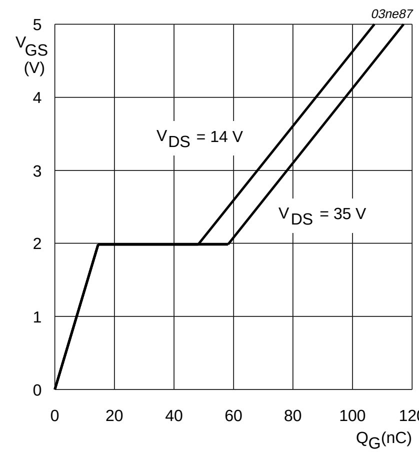
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



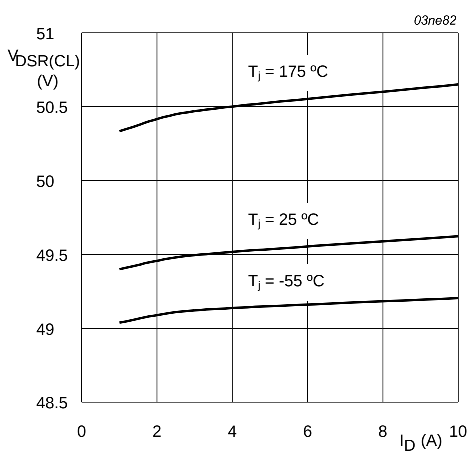
V_{DS} = 25 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



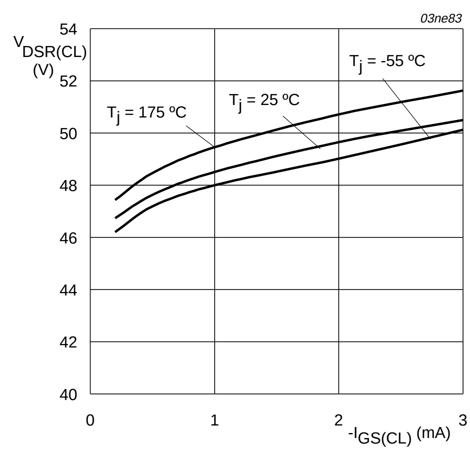
T_j = 25 °C; I_D = 50 A

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



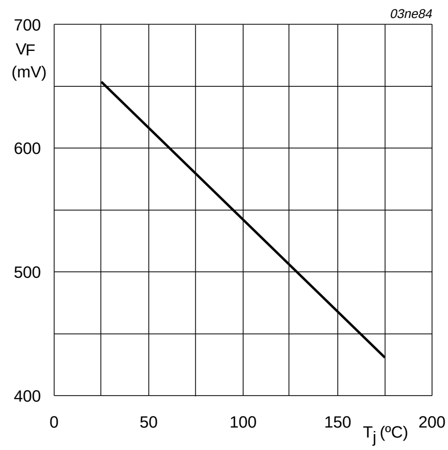
$I_{GS(CL)}$ = –2 mA

Fig 15. Drain-source clamping voltage as a function of drain current; typical values.



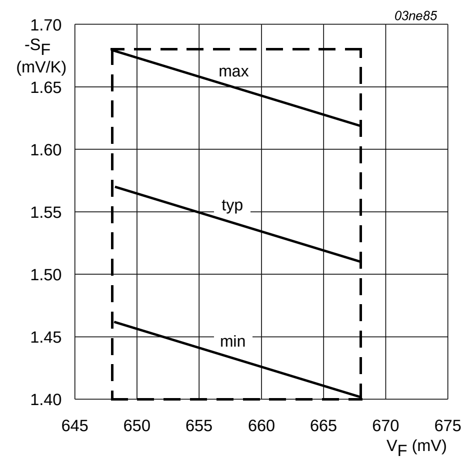
I_D = 10 A

Fig 16. Drain-source clamping voltage as a function of gate current; typical values.



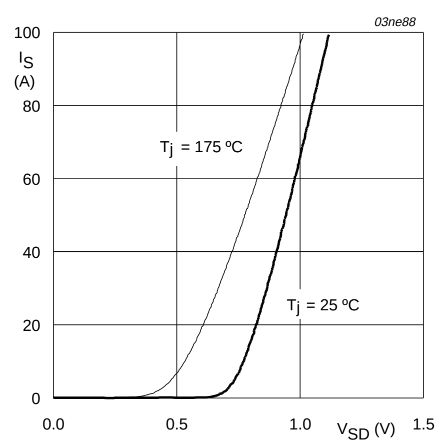
I_F = 250 µA

Fig 17. Forward voltage of temperature sense diode as a function of junction temperature; typical values.



V_F at T_j = 25 °C; I_F = 250 µA

Fig 18. Temperature coefficient of temperature sense diode as a function of forward voltage; typical values.

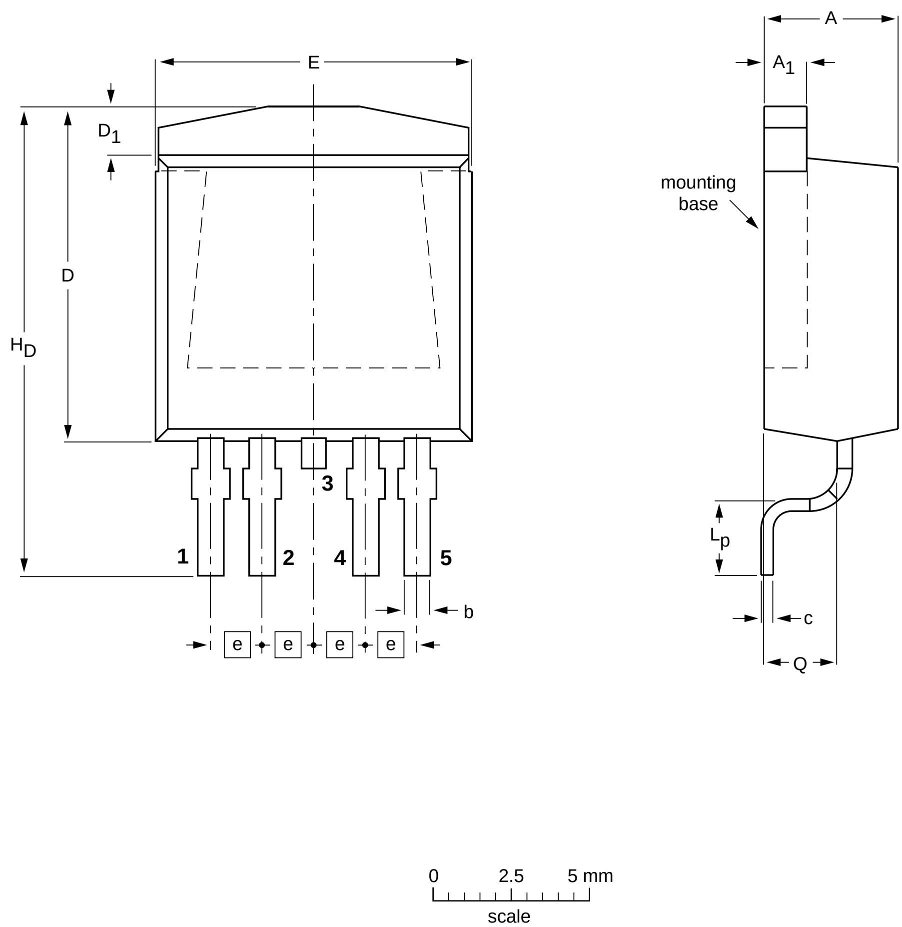


V_{GS} = 0 V

Fig 19. Reverse diode current as a function of reverse diode voltage; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version of D[2]-PAK); 5 leads (one lead cropped) **SOT426**



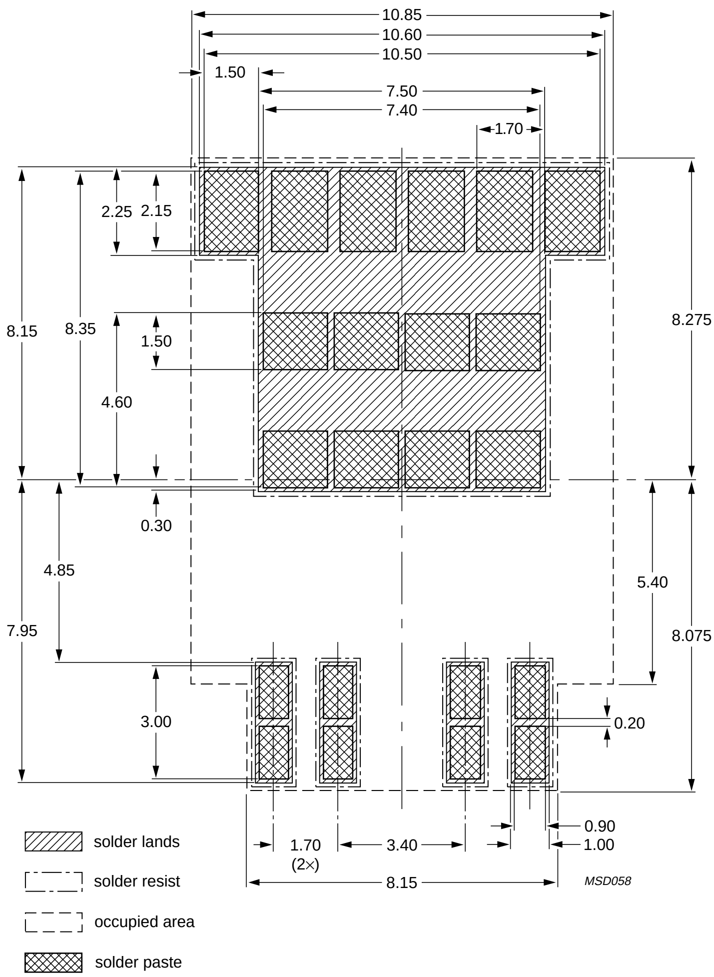
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	1.70	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT426						~~98-12-14~~ 99-06-25

Fig 20. SOT426.

10. Soldering



Dimensions in mm.

Fig 21. Reflow soldering footprint for SOT426.

11. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	20020122	-	**Product data; third version (9397 750 08724); supersedes second version of 20010829**
02	20010829	-	**Product data; second version (9397 750 08709); supersedes initial version of 20010814** • Units of symbol 'R_{DSon}' changed from 'μΩ' to 'mΩ' in Table 2 • Units of timing parameters changed from 'ns' to 'μs' in Table 5 • Values of timing parameters changed in Table 5
01	20010814	-	**Product data; initial version (9397 750 08319)**

12. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

13. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

14. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

15. Trademarks

TrenchMOS — is a registered trademark of Koninklijke Philips Electronics N.V.

Contact information

For additional information, please visit **http://www.semiconductors.philips.com**.
For sales office addresses, send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Fax: +31 40 27 24825

Contents

Date of release: 22 January 2002 **Document order number: 9397 750 08724**