OptiMOS™2 Power-Transistor

Product Summary

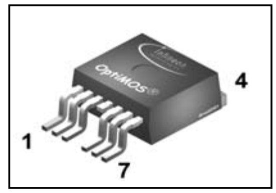
V_{DS}	40	V
$R_{DS(on),max}$	2.1	mΩ
I_D	160	A

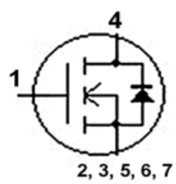
Features

- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1)] for target application
- For sync. rectification, or-ing and motor control
- Halogen-free accordig to IEC61249-2-21

RoHS Halogen-Free

PG-TO263-7





Type	Package	Marking
IPB021N04N	PG-TO263-7	21N04N

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[2)]	160	A
		T_C=100 °C	157	
Pulsed drain current[3)]	$I_{D,pulse}$	T_C=25 °C	640	
Avalanche energy, single pulse	E_{AS}	I_D=80 A, R_{GS}=25 Ω	898	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	214	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.7	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[4)]	-	-	40	

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=150 µA	2.1	3.0	4	
Zero gate voltage drain current	I_{DSS}	V_{DS}=32 V, V_{GS}=0 V, T_j=25 °C	-	-	1	µA
		V_{DS}=32 V, V_{GS}=0 V, T_j=125 °C	-	-	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=80 A	-	1.6	2.1	mΩ
Gate resistance	R_G		-	1.7	-	Ω

1) J-STD20 and JESD22

2) Current is limited by bondwire; with an R_{thJC}=0.7 K/W the chip is able to carry 221 A.

3) See figure 3

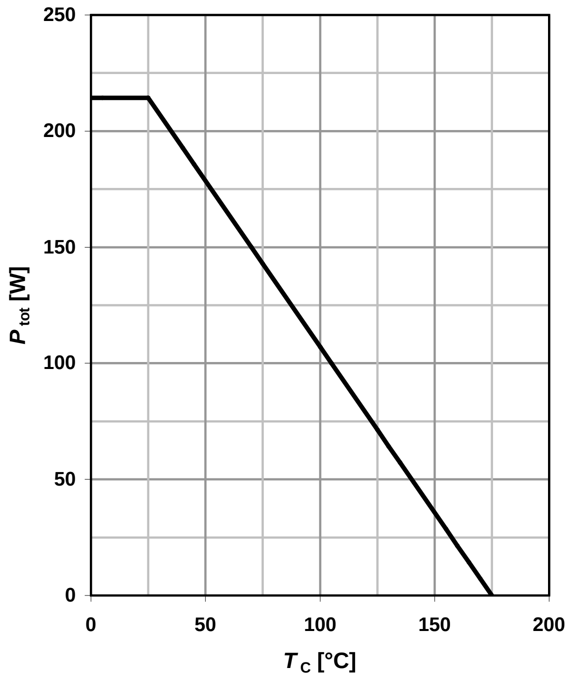
4) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	7400	9600	pF
Output capacitance	C_{oss}		-	2000	2660	
Reverse transfer capacitance	C_{rss}		-	310	465	
Turn-on delay time	$t_{d(on)}$	V_{DD}=20 V, V_{GS}=10 V, I_D=80 A, R_G=3.3 Ω	-	30	-	ns
Rise time	t_r		-	16	-	
Turn-off delay time	$t_{d(off)}$		-	46	-	
Fall time	t_f		-	17	-	
Gate Charge Characteristics[6)]						
Gate to source charge	Q_{gs}	V_{DD}=32 V, I_D=80 A, V_{GS}=0 to 10 V	-	38	50	nC
Gate to drain charge	Q_{gd}		-	25	45	
Switching charge	Q_{sw}		-	40	58	
Gate charge total	Q_g		-	110	145	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V
Output charge	Q_{oss}	V_{DD}=20 V, V_{GS}=0 V	-	66	88	nC
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	160	A
Diode pulse current	$I_{S,pulse}$		-	-	640	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=80 A, T_j=25 °C	-	0.85	1.3	V
Reverse recovery time	t_{rr}	V_R=20 V, I_F=50A, di_F/dt=100 A/µs	-	60		ns
Reverse recovery charge	Q_{rr}		-	95	-	nC

[6)] See figure 16 for gate charge parameter definition

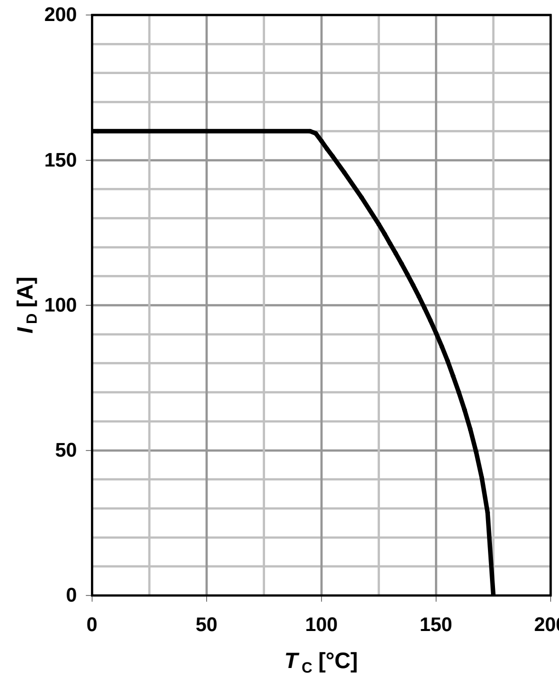
1 Power dissipation

P_{tot}=f(T_C)



2 Drain current

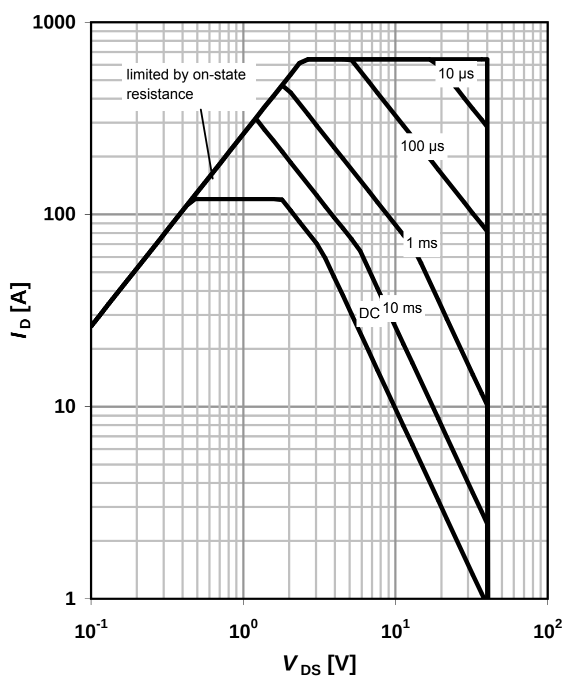
I_D=f(T_C); V_{GS}≥10 V



3 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

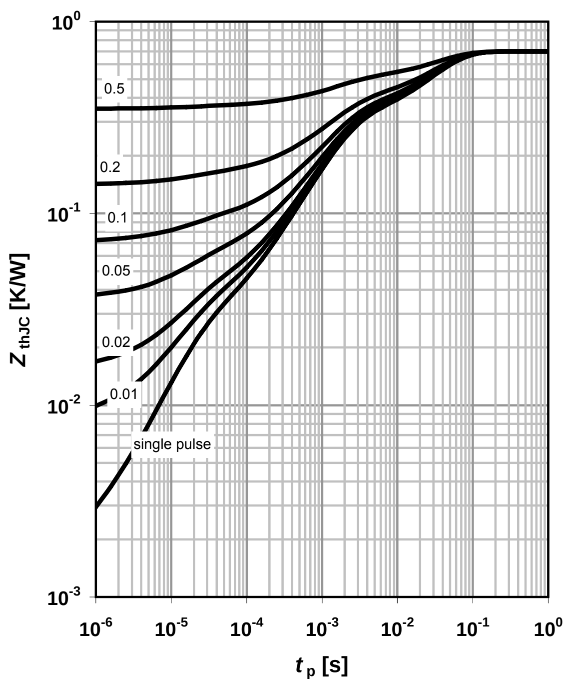
parameter: t_p



4 Max. transient thermal impedance

Z_{thJC}=f(t_p)

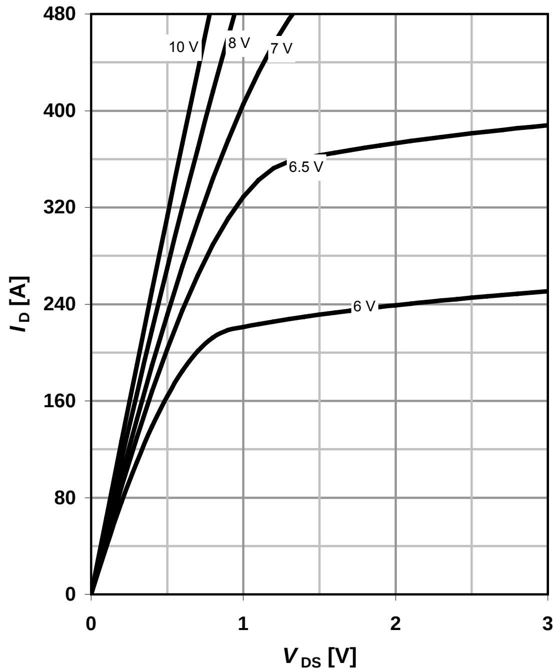
parameter: D=t_p/T



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

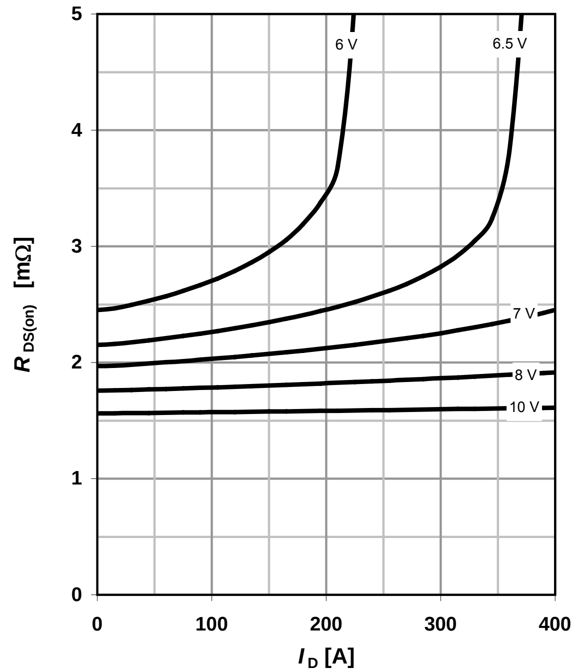
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

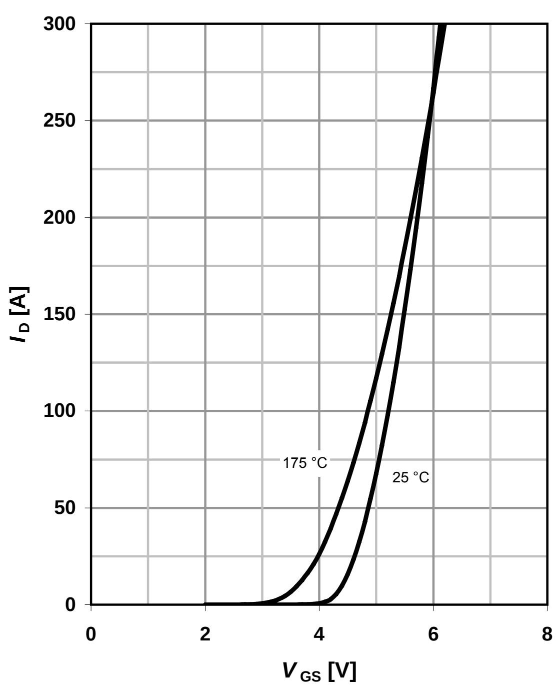
parameter: V_{GS}



7 Typ. transfer characteristics

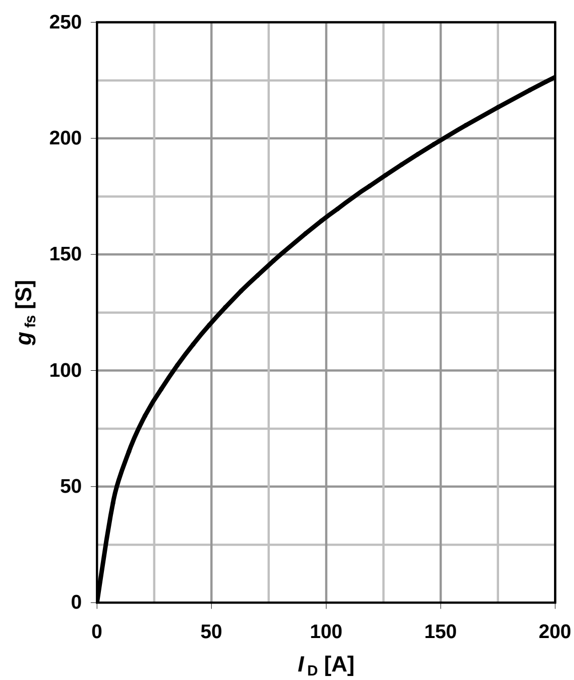
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$

parameter: T_j



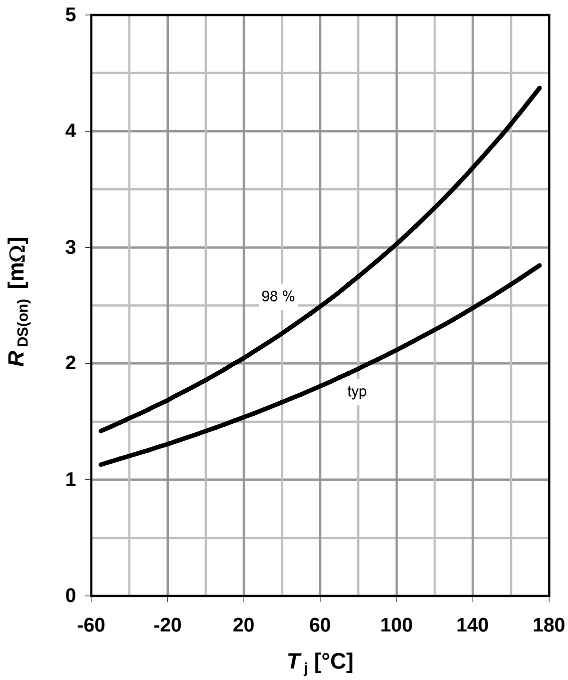
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

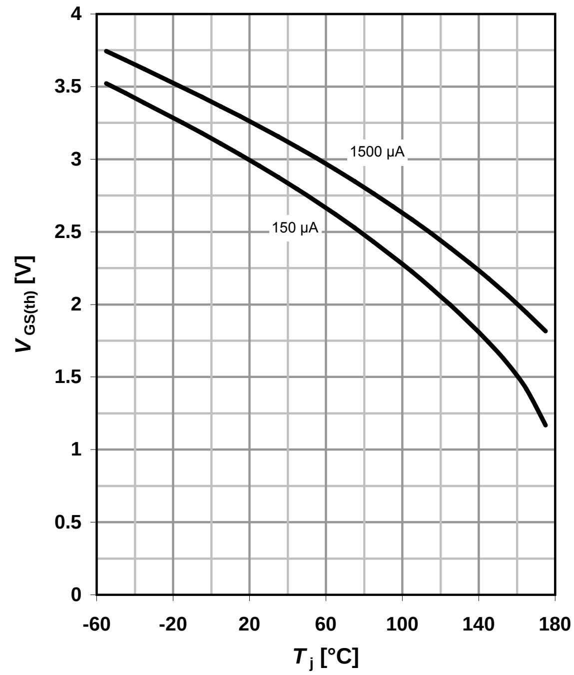
$R_{DS(on)}$=f(T_j); I_D=80 A; V_{GS}=10 V



10 Typ. gate threshold voltage

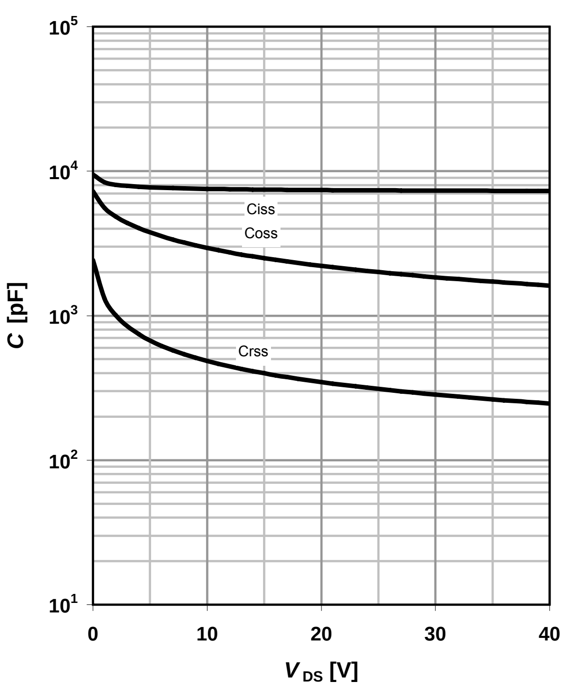
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

parameter: I_D



11 Typ. capacitances

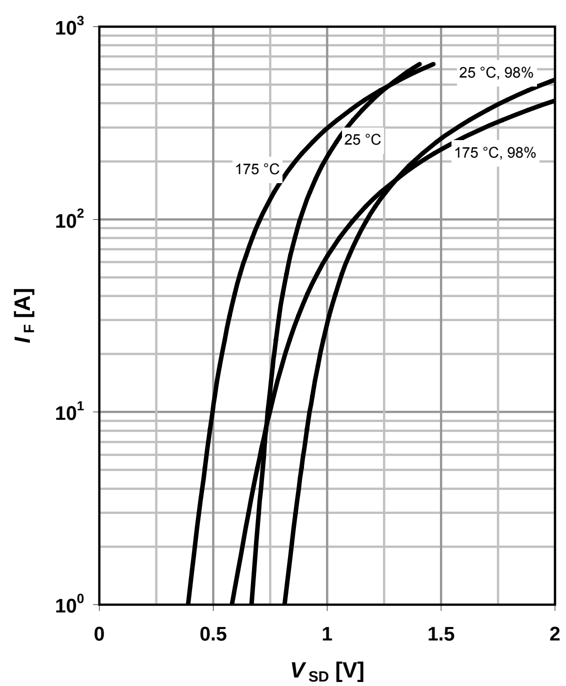
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

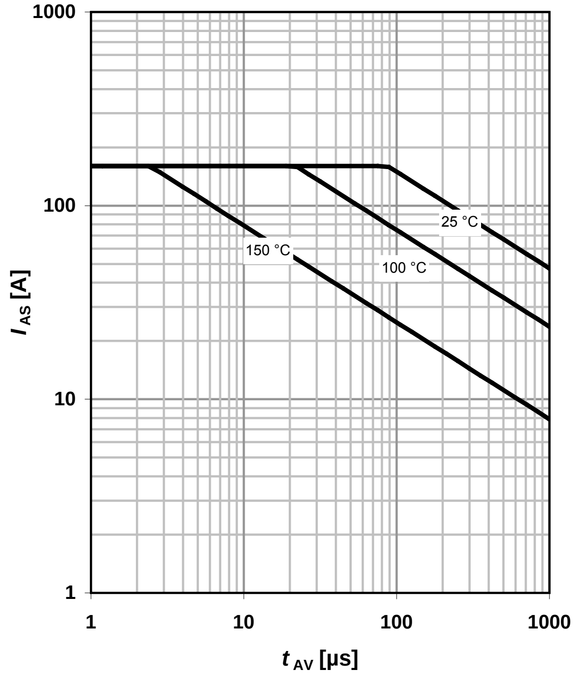
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

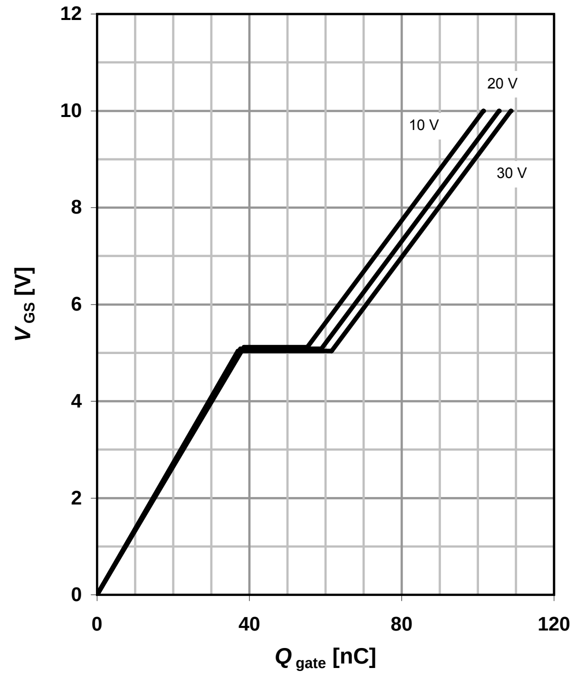
parameter: $T_{j(start)}$



14 Typ. gate charge

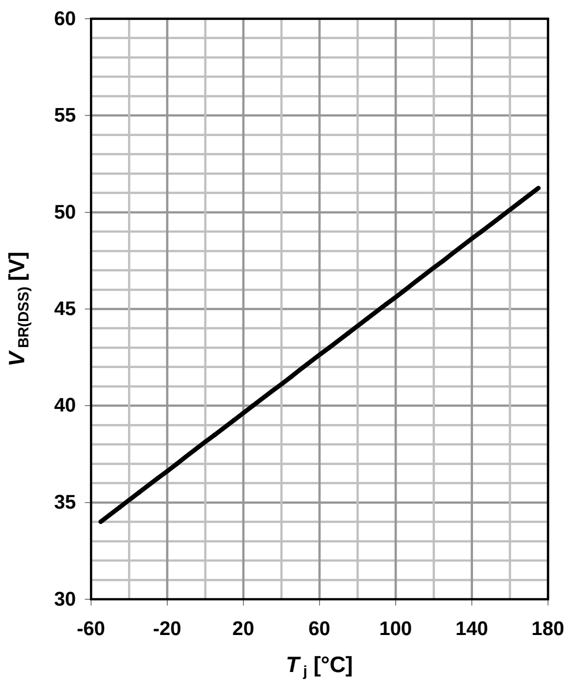
V_{GS}=f(Q_{gate}); I_D=80 A pulsed

parameter: V_{DD}

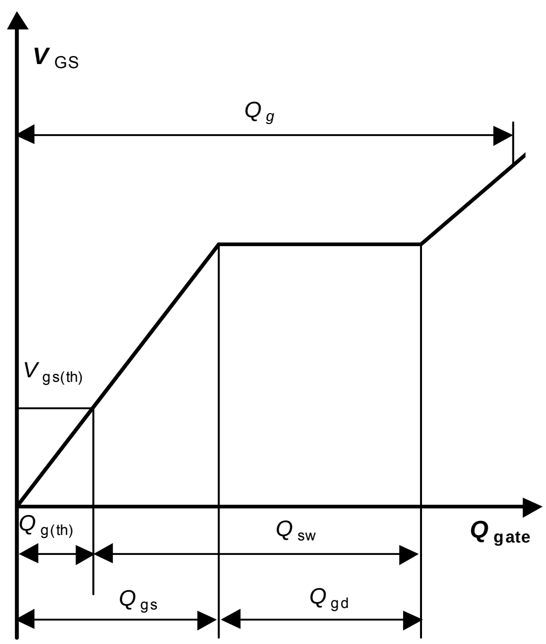


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



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