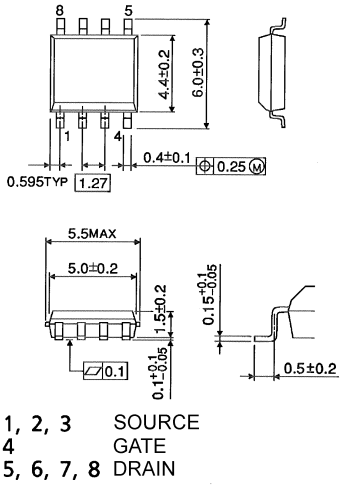
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOS IV)

TPC8030

Lithium Ion Battery Applications
Portable Equipment Applications
Notebook PC Applications

- Small footprint due to small and thin package
- Low drain-source ON-resistance: $R_{DS\ (ON)}$ = 7.5 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 26 S (typ.)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 30 V)
- Enhancement mode: V_{th} = 1.3 to 2.5 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



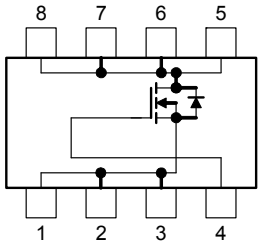
JEDEC	—
JEITA	—
TOSHIBA	2-6J1B

Weight: 0.08 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	30	V
Gate-source voltage		V_{GSS}	± 25	V
Drain current	DC (Note 1)	I_D	11	A
	Pulse (Note 1)	I_{DP}	44	
Drain power dissipation (t = 10 s) (Note 2a)		P_D	1.9	W
Drain power dissipation (t = 10 s) (Note 2b)		P_D	1.0	W
Single pulse avalanche energy (Note 3)		E_{AS}	31	mJ
Avalanche current		I_{AR}	11	A
Repetitive avalanche energy (Note 2a) (Note 4)		E_{AR}	0.053	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Circuit Configuration



Note 1, Note 2, Note 3 and Note 4: See the next page.

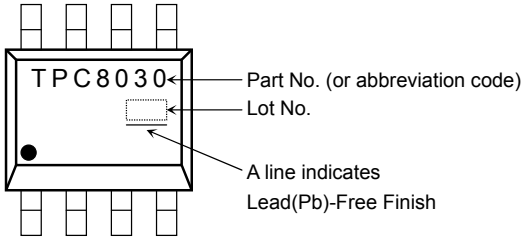
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/”Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

Thermal Characteristics

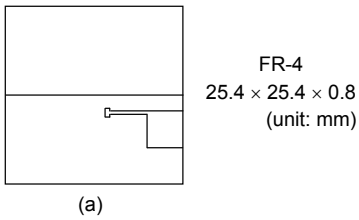
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	65.8	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	125	°C/W

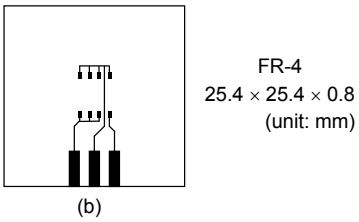
Marking (Note 5)



Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



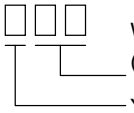


Note 3: V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 0.2 mH, I_{AR} = 11 A

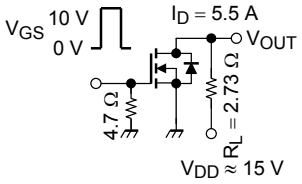
Note 4: Repetitive rating: pulse width limited by max channel temperature

Note 5: • on lower left of the marking indicates Pin 1.

※ Weekly code: (Three digits)



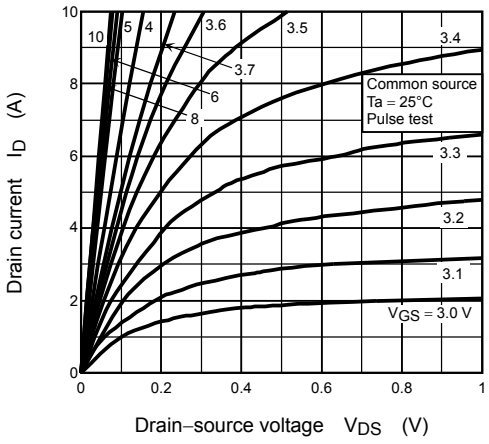
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	—	—	±100	nA
Drain cut-OFF current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −25 V	5	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.3	—	2.5	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 5.5 A	—	11.5	17	mΩ
			V_{GS} = 10 V, I_D = 5.5 A	—	7.5	9	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 5.5 A	13	26	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1140	—	pF
Reverse transfer capacitance		C_{rss}		—	255	—	
Output capacitance		C_{oss}		—	390	—	
Switching time	Rise time	t_r	 Duty ≤ 1%, t_w = 10 μs	—	14	—	ns
	Turn-ON time	t_{on}		—	25	—	
	Fall time	t_f		—	9	—	
	Turn-OFF time	t_{off}		—	33	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 11 A	—	24	—	nC
Gate-source charge 1		Q_{gs1}		—	4	—	
Gate-drain (“miller”) charge		Q_{gd}		—	8.4	—	

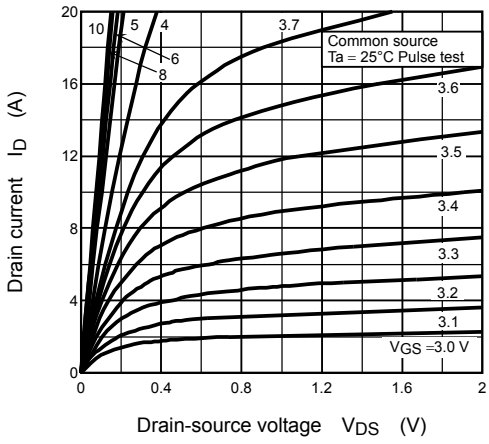
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	44	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 11 A, V_{GS} = 0 V	—	—	−1.2	V

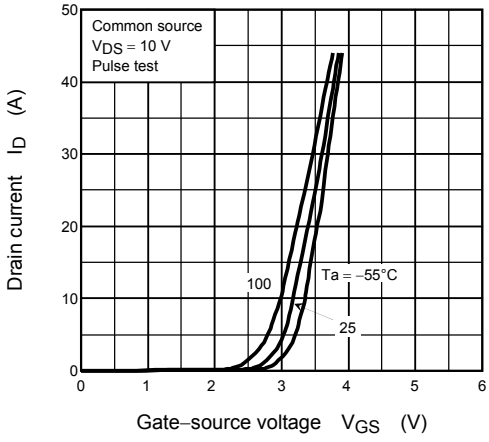
$I_D - V_{DS}$



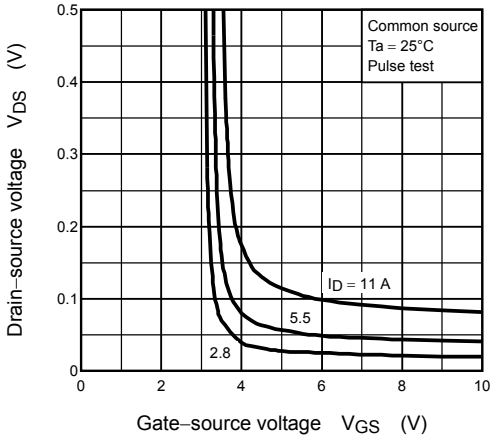
$I_D - V_{DS}$



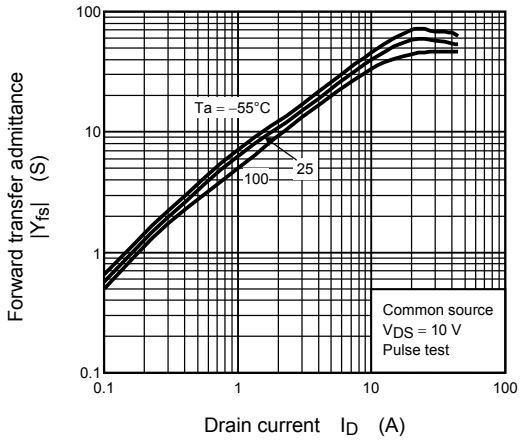
$I_D - V_{GS}$



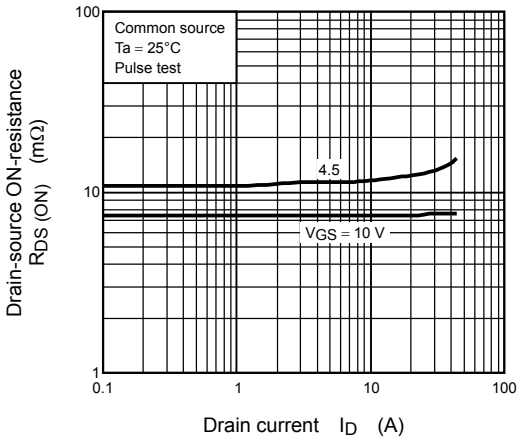
$V_{DS} - V_{GS}$



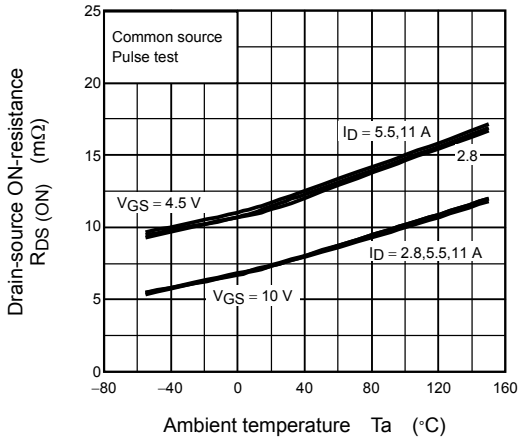
$|Y_{fs}| - I_D$



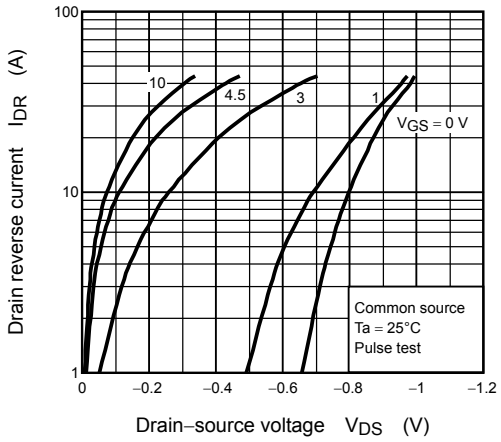
$R_{DS\ (ON)} - I_D$



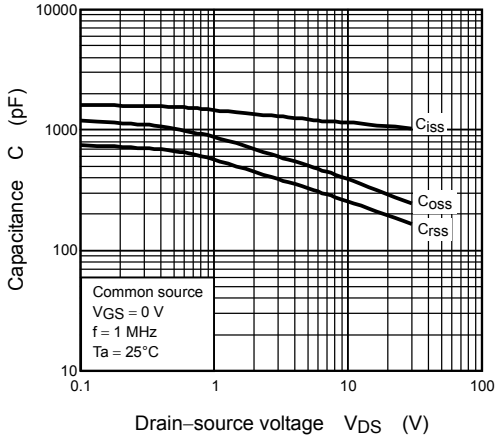
$R_{DS\ (ON)}$ – Ta



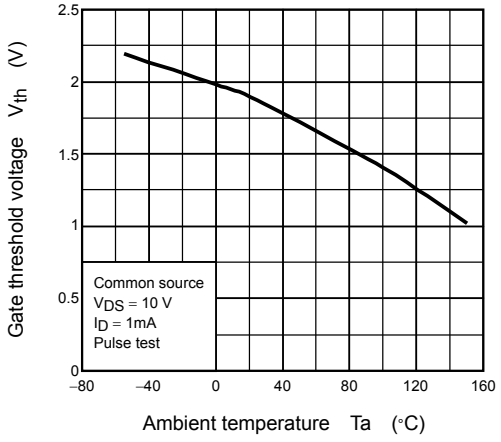
I_{DR} – V_{DS}



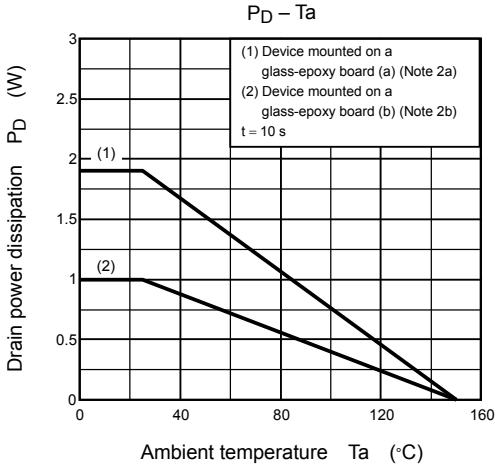
Capacitance – V_{DS}



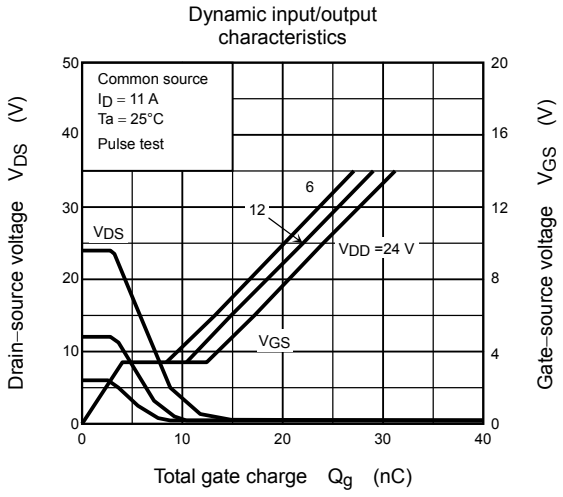
V_{th} – Ta

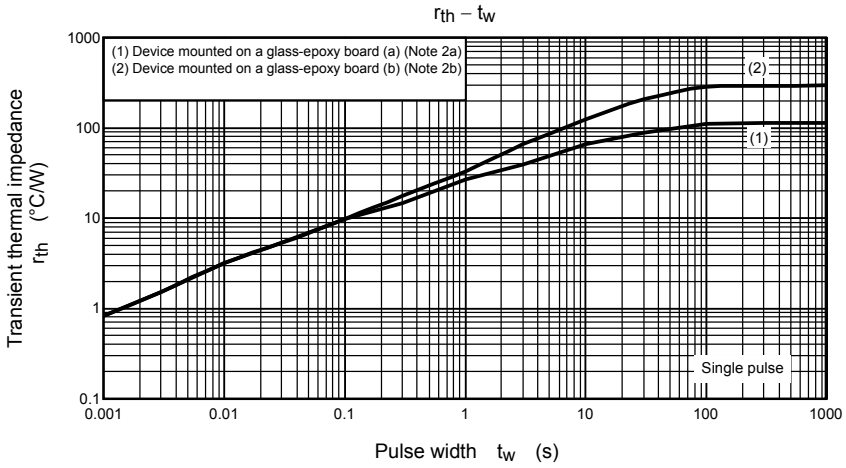


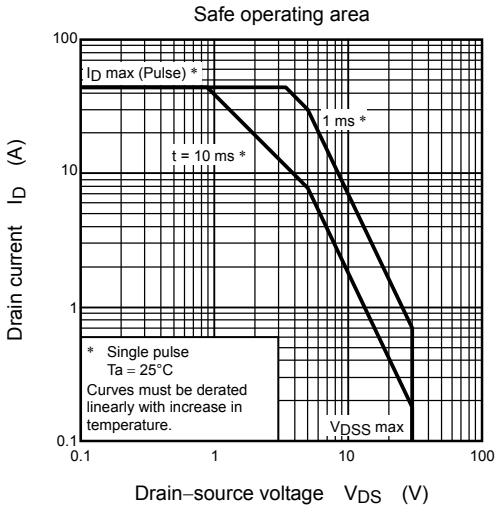
P_D – Ta



Dynamic input/output characteristics







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20070701-EN GENERAL

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