



P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
- 20	0.025 at V _{GS} = - 4.5 V	- 12 ^a	24 nC
	0.031 at V _{GS} = - 2.5 V	- 12 ^a	
	0.041 at V _{GS} = - 1.8 V	- 12 ^a	
	0.070 at V _{GS} = - 1.5 V	- 4	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

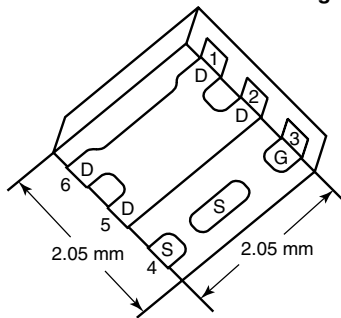


RoHS
COMPLIANT
HALOGEN
FREE

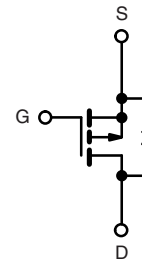
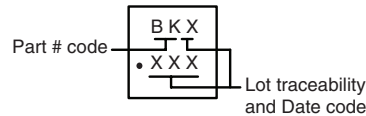
APPLICATIONS

- Load Switch, PA Switch and Battery Switch for Portable Devices

PowerPAK SC-70-6L-Single



Marking Code



Ordering Information: SiA431DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 20	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 12 ^a
		T _C = 70 °C	- 12 ^a
		T _A = 25 °C	- 9.6 ^{b, c}
		T _A = 70 °C	- 7.7 ^{b, c}
Pulsed Drain Current	I _{DM}	- 30	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	- 2.9 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	19
		T _C = 70 °C	12
		T _A = 25 °C	3.5 ^{b, c}
		T _A = 70 °C	2.2 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	28	36	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	5.3	6.5	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 80 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-14.5		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.7		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4		-0.85	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -6.5\text{ A}$		0.020	0.025	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -5.8\text{ A}$		0.025	0.031	
		$V_{GS} = -1.8\text{ V}, I_D = -2.5\text{ A}$		0.034	0.041	
		$V_{GS} = -1.5\text{ V}, I_D = -1.5\text{ A}$		0.045	0.070	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -6.5\text{ A}$		31		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1700		pF
Output Capacitance	C_{oss}			230		
Reverse Transfer Capacitance	C_{rss}			205		
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -8\text{ V}, I_D = -9.6\text{ A}$		40	60	nC
				24	36	
Gate-Source Charge	Q_{gs}	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -9.6\text{ A}$		2.4		
Gate-Drain Charge	Q_{gd}			6.5		
Gate Resistance	R_g	$f = 1\text{ MHz}$	1.3	6.3	13	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 1.3\text{ }\Omega$ $I_D \cong -7.7\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		22	35	ns
Rise Time	t_r			25	40	
Turn-Off Delay Time	$t_{d(off)}$			65	100	
Fall Time	t_f			25	40	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 1.3\text{ }\Omega$ $I_D \cong -7.7\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\text{ }\Omega$		10	15	
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			65	100	
Fall Time	t_f			20	30	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-12	A
Pulse Diode Forward Current	I_{SM}				-30	
Body Diode Voltage	V_{SD}	$I_S = -7.7\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -7.7\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		35	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			21	35	nC
Reverse Recovery Fall Time	t_a			20		ns
Reverse Recovery Rise Time	t_b			15		

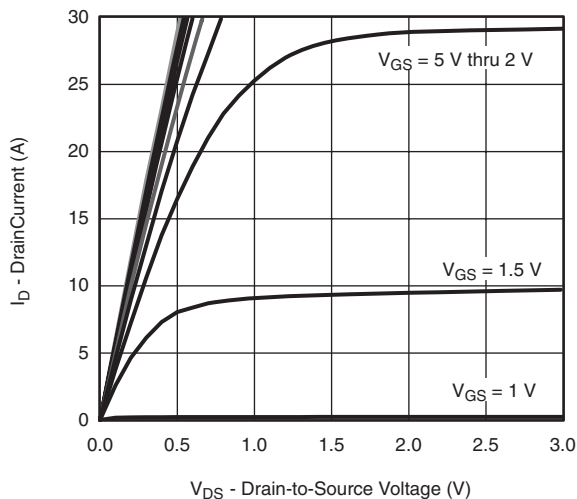
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

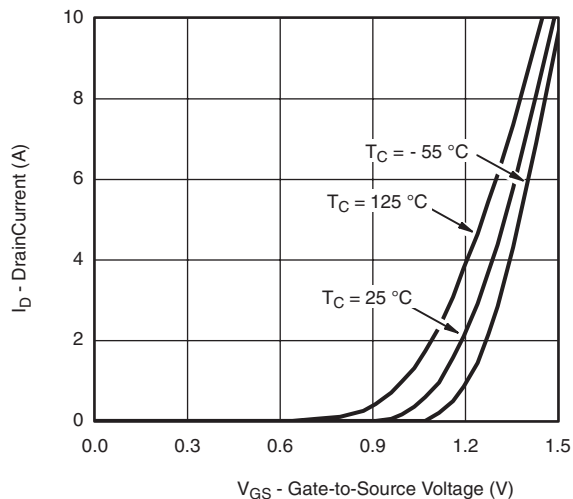
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



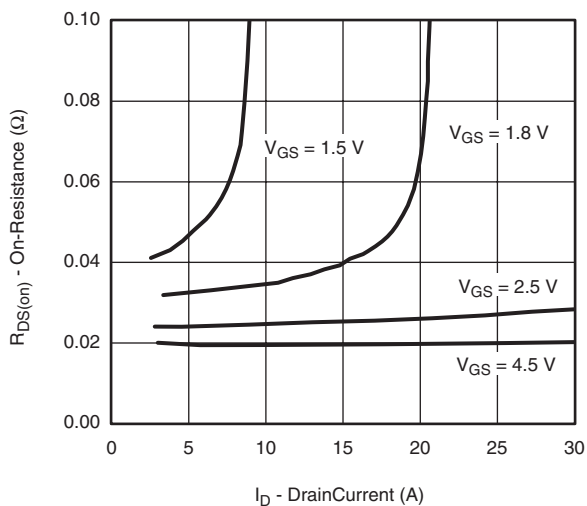
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



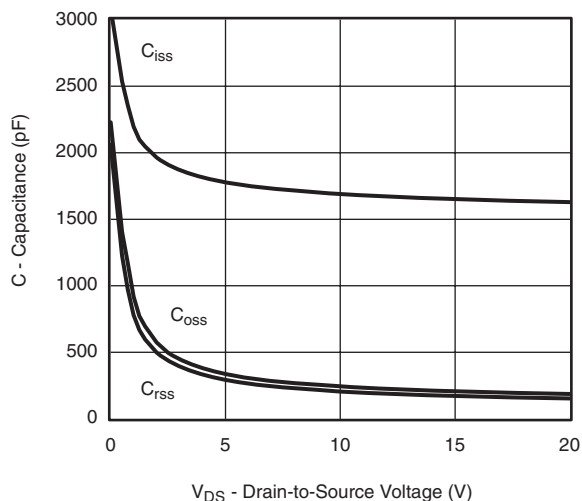
Output Characteristics



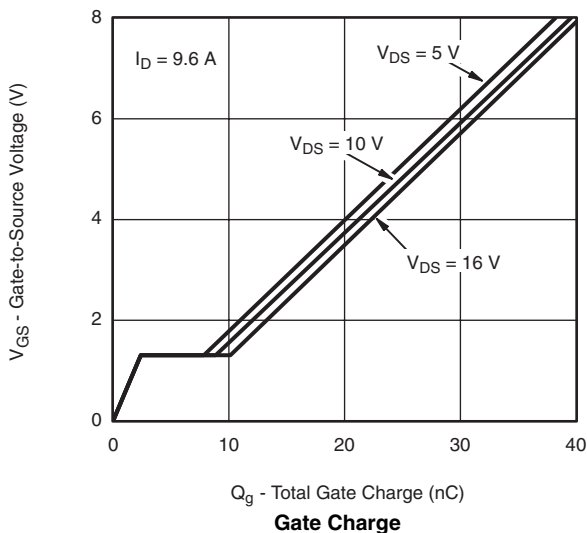
Transfer Characteristics



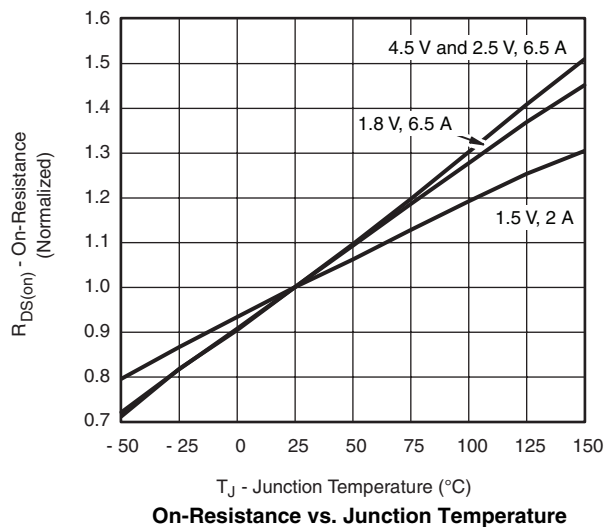
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



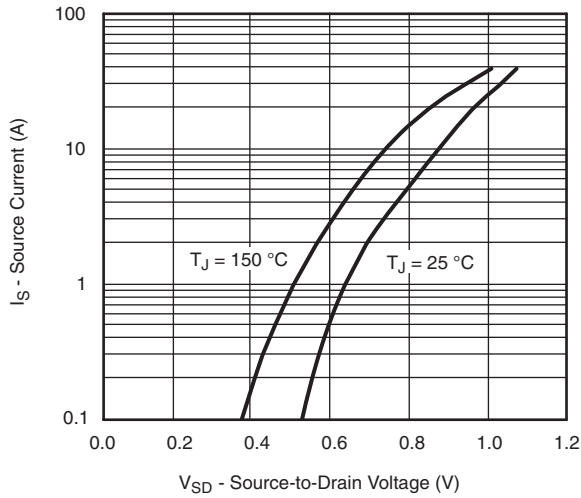
On-Resistance vs. Junction Temperature

SiA431DJ

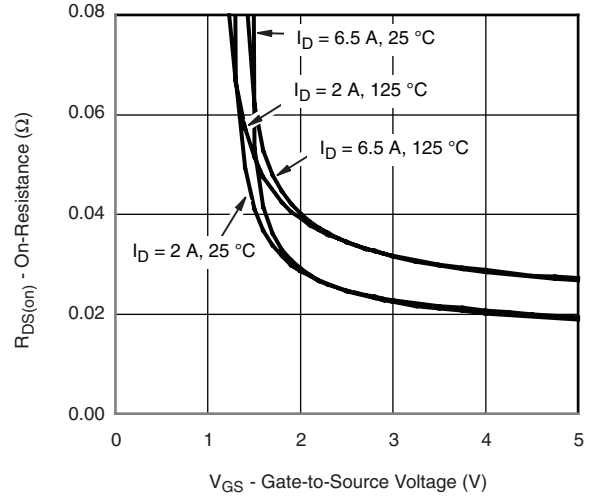
Vishay Siliconix



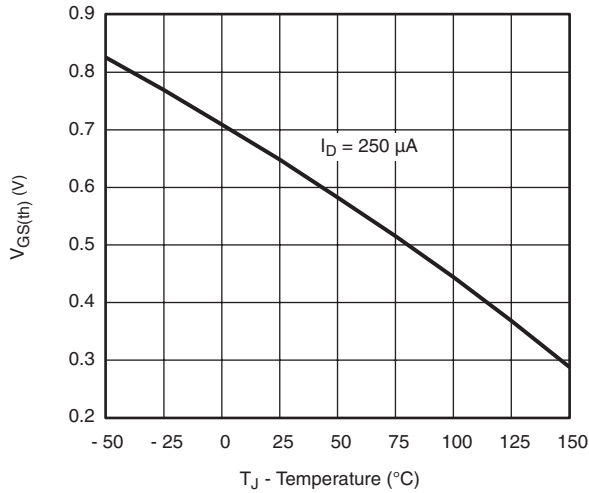
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



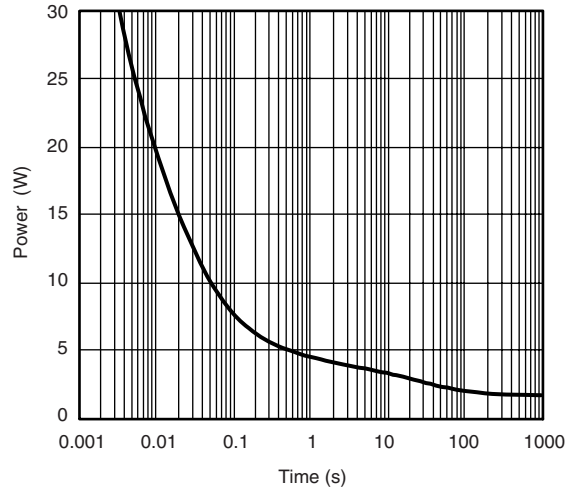
Source-Drain Diode Forward Voltage



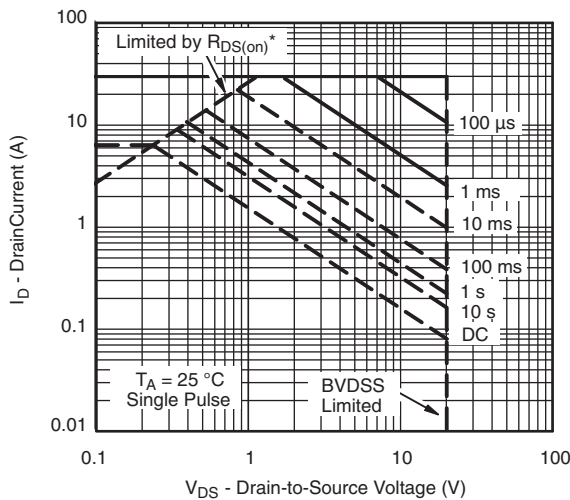
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



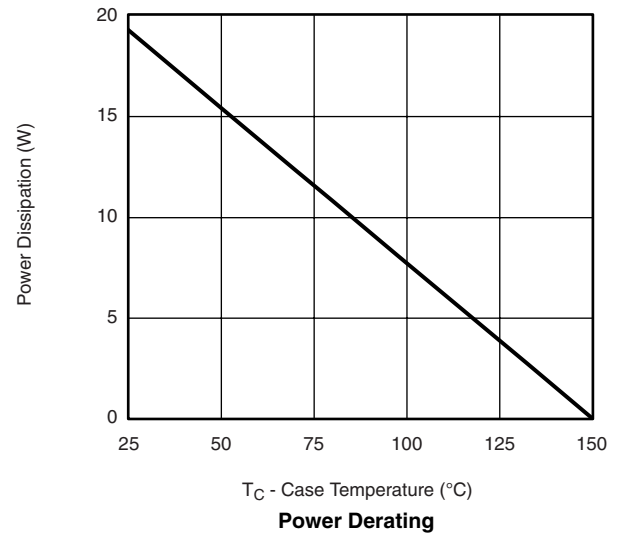
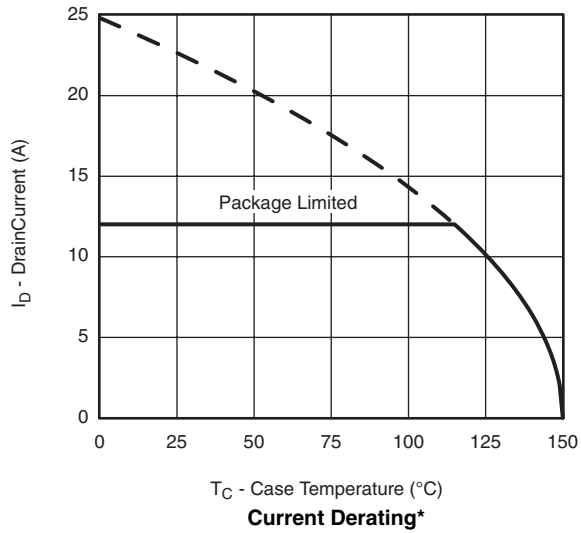
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



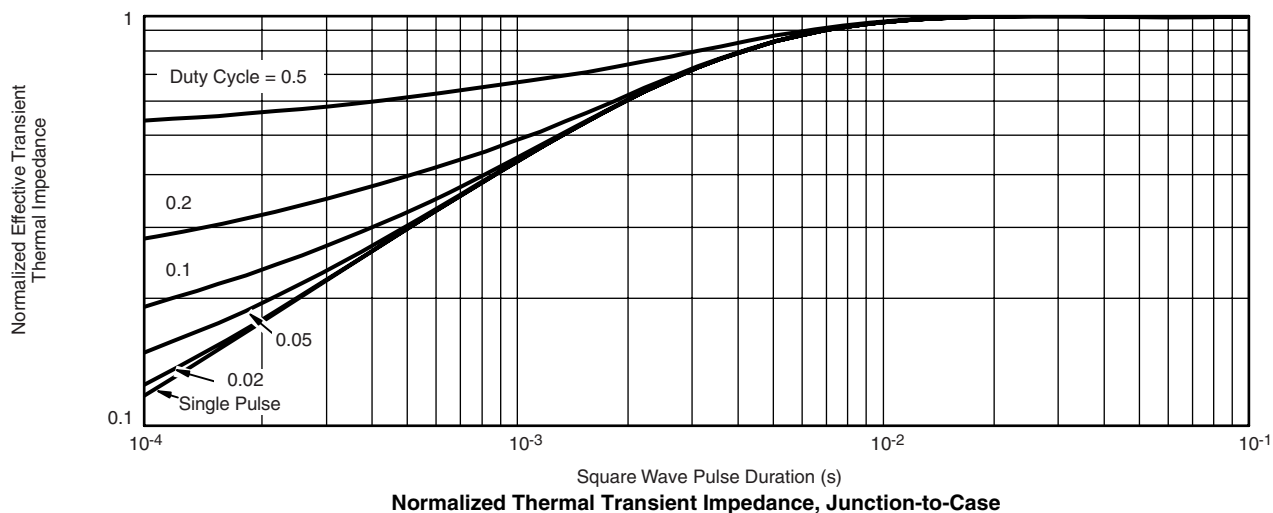
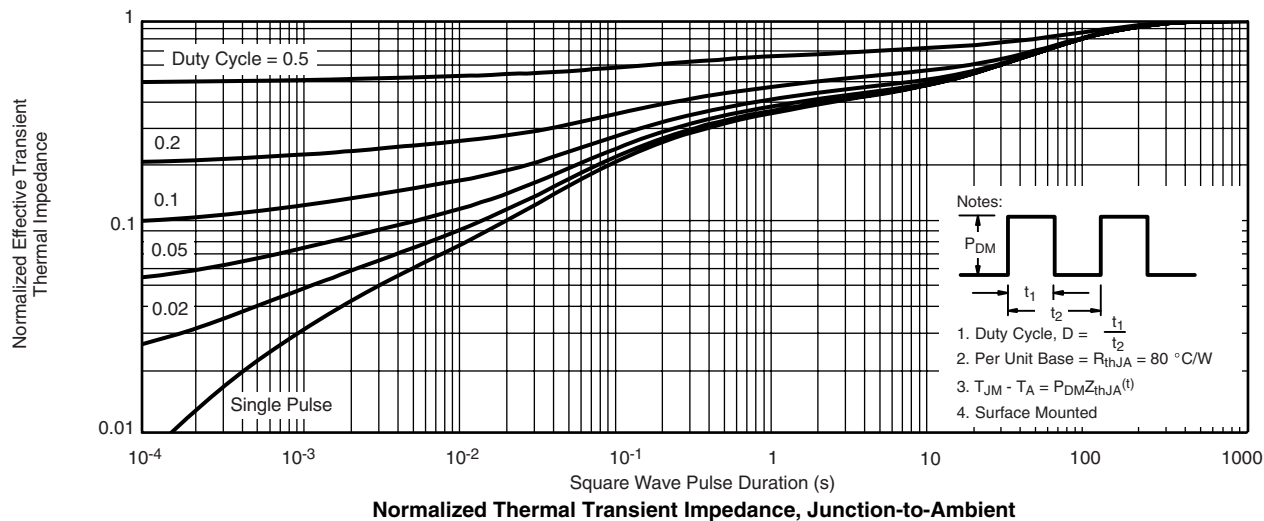
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SiA431DJ

Vishay Siliconix



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65267.



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