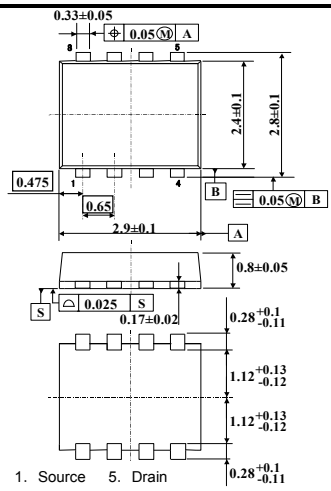
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (Ultra High speed U-MOSIII)

TPCP8001-H

High Efficiency DC／DC Converter Applications
Notebook PC Applications
Portable Equipment Applications

- Small footprint due to a small and thin package
- High speed switching
- Small gate charge: Q_{SW} = 3.6 nC (typ.)
- Low drain-source ON-resistance: $R_{DS\ (ON)}$ = 13 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 16 S (typ.)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 30V)
- Enhancement mode: V_{th} = 1.1 to 2.3 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-3V1K

Weight: 0.017 g (typ.)

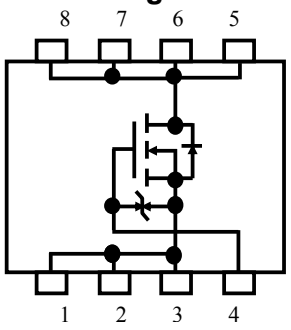
Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	7.2	A
	Pulsed (Note 1)	I_{DP}	28.8	
Drain power dissipation (t = 5 s) (Note 2a)		P_D	1.68	W
Drain power dissipation (t = 5 s) (Note 2b)		P_D	0.84	W
Single-pulse avalanche energy (Note 3)		E_{AS}	33.6	mJ
Avalanche current		I_{AR}	7.2	A
Repetitive avalanche energy (Note 2a) (Note 4)		E_{AR}	0.066	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

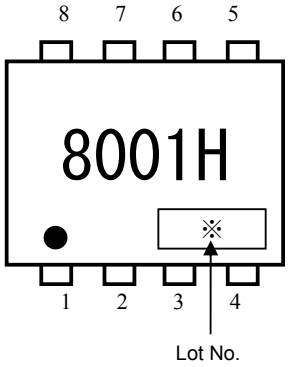
Note: For Notes 1 to 5, refer to the next page.

This transistor is an electrostatic-sensitive device. Handle with care.

Circuit Configuration



Marking (Note 5)

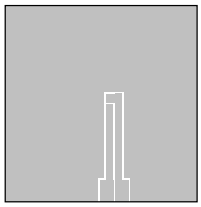


Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 5 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	74.4	°C/W
Thermal resistance, channel to ambient (t = 5 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	148.8	°C/W

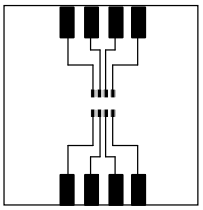
Note 1: The channel temperature should not exceed 150°C during use.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(a)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

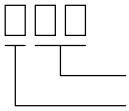
(b)

Note 3: V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 0.5 mH, R_G = 25 Ω, I_{AR} = 7.2A

Note 4: Repetitive rating: pulse width limited by max channel temperature

Note 5: ● on the lower left of the marking indicates Pin 1.

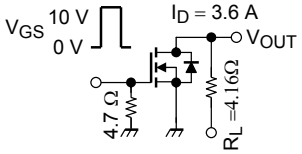
* Weekly code: (Three digits)



Week of manufacture
(01 for first week of the year, continuing up to 52 or 53)

Year of manufacture
(The last digit of the calendar year)

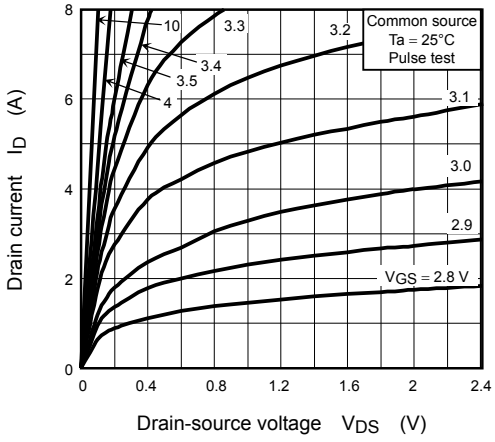
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cutoff current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	15	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.1	—	2.3	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 3.6 A	—	19	25	mΩ
			V_{GS} = 10 V, I_D = 3.6 A	—	13	16	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 3.6 A	8	16	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	640	—	pF
Reverse transfer capacitance		C_{rss}		—	75	—	
Output capacitance		C_{oss}		—	300	—	
Switching time	Rise time	t_r	 Duty ≦ 1%, t_w = 10 μs	—	4	—	ns
	Turn-on time	t_{on}		—	8	—	
	Fall time	t_f		—	4	—	
	Turn-off time	t_{off}		—	18	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ 24 V, V_{GS} = 10 V, I_D = 7.2 A	—	11	—	nC
			V_{DD} ≃ 24 V, V_{GS} = 5 V, I_D = 7.2 A	—	6.3	—	
Gate-source charge 1		Q_{gs1}	V_{DD} ≃ 24 V, V_{GS} = 10 V, I_D = 7.2 A	—	2.2	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	2.6	—	
Gate switch charge		Q_{SW}		—	3.6	—	

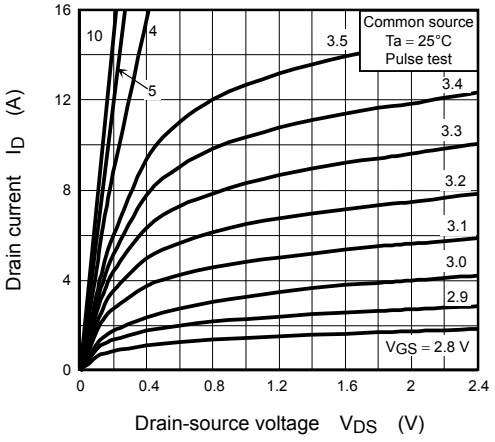
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	28.8	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 7.2 A, V_{GS} = 0 V	—	—	−1.2	V

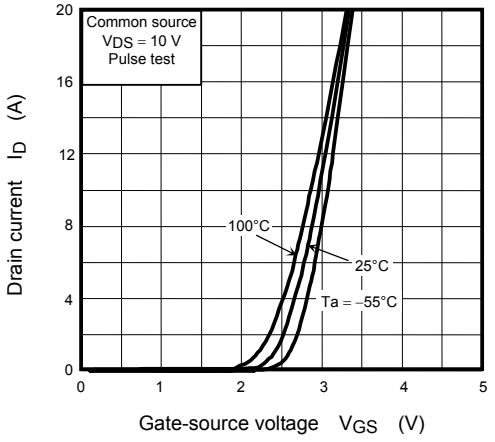
$I_D - V_{DS}$



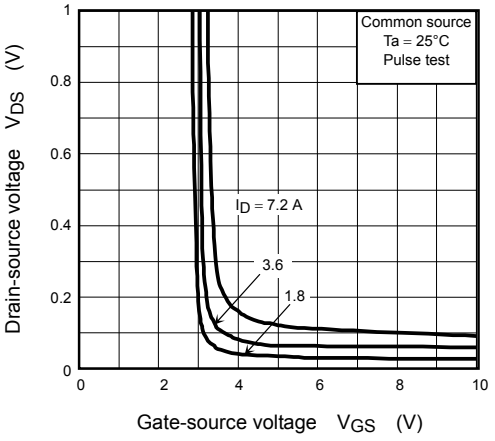
$I_D - V_{DS}$



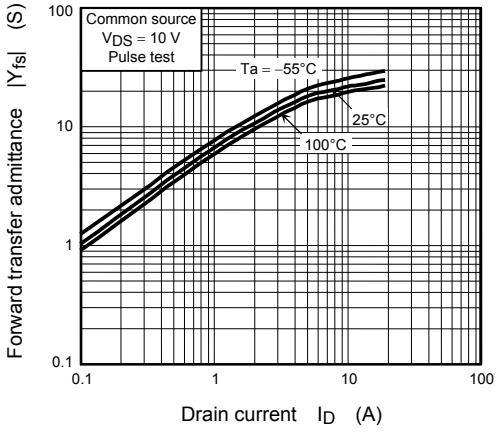
$I_D - V_{GS}$



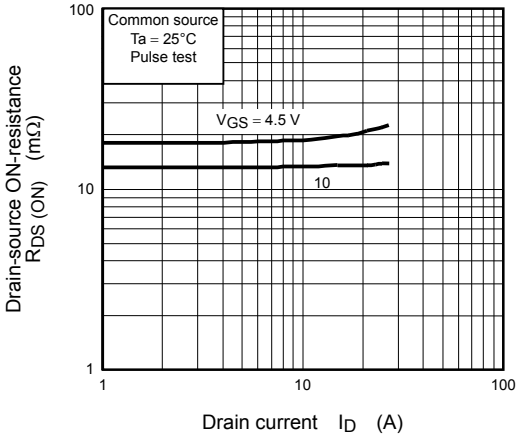
$V_{DS} - V_{GS}$



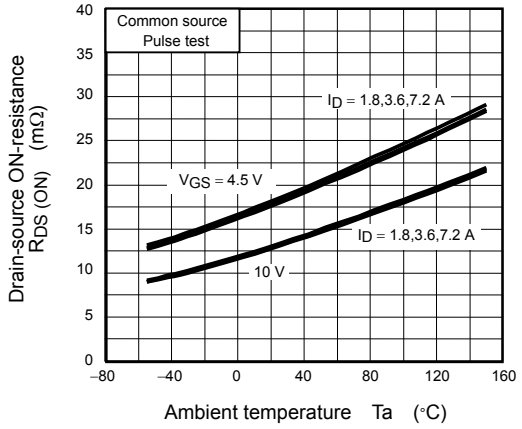
$|Y_{fs}| - I_D$



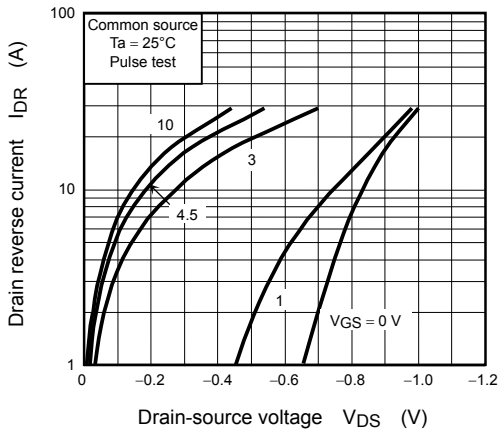
$R_{DS\ (ON)} - I_D$



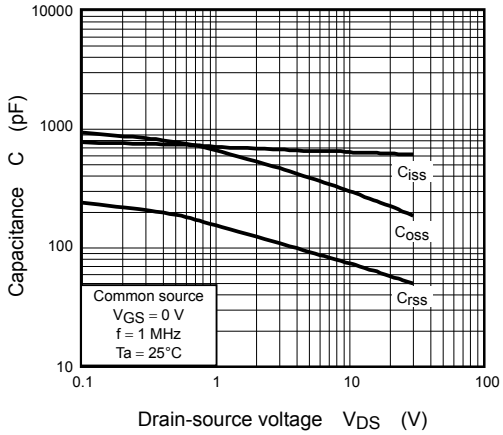
$R_{DS\ (ON)}$ – Ta



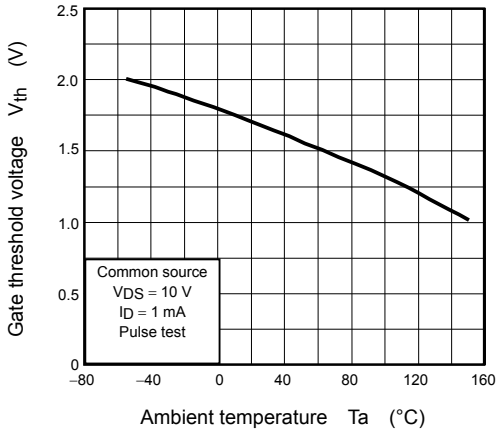
I_{DR} – V_{DS}



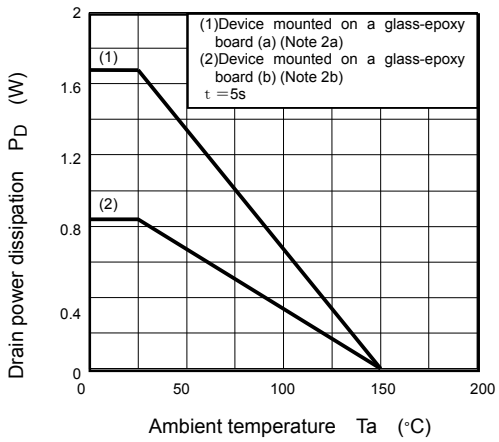
Capacitance – V_{DS}



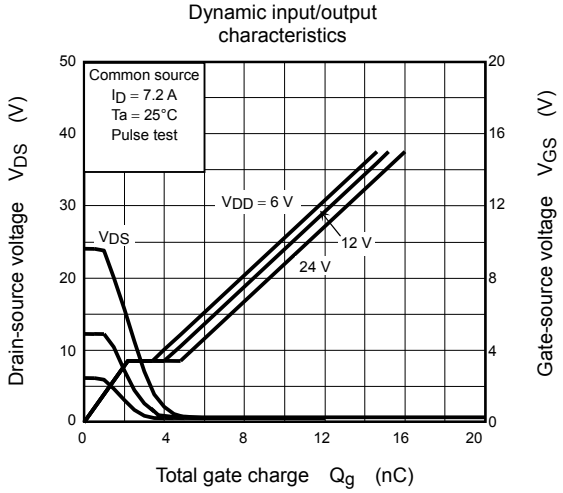
V_{th} – Ta



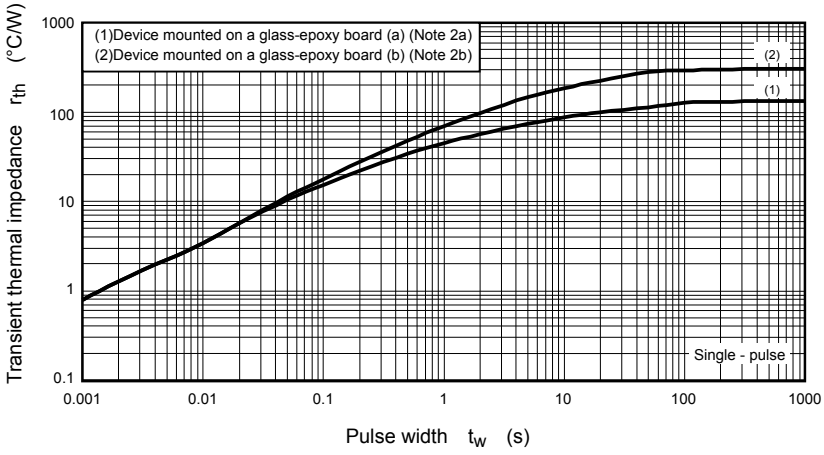
P_D – Ta



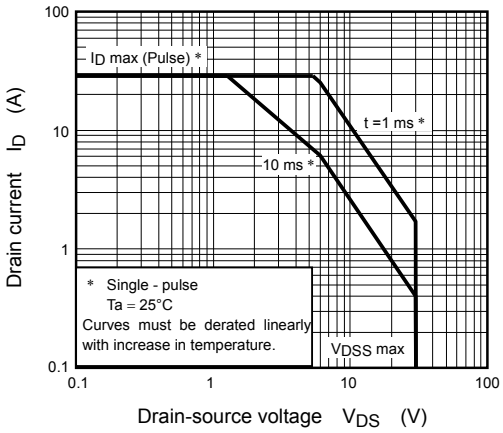
Dynamic input/output characteristics



$r_{th} - t_w$



Safe operating area



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