P-Channel Enhancement-Mode Vertical DMOS FET

Features

- Low threshold (-2.4V max.)
- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Medical Ultrasound imaging
- Non-destructive evaluation
- Solid state relays
- Telecom switches
- Logic level interfaces – ideal for TTL and CMOS

General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Option	BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$I_{D(ON)}$ (min) (A)
	3-Lead TO-252 (D-PAK)			
VP5225	VP5225K4	-250	3.0	-2.5

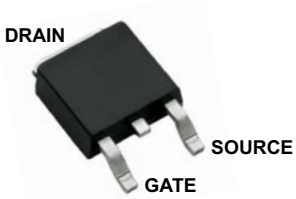
Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

** Distance of 1.6mm from case for 10 seconds.*

Pin Configuration



3-Lead TO-252 (D-PAK) (K4)

Product Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number

3-Lead TO-252 (D-PAK) (K4)

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Thermal Characteristics

Package	I_D (continuous)† (mA)	I_D (pulsed) (A)	Power Dissipation @T_A = 25°C (W)	θ_{jc} (°C/W)	θ_{ja} (°C/W)	I_{DR}† (mA)	I_{DRM} (A)
3-LeadTO-252 (D-PAK)	645	3.0	2.5‡	6.25	50‡	645	3.0

Notes:

† I_D (continuous) is limited by max rated T_j of 150°C.

‡ Mounted on FR4 board, 25mm x 25mm x 1.57mm

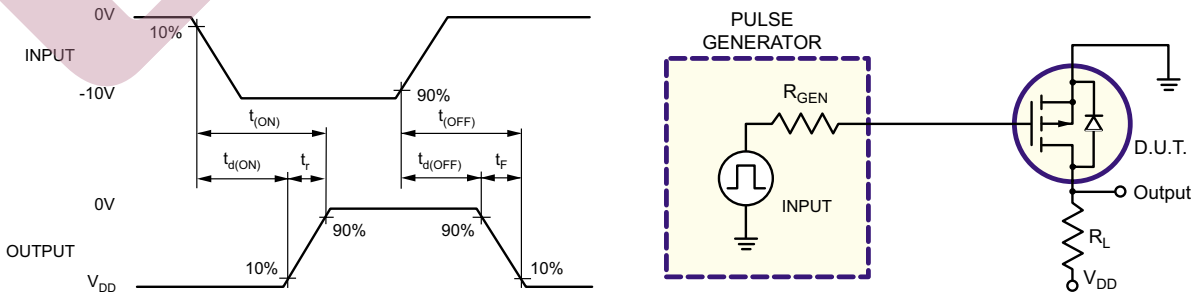
Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-250	-	-	V	V_{GS} = 0V, I_D = -250µA
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	V_{GS} = V_{DS}, I_D= -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	4.5	mV/°C	V_{GS} = V_{DS}, I_D= -1.0mA
I_{GSS}	Gate body leakage	-	-	-100	nA	V_{GS} = ± 20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	-10	µA	V_{GS} = 0V, V_{DS} = Max Rating
		-	-	-1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	-2.5	-	-	A	V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	5.0	Ω	V_{GS} = -4.5V, I_D = -250mA
		-	-	3.0		V_{GS} = -10V, I_D = -1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.7	%/°C	V_{GS} = -10V, I_D = -1.0A
G_{FS}	Forward transductance	500	-	-	mmho	V_{DS} = -25V, I_D = -200mA
C_{ISS}	Input capacitance	-	-	400	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	-	150		
C_{RSS}	Reverse transfer capacitance	-	-	50		
$t_{d(ON)}$	Turn-on delay time	-	-	20	ns	V_{DD} = -25V, I_D = -500mA, R_{GEN} = 25Ω
t_r	Rise time	-	-	30		
$t_{d(OFF)}$	Turn-off delay time	-	-	60		
t_f	Fall time	-	-	30		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	V_{GS} = 0V, I_{SD} = -500mA
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = -500mA

Notes:

1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit



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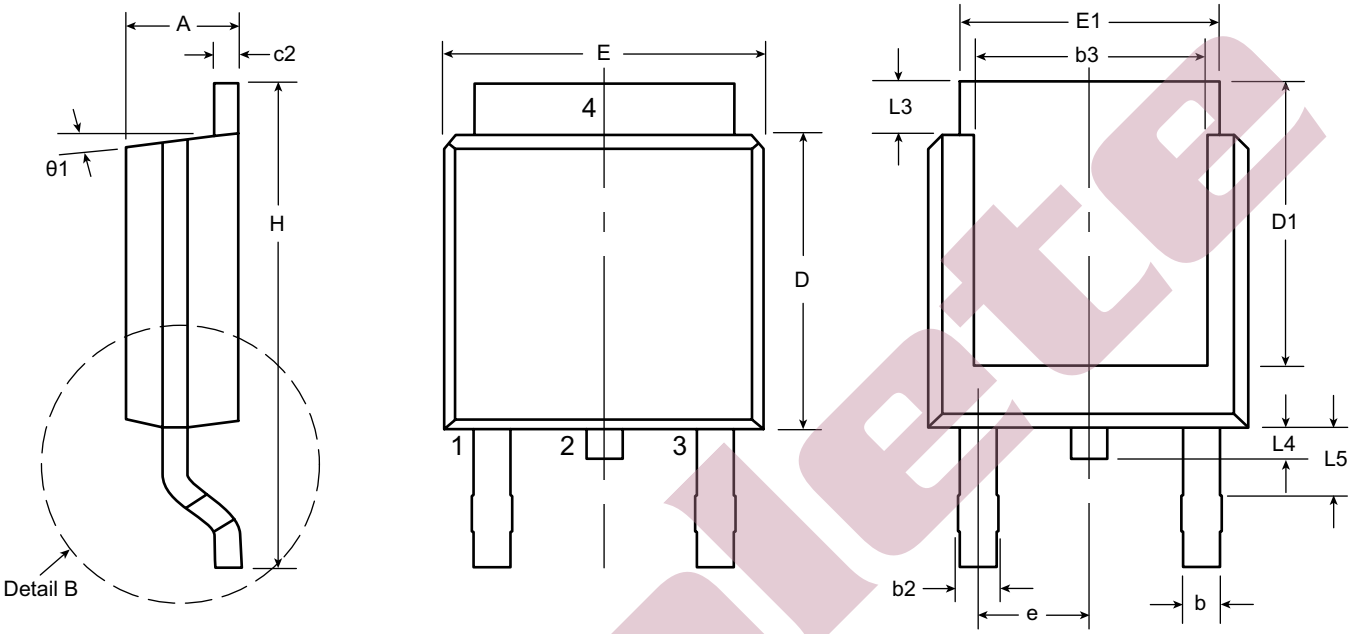
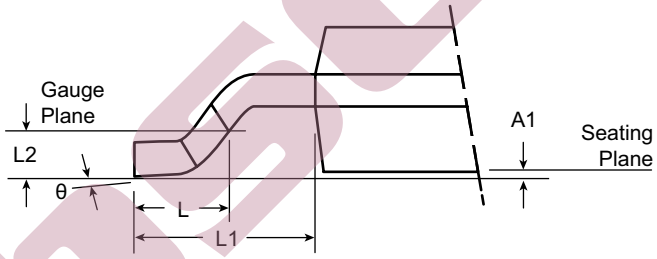
3-Lead TO-252 D-PAK Package Outline (K4)



Side View **Front View** **Rear View**



Detail B

Notes:

1. 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

Symbol		A	A1	b	b2	b3	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1
Dimension (inches)	MIN	.086	-	.025	.030	.195	.018	.235	.205	.250	.170	.090 BSC	.370	.055	.108 REF	.020 BSC	.035	-	.045	0^o	0^o
	NOM	-	-	-	-	-	-	.240	-	-	-		-	.060			-	-	-	-	-
	MAX	.094	.005	.035	.045	.215	.035	.245	-	.265	-		.410	.070			.050	.040	.060	10^o	15^o

JEDEC Registration TO-252, Variation AA, Issue E, June 2004.
Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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