



# ESDA14V2-2BF3

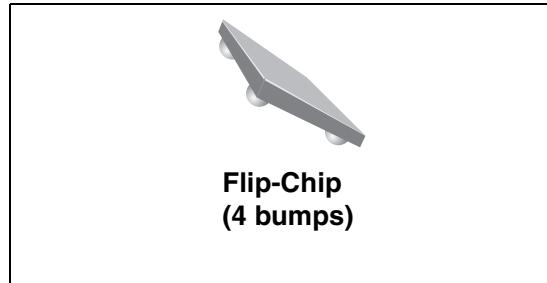
ASD (Application Specific Devices)  
Dual bidirectional TRANSIL™ array for ESD protection

## Application

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems and cellular phones
- Video equipment

This device is particularly adapted to the protection of symmetrical signals.



Flip-Chip  
(4 bumps)

## Description

The ESDA14V2-2BF3 is a monolithic array designed to protect 2 lines against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

## Features

- 2 Bidirectional Transil functions
- ESD Protection: IEC61000-4-2 level 4
- Stand off voltage: 12 V Min.
- Low leakage current
- Very small PCB area < 1.5 mm<sup>2</sup>
- 400 microns pitch

## Complies with the following standards:

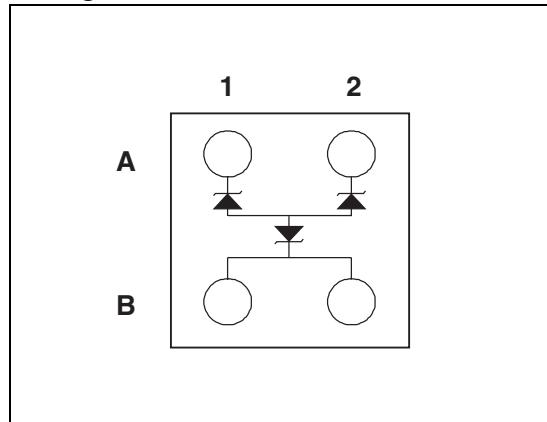
### IEC61000-4-2

15 kV (air discharge)  
8 kV (contact discharge)

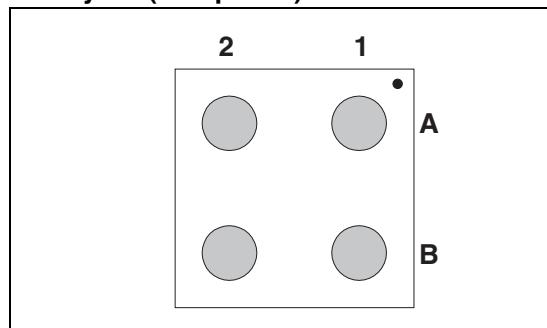
### MIL STD 883E- Method 3015-7: class3

25 kV (human body model)

## Configuration



## Pin layout (bump side)



## Order Code

Part number	Marking
ESDA14V2-2BF3	EG

TM: TRANSIL is a trademark of STMicroelectronics

December 2005

Rev 2  
1/9

[www.st.com](http://www.st.com)

# 1 Characteristics

## 1.1 Absolute maximum ratings ( $T_{amb} = 25^{\circ}\text{C}$ )

Symbol	Parameter	Value	Unit
$V_{PP}$	ESD discharge MIL STD 883E - Method 3015-7 IEC61000-4-2 air discharge IEC61000-4-2 contact discharge	$\pm 25$ $\pm 15$ $\pm 8$	kV
$P_{PP}$	Peak pulse power (8/20μs)	50	W
$T_j$	Junction temperature	125	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range	-55 to +150	$^{\circ}\text{C}$
$T_L$	Lead solder temperature (10 seconds duration)	260	$^{\circ}\text{C}$
$T_{op}$	Operating temperature range	-40 to +125	$^{\circ}\text{C}$

## 1.2 Electrical characteristics ( $T_{amb} = 25^{\circ}\text{C}$ )

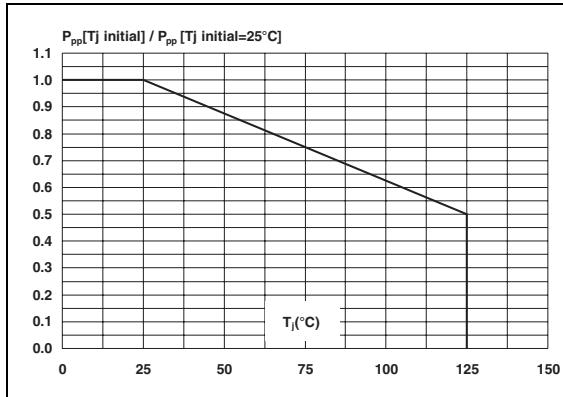
Symbol	Parameter		
$V_{BR}$	Breakdown voltage		
$I_{RM}$	Leakage current @ $V_{RM}$		
$V_{RM}$	Stand-off voltage		
$V_{CL}$	Clamping voltage		
$R_d$	Dynamic impedance		
$I_{PP}$	Peak pulse current		
$\alpha T$	Voltage temperature coefficient		
C	Capacitance		

Part Number	$V_{BR} @ I_R$			$I_{RM} @ V_{RM}$		$R_d$ typ. <sup>(1)</sup>	$\alpha T$ max. <sup>(2)</sup>	C typ. 0V bias
	min.	max.		max.				
ESDA14V2-2BF3	V	V	mA	μA	V	Ω	$10^{-4}/^{\circ}\text{C}$	pF
	14.2	18	1	0.5	12	3.2	6.5	12
				0.1	3			

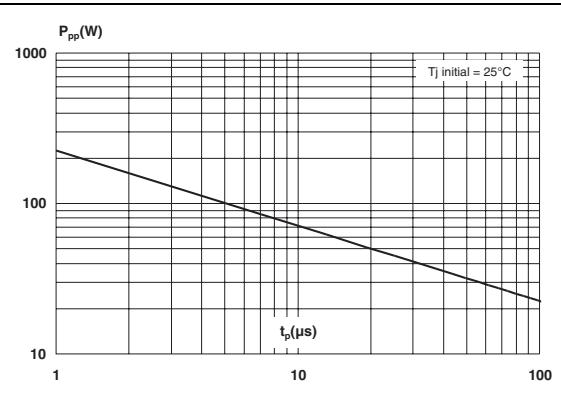
1. Square pulse,  $I_{PP} = 3\text{A}$ ,  $t_p = 2.5\mu\text{s}$ .

2.  $\Delta V_{BR} = \alpha T (T_{amb} - 25^{\circ}\text{C}) \times V_{BR} (25^{\circ}\text{C})$

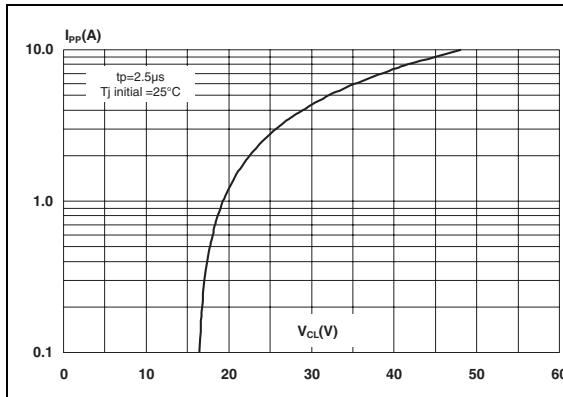
**Figure 1. Relative variation of peak pulse power versus initial junction temperature**



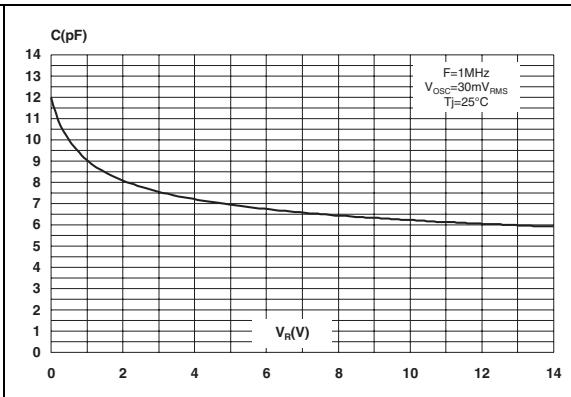
**Figure 2. Peak pulse power versus exponential pulse duration**



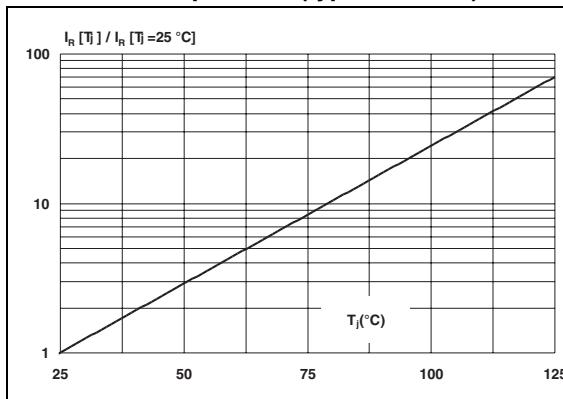
**Figure 3. Clamping voltage versus peak pulse current (typical values, rectangular waveform)**



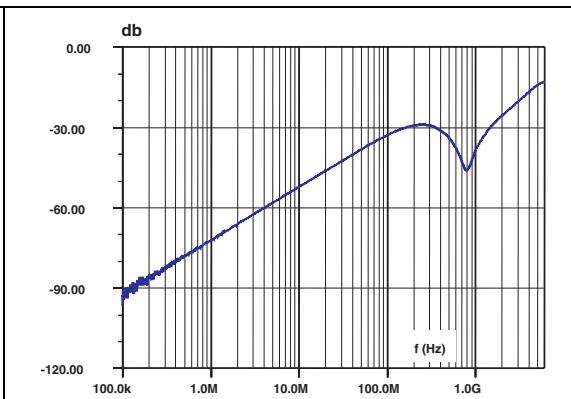
**Figure 4. Junction capacitance versus reverse applied voltage (typical values)**

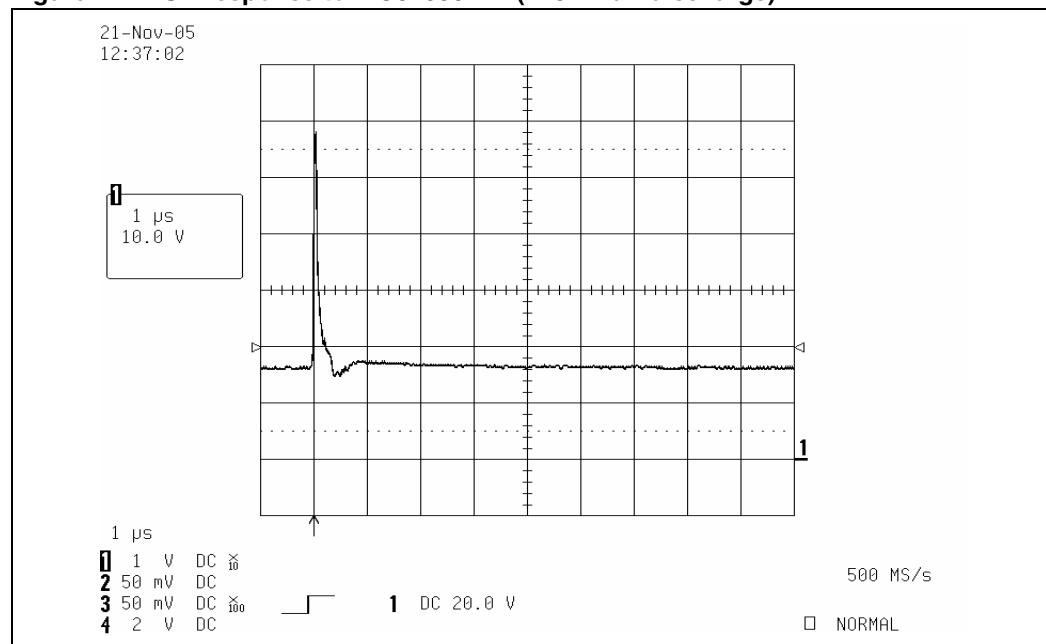
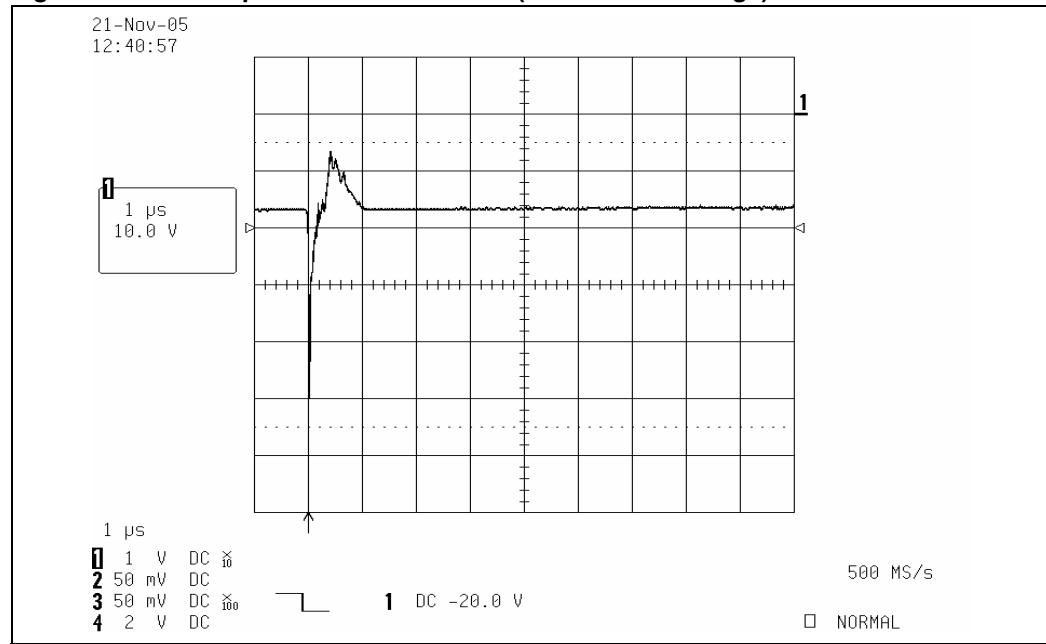


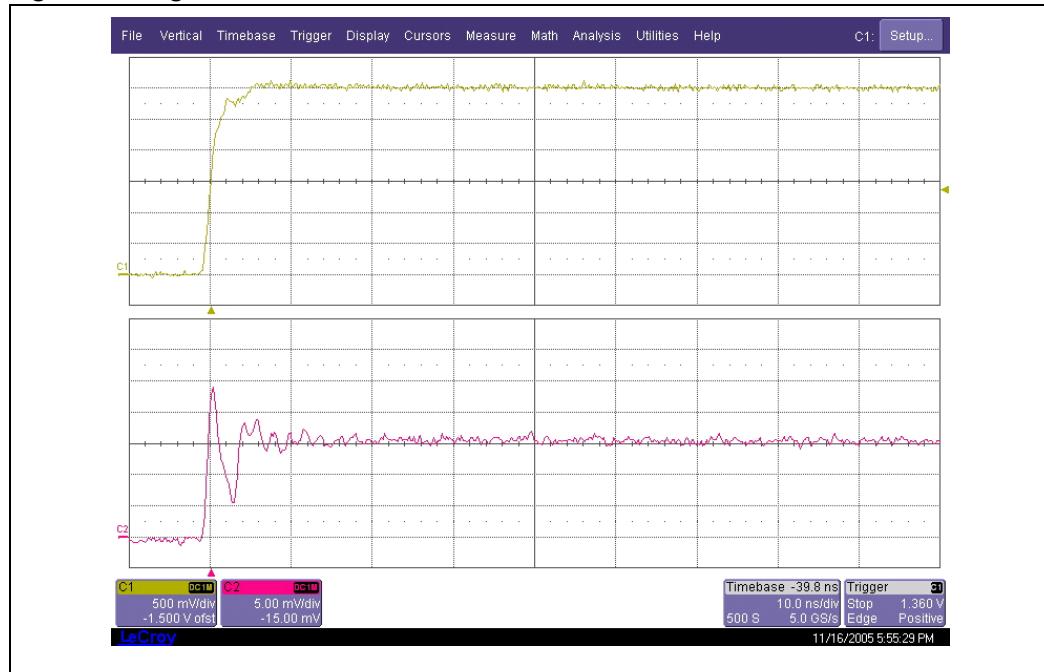
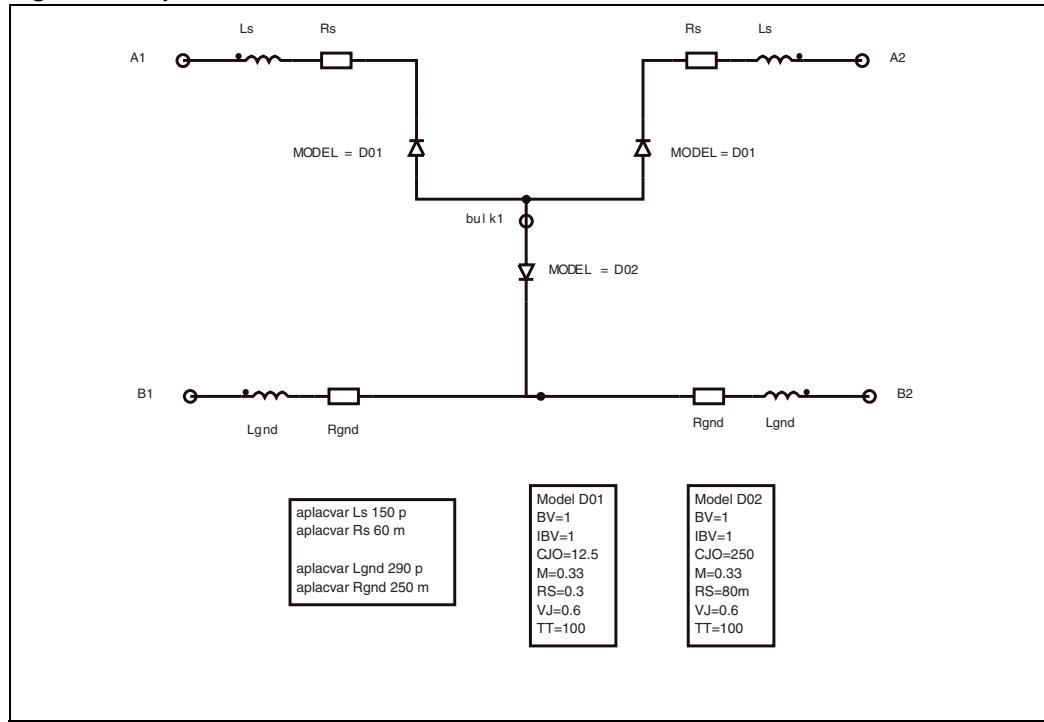
**Figure 5. Relative variation of leakage current versus junction temperature (typical values)**



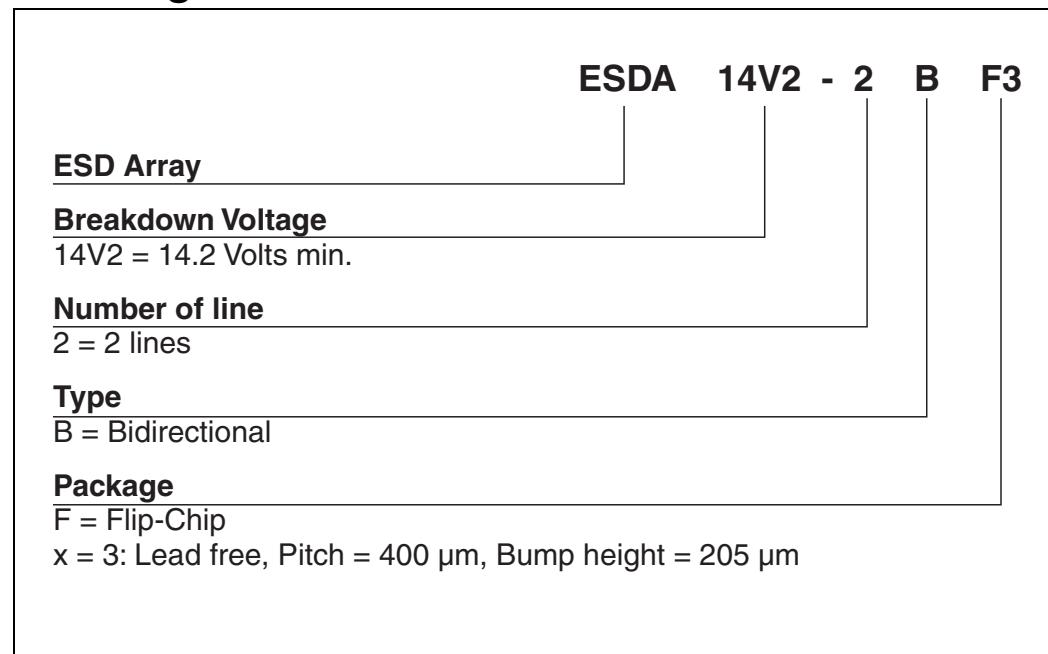
**Figure 6. Analog crosstalk measurements**



**Figure 7. ESD response to IEC61000-4-2 (+15 kV air discharge)****Figure 8. ESD response to IEC61000-4-2 (-15 kV air discharge)**

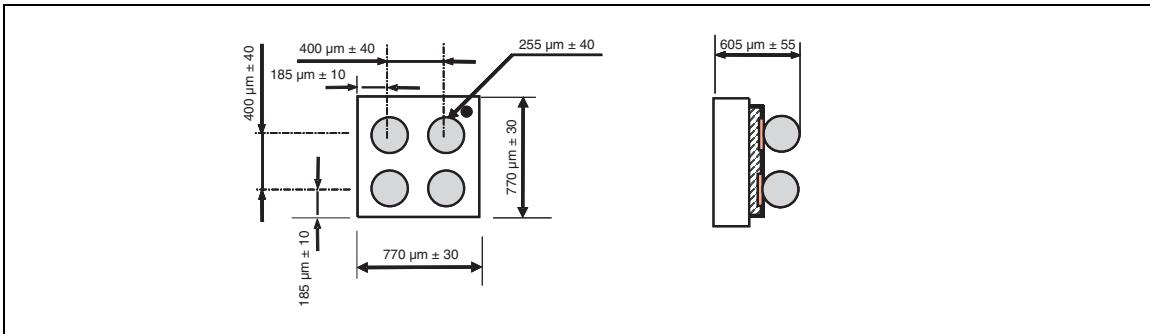
**Figure 9.** Digital crosstalk measurements**Figure 10.** Aplac model

## 2 Ordering information scheme

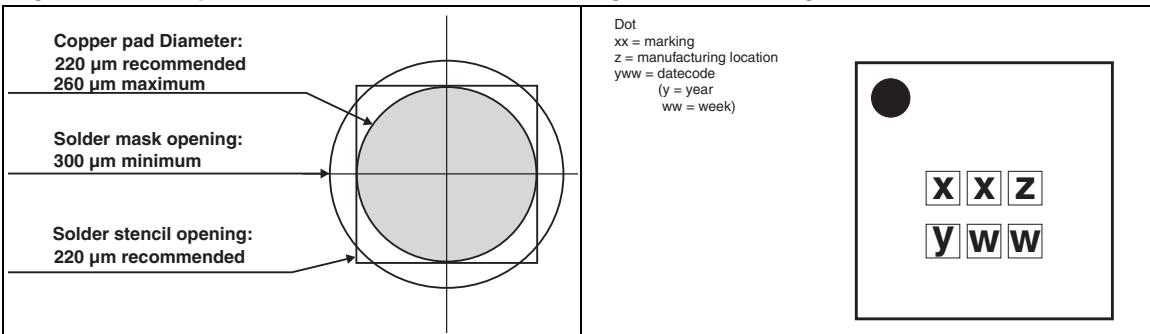


### 3 Package information

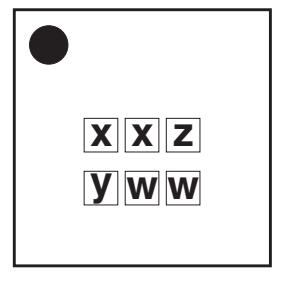
**Figure 11. Mechanical data**



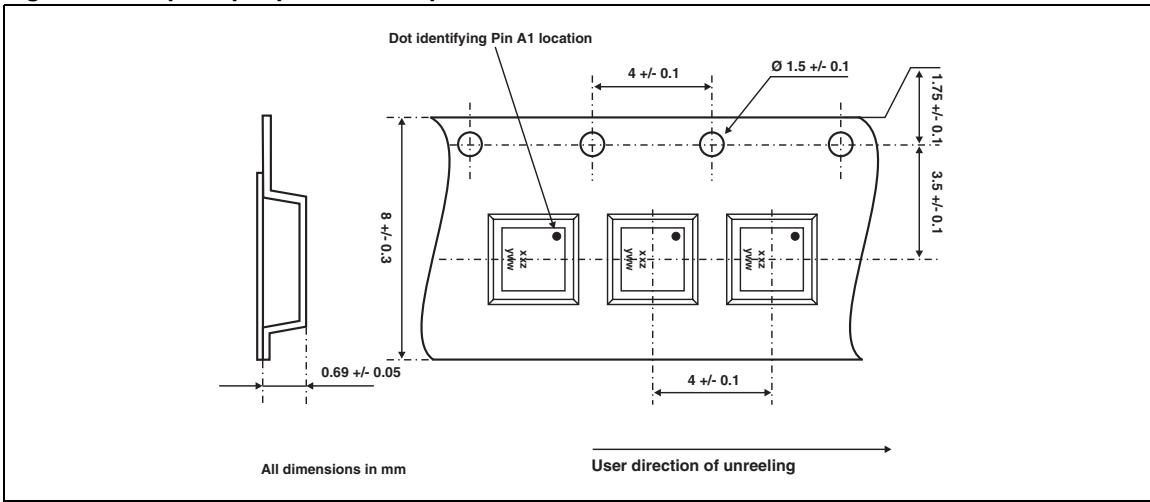
**Figure 12. Footprint recommendations**



**Figure 13. Marking**



**Figure 14. Flip-Chip tape and reel specifications**



Note: more information is available in the application notes:  
 AN1235: "Flip Chip: Package description and recommendations for use"  
 AN1751: "EMI Filters: Recommendations and measurements"

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

## 4 Ordering information

Part number	Marking	Package	Weight	Base qty	Delivery mode
ESDA14V2-2BF3	EG	Flip-Chip	0.79 mg	5000	Tape and reel 7"

## 5 Revision history

Date	Revision	Changes
02-Dec-2005	1	Initial release.
15-Dec-2005	2	Ordering information changed.

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