# MAATCC0011

## Digital Attenuator
## 31.5 dB, 6-Bit, TTL Driver, DC-4.0 GHz

Rev. V5

### Features

- Attenuation: 0.5 dB Steps to 31.5 dB
- Single Positive Supply
- Contains internal DC to DC converter
- Low DC Power Consumption
- Small Footprint, JEDEC Package
- Integral TTL Driver
- 50 ohm Impedance
- Lead-Free CSP-1 Package
- 100% Matte Tin Plating over Copper
- Halogen-Free "Green" Mold Compound
- 260°C Reflow Compatible
- RoHS* Compliant Version of AT90-1107

### Description

M/A-COM's MAATCC0011 is a GaAs FET 6-bit digital attenuator with integral TTL driver. Step size is 0.5 dB providing a 31.5 dB total attenuation range. This device is in an PQFN plastic surface mount package. The MAATCC0011 is ideally suited for use where accuracy, fast speed, very low power consumption and low costs are required. For dual supply designs without switching noise, use MAATCC0009.

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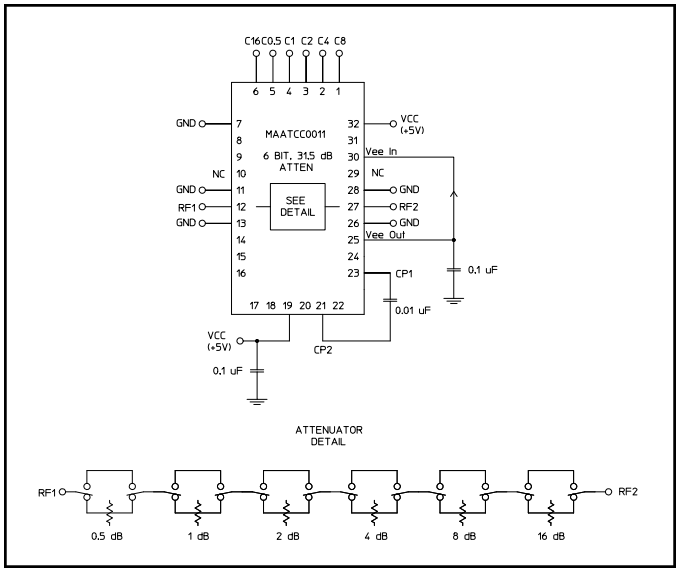
### Ordering Information

| Part Number | Package |
|---|---|
| MAATCC0011 | Bulk Packaging |
| MAATCC0011TR | 1000 piece reel |
| MAATCC0011-TB | Sample Test Board |

Note: Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

### Schematic with Off-Chip Components




### Pin Configuration[3]

| Pin No. | Function | Pin No. | Function |
|---|---|---|---|
| 1 | C8 | 17 | NC |
| 2 | C4 | 18 | NC |
| 3 | C2 | 19 | Vcc |
| 4 | C1 | 20 | NC |
| 5 | C0.5 | 21 | Cp |
| 6 | C16 | 22 | NC |
| 7 | GND | 23 | Cp |
| 8 | NC | 24 | NC |
| 9 | NC | 25 | $V_{EE}$[2] |
| 10 | NC[1] | 26 | GND |
| 11 | GND | 27 | RF2 |
| 12 | RF1 | 28 | GND |
| 13 | GND | 29 | NC[1] |
| 14 | NC | 30 | $V_{EE}$[2] |
| 15 | NC | 31 | NC |
| 16 | NC | 32 | Vcc |

1. Pins 10 and 29 must be isolated.
2. VEE is produced internally and requires a .1 µF cap to GND. Generated noise is typical of switching DC-DC Converters.
3. The exposed pad centered on the package bottom must be connected to RF and DC ground. (For PQFN Packages)





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## Electrical Specifications: $T_A$ = +25°C

| Parameter | Test Conditions | Frequency | Units | Min | Typ | Max |
|---|---|---|---|---|---|---|
| Insertion Loss | — | DC - 4.0 GHz | dB | — | 4.5 | 5.1 |
| Attenuation Accuracy | Individual Bits 0.5-1-2-4-8-16 dB<br>Any Combination of Bits 1 to 31.5 dB | DC - 4.0 GHz<br>DC - 4.0 GHz | dB<br>dB | —<br>— | —<br>— | ±(.3 +7% of atten setting)<br>±(.5 +8% of atten setting) |
| VSWR | Full Range | DC - 4.0 GHz | Ratio | — | 2.0:1 | 2.2:1 |
| Switching Speed | 50% Cntl to 90%/10% RF<br>10% to 90% or 90% to 10% | —<br>— | nS<br>nS | —<br>— | 75<br>20 | —<br>— |
| 1 dB Compression | —<br>— | 50 MHz<br>0.5 - 4.0 GHz | dBm<br>dBm | —<br>— | +21<br>+24 | —<br>— |
| Input $IP_3$ | Two-tone inputs up to +5 dBm | 50 MHz<br>0.5-4.0 GHz | dBm<br>dBm | —<br>— | +35<br>+48 | —<br>— |
| Vcc | — | — | V | 4.75 | 5.0 | 5.25 |
| $V_{IL}$<br>$V_{IH}$ | LOW-level input voltage<br>HIGH-level input voltage | —<br>— | V<br>V | 0.0<br>2.0 | —<br>— | 0.8<br>5.0 |
| Iin (Input Leakage Current) | Vin = $V_{CC}$ or GND | — | uA | -1.0 | — | 1.0 |
| Icc[4] | Vcc min to max, Logic “0” or “1” | — | mA | — | 6 | 10 |
| Turn-on Current[5] | For guaranteed start-up | — | mA | — | — | 125 |
| ΔIcc (Additional Supply Current Per TTL Input Pin) | $V_{CC}$ = Max, Vcntrl = $V_{CC}$ - 2.1 V | — | mA | — | — | 1.0 |
| Switching Noise | Generated from DC-DC Converter with recommended capacitors | 3.5 MHz | dBm | — | -93 | — |
| Thermal Resistance θjc | — | — | °C/W | — | 15 | — |

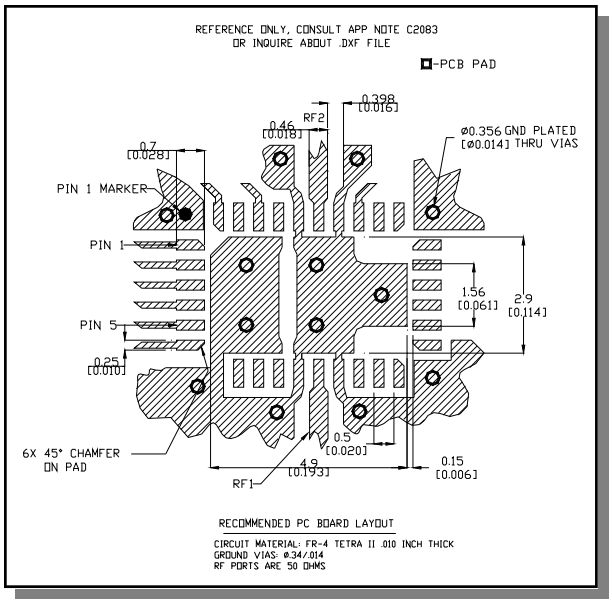
4. During turn-on, the device requires an initial “Turn-on Current”. Once operational, Icc will drop to the specified levels.
5. The DC-DC converter is guaranteed to start in 100 µs as long as the power supplies can provide a minimum of 100 mA “Turn-on Current”.

## Absolute Maximum Ratings[6,7]

| Parameter | Absolute Maximum |
|---|---|
| Max. Input Power<br>0.05 GHz<br>0.5 - 4.0 GHz | <br>+27 dBm<br>+34 dBm |
| $V_{CC}$ | -0.5V ≤ $V_{CC}$ ≤ +6.0V |
| Vin[8] | -0.5V ≤ Vin ≤ $V_{CC}$ + 0.5V |
| Operating Temperature | -40ºC to +85ºC |
| Storage Temperature | -65ºC to +125ºC |

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. M/A-COM does not recommend sustained operation near these survivability limits.
8. Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

## Recommended PCB Configuration[9]




9. Application Note S2083 is available on line at www.macom.com





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## Handling Procedures

Please observe the following precautions to avoid damage:

## Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

## Moisture Sensitivity

The MSL rating for this part is defined as Level 2 per IPC/JEDEC J-STD-020. Parts shall be stored and/or baked as required for MSL Level 2 parts.

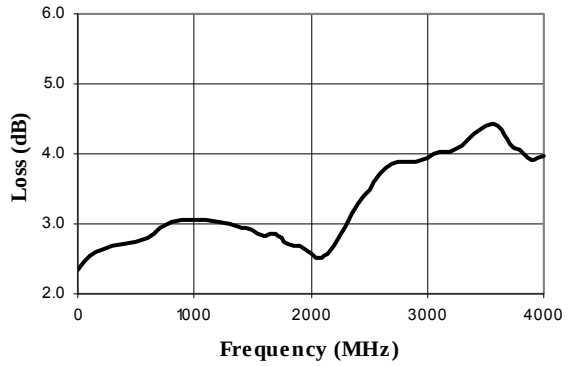
## Truth Table (Digital Attenuator)

| C16 | C8 | C4 | C2 | C1 | C0. | Attenuation |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Loss, Reference |
| 0 | 0 | 0 | 0 | 0 | 1 | 0.5 dB |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.0 dB |
| 0 | 0 | 0 | 1 | 0 | 0 | 2.0 dB |
| 0 | 0 | 1 | 0 | 0 | 0 | 4.0 dB |
| 0 | 1 | 0 | 0 | 0 | 0 | 8.0 dB |
| 1 | 0 | 0 | 0 | 0 | 0 | 16.0 dB |
| 1 | 1 | 1 | 1 | 1 | 1 | 31.5 dB |

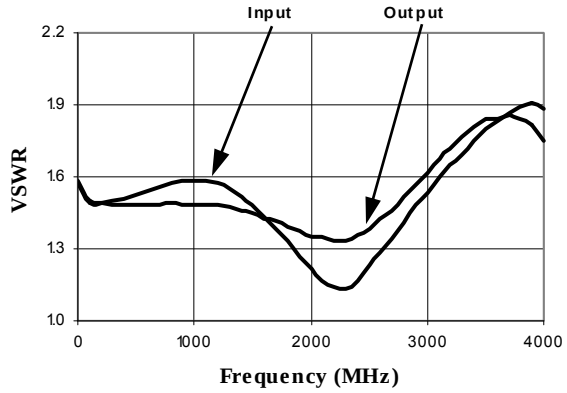
0 = TTL Low; 1 = TTL High

## Typical Performance Curves

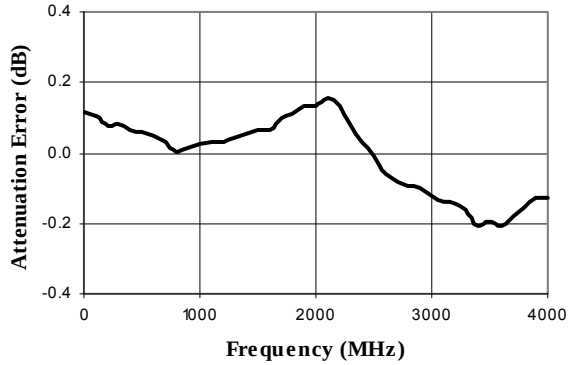
***Insertion Loss***



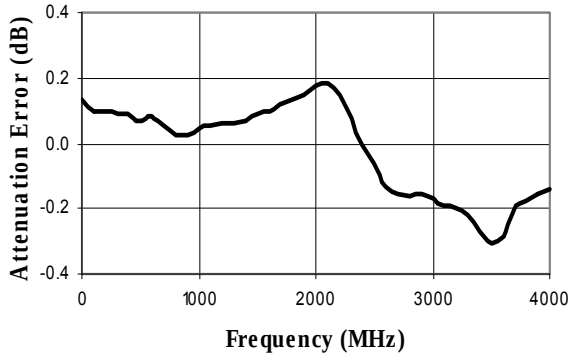

***VSWR @ Insertion Loss***




***Attenuation Error, 0.5 dB Bit***




***Attenuation Error, 1 dB Bit***





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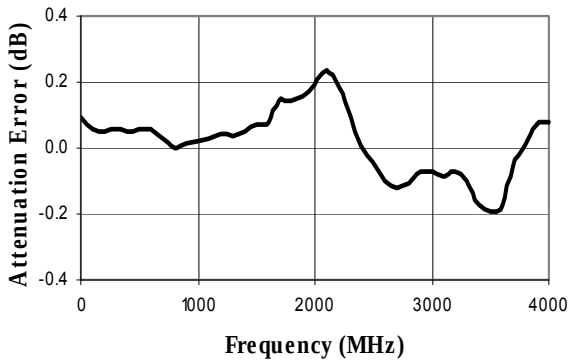
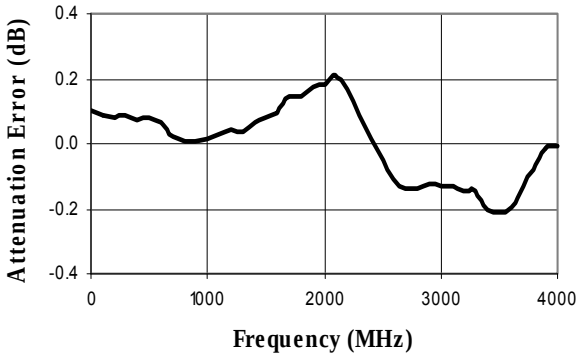
## Typical Performance Curves

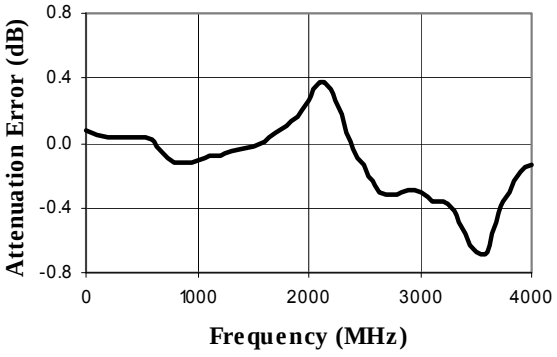
***Attenuation Error, 2 dB Bit***



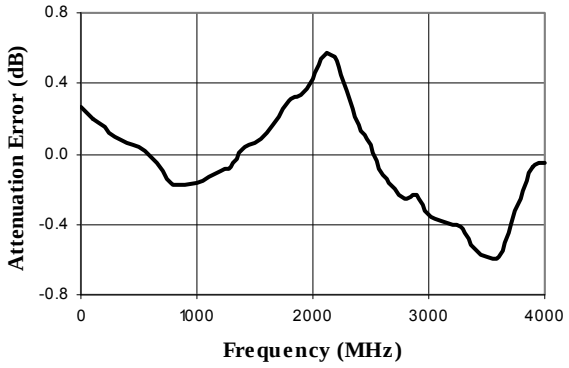

***Attenuation Error, 4 dB Bit***



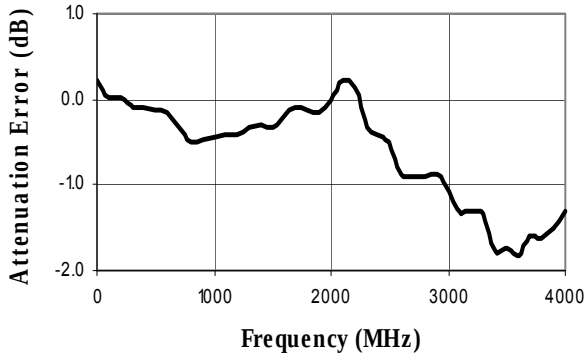

***Attenuation Error, 8 dB Bit***



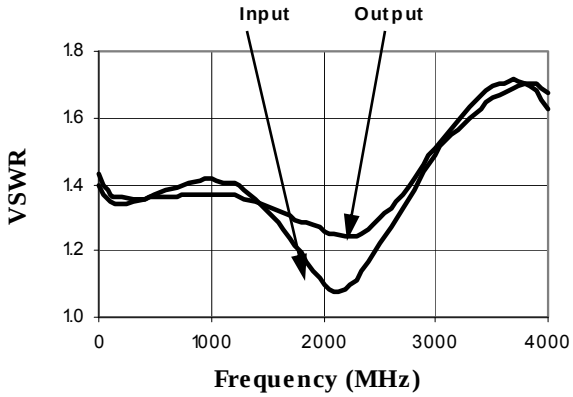

***Attenuation Error, 16 dB Bit***




***Attenuation Error, Max. Attenuation***




***VSWR, 0.5 dB Bit***





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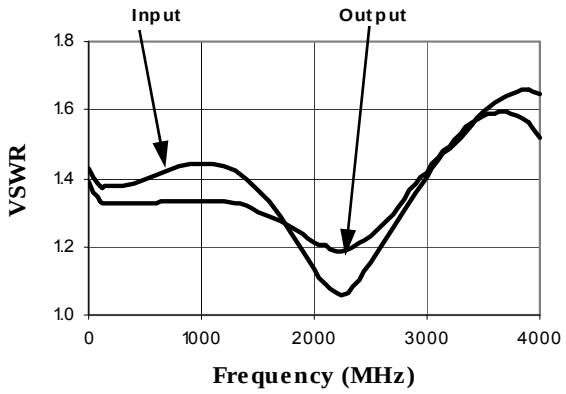
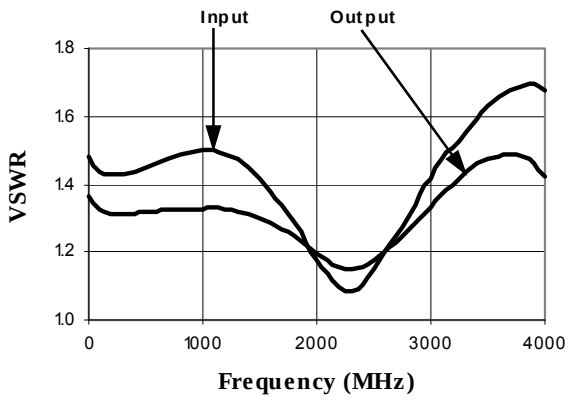
## Typical Performance Curves

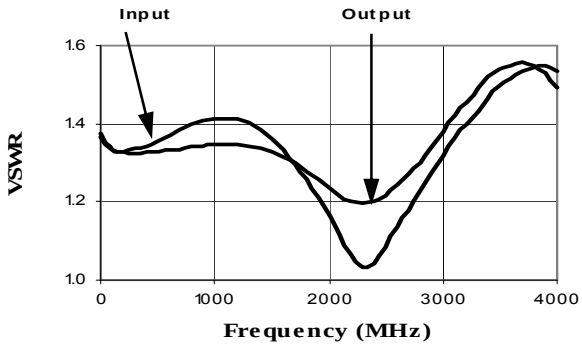
***VSWR, 1 dB Bit***



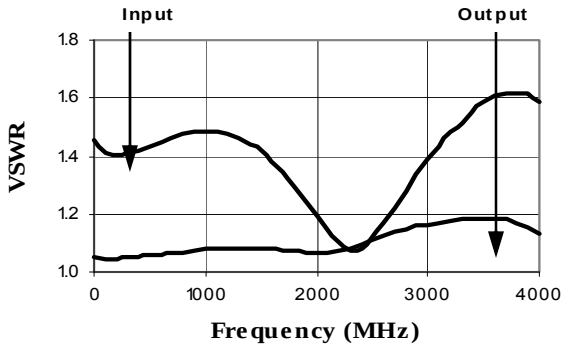

***VSWR, 2 dB Bit***



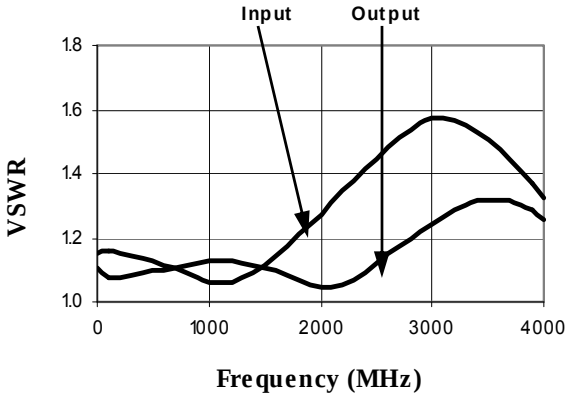

***VSWR, 4 dB Bit***



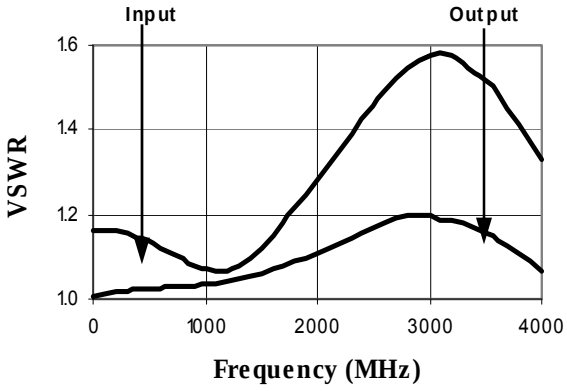

***VSWR, 8 dB Bit***




***VSWR, 16 dB Bit***




***VSWR, Max. Attenuation***





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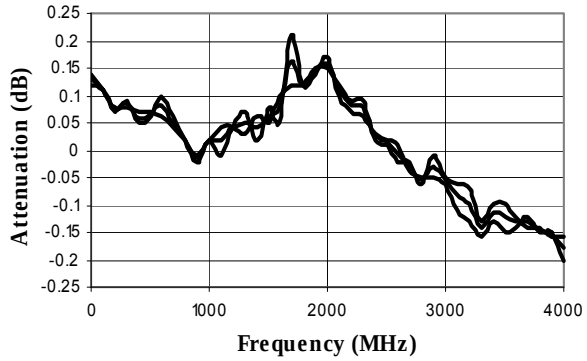
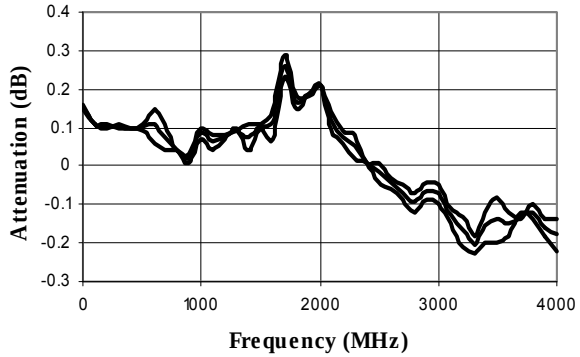
## Typical Performance Curves

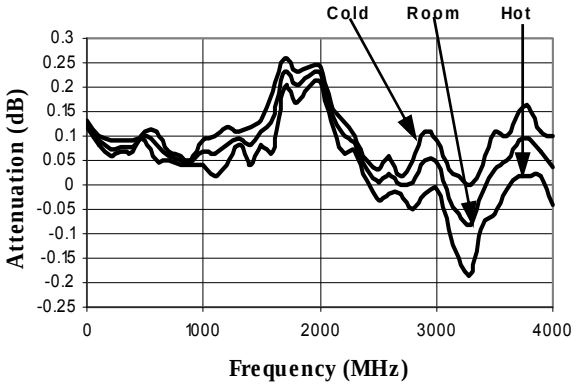
***Typical Attenuation Deviation vs. Temperature for 0.5 dB Bit***



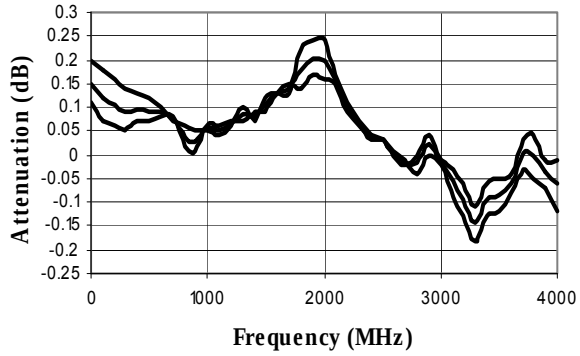

***Typical Attenuation Deviation vs. Temperature for 1 dB Bit***



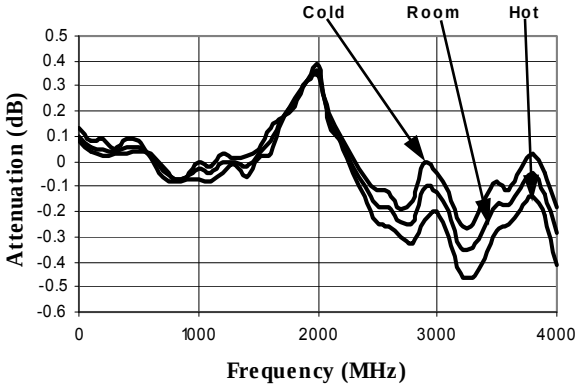

***Typical Attenuation Deviation vs. Temperature for 2 dB Bit***



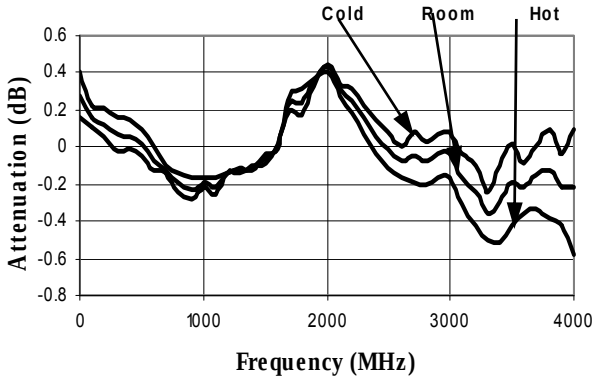

***Typical Attenuation Deviation vs. Temperature for 4 dB Bit***




***Typical Attenuation Deviation vs. Temperature for 8 dB Bit***




***Typical Attenuation Deviation vs. Temperature for 16 dB Bit***





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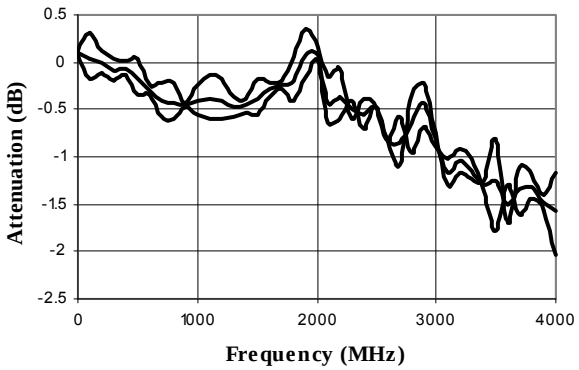
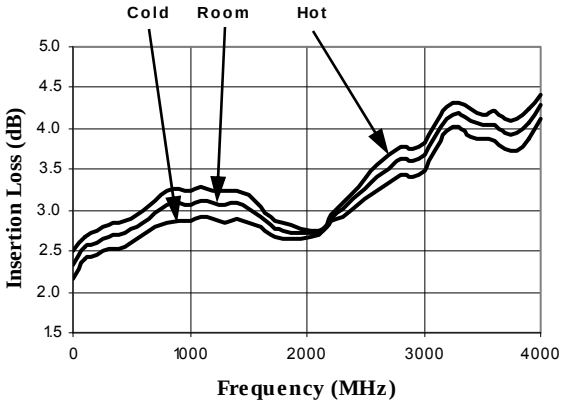
## Typical Performance Curves

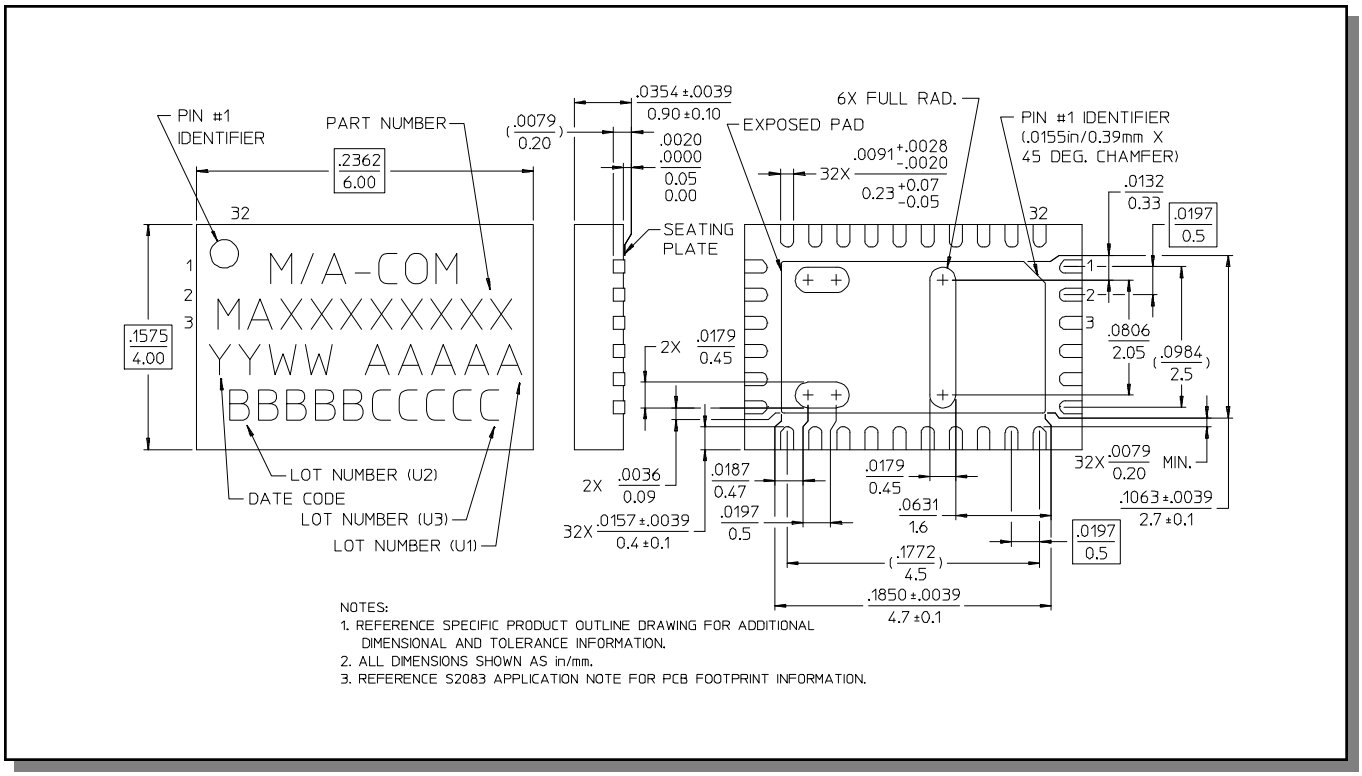
***Typical Attenuation Deviation vs. Temperature at Maximum Attenuation***




***Insertion Loss vs. Temperature***




## *CSP-1, Lead-Free* 4 x 6 mm, 32-lead PQFN†




† Reference Application Note M538 for lead-free solder reflow recommendations.





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