

### GENERAL DESCRIPTION

The PT6105 is a highly integrated, digitally programmable, charging/discharging management IC for 3 to 7 serially connected Li-Ion or LiFePO<sub>4</sub> batteries used in portable electrical tools or other multi-cell battery powered systems. It contains a multi-channel 10-bit ADC digitizing battery voltages, environment temperature, and battery discharge current. The converted data is transferred to MCU via I<sup>2</sup>C interface and is used for battery balancing and safety protections against battery over-voltage, under-voltage, discharging over current, and over temperature. The integrated battery balance circuitry could deliver a programmable shunt current as high as 200mA without the need of external transistors. The PT6105 buffers both DC and PWM (Pulse Width Modulation) MOSFET control signals generated from MCU to drive an electrical motor.

Key parameters in the PT6105 are programmable by a microprocessor through an I<sup>2</sup>C interfacing port, which features customers to achieve flexible and optimal multi-cell Li-ion/LiFePO<sub>4</sub> battery charging/discharging progress control and safety protection. The package is QFN-24.

### PIN ASSIGNMENT

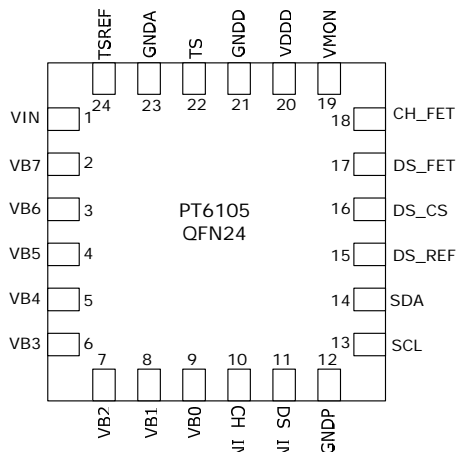


Figure 1. Pin order in QFN-24 package

### FEATURES

#### Charging Control

- 3~7 Li-ion or LiFePO<sub>4</sub> battery cells system
- Cell balancing with programmable shunt currents up to 200mA
- Accurately sensing battery cell voltages and temperature through a 10-bit ADC.
- MCU controlled protection cutoff voltages.

#### Discharging

- Programmable discharge over-current or short-circuit protection thresholds
- MCU controlled battery under-voltage protection thresholds
- 10~15V PWM or DC MOSFET gate driving voltages
- 200mA maximum MOSFET gate driving current
- Load protection to prevent discharging on short-circuit or light load between two terminals connected to the motor

#### MCU Interfacing

- A 10-bit ADC samples up to 7 individual cell voltages, environmental temperature, and discharge current.
- ADC sampling time <20ms through all channels
- ADC fail bit indicates overflow
- 100 kHz I<sup>2</sup>C communication port
- 2 seconds watchdog function for MUC.
- 5~3.2V supply voltage to MCU

#### Other Protections

- 6V under voltage lockout voltage (UVLO)
- Protected from <1.0ms negation glitch toward ground generated from battery pack
- Internal over temperature shutdown (TSD)

**PIN DESCRIPTION**

| Pin # | Function                         | Name   | Description   |
|-------|----------------------------------|--------|---|
| 1     | Battery voltage input            | VIN    | Power supply  |
| 2     |                                  | VB7    | Battery cell 7 voltage input  |
| 3     |                                  | VB6    | Battery cell 6 voltage input  |
| 4     |                                  | VB5    | Battery cell 5 voltage input  |
| 5     |                                  | VB4    | Battery cell 4 voltage input  |
| 6     |                                  | VB3    | Battery cell 3 voltage input  |
| 7     |                                  | VB2    | Battery cell 2 voltage input  |
| 8     |                                  | VB1    | Battery cell 1 voltage input  |
| 9     |                                  | VB0    | This pin connects to the most negative terminal in the battery string |
| 10    | Charging/<br>discharging control | CH_IN  | Charge control signal in  |
| 11    |                                  | DS_IN  | Discharge control signal in   |
| 12    |                                  | GNDP   | Connect to ground   |
| 15    | Charging/<br>discharging control | DS_REF | Discharging current sense reference                                   |
| 16    |                                  | DS_CS  | Discharging current sense monitor                                     |
| 17    |                                  | DS_FET | Discharge MOSFET gate drive   |
| 18    |                                  | CH_FET | Charge MOSFET gate drive  |
| 19    |                                  | VMON   | Discharge load monitoring for short circuit protection                |
| 13    | Interface<br>with MCU            | SCL    | Serial clock  |
| 14    |                                  | SDA    | Serial data   |
| 20    |                                  | VDDD   | Regulated 5V supply voltage to MCU and E <sup>2</sup> PROM            |
| 21    |                                  | GNDD   | Digital ground  |
| 22    |                                  | TS     | Temperature monitor input   |
| 23    | Analog power<br>supply           | GNDA   | Analog ground   |
| 24    |                                  | TSREF  | TS input reference voltage  |

**TYPICAL APPLICATION EXAMPLE**

Q1 and Q2 are MOSFET switches controlled by two gate driving voltages CH\_FET and DS\_FET. Their functions are described in Table 2.

| CH_FET     | DS_FET     | Operation status  |
|------------|------------|---|
| 1 (or PWM) | 1 (or PWM) | Battery charging or discharging   |
| 0          | 0          | 1) Battery charging/discharging safety protection<br>2) Battery standby |

**Table 2. The functions of charging/discharging control switched**

Please note that Q1 and Q2 could be not only turned on by DC voltage, but also by a PWM sequence. D2 and R1 are added for short circuit loading protection during

battery discharging. D3 limits the gate-source voltage of Q1 to be less than 15V. D4 and R2 are used to protect the CH\_FET pin from being damaged by the

## Multi-cell Battery Management Front End with I<sup>2</sup>C Interface

flyback voltage from the motor windings, when the CH\_FET is opened suddenly for over current or short circuit shut-down.

The only positive power supply voltage terminal of the chip is VIN. D1, C1, and C2 are added to stabilize the chip power supply in case of a positive or negative voltage surge coming from the battery or motor. GNDA and GNDD are internally generated supplies. "VB0" is connected to ground but is only used for the measurements of VB1 and external temperature.

Rt is a thermal resistor to sense the battery pack temperature. R5 and R6 are used for linearization. R4 and C4 filter noise added on the sensed discharge current and provide a certain time delay for over current protection., R8 and D5 are used for the protection of chip DS\_CS input from the transient high voltage impulse when the system begins discharging operation.

D1 is suggested to be removed if there are only three batteries.

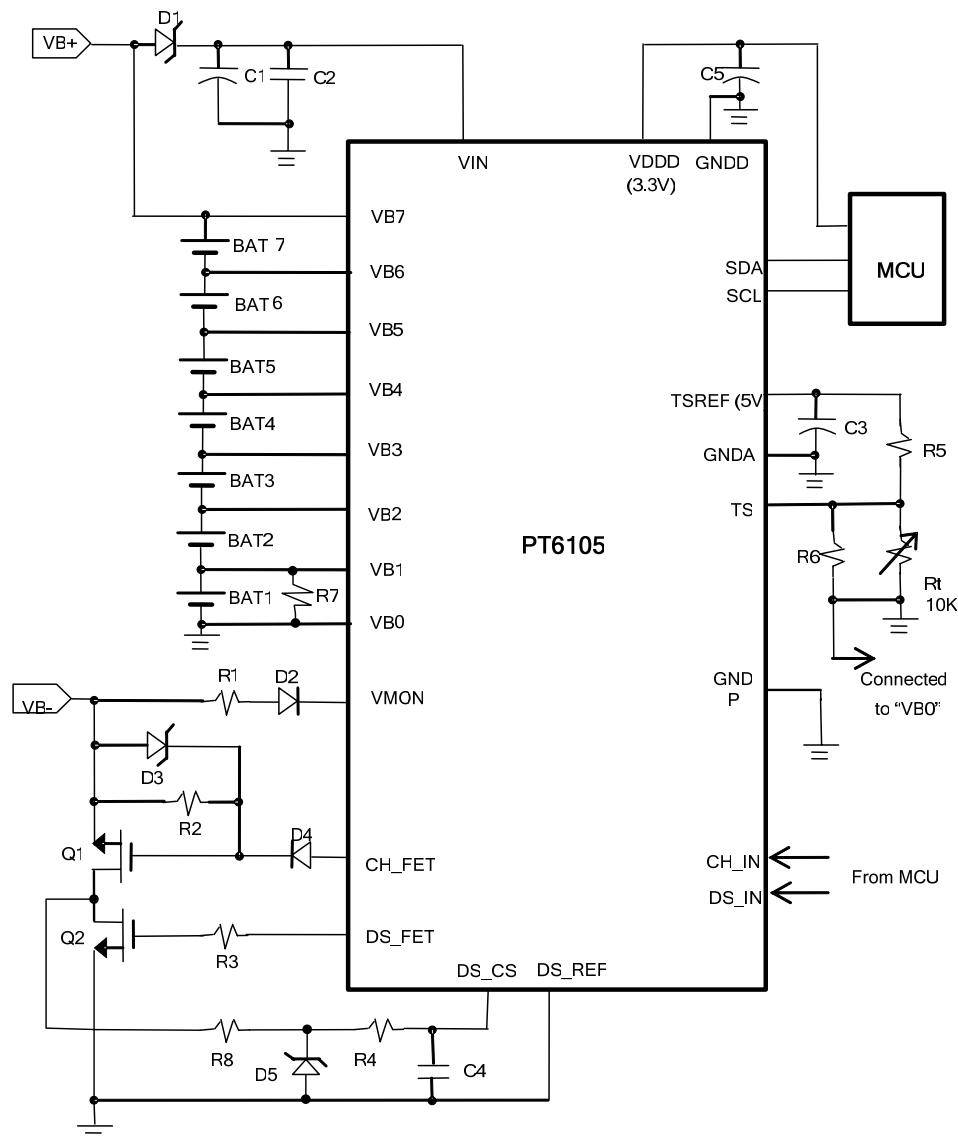


Figure 2. Typical application of PT6105 for 7 Li-ion battery cells

**ABSOLUTE MAXIMUM RATINGS**

| SYMBOL                               | ITEMS  | VALUE       | UNIT |
|--------------------------------------|--|-------------|------|
| V <sub>IN</sub>                      | Power Supply Voltage                         | -0.5V ~ 36  | V    |
| V <sub>Bi(i=1~n)</sub>               | V <sub>Bn</sub> - V <sub>B</sub> (n-1) n=1~7 | -0.5V to 6  | V    |
| V <sub>MON</sub> , CH_FET,<br>DS_FET | Terminal Voltage                             | -0.5V to 32 | V    |
| All other pins                       | Terminal Voltage                             | -0.5V to 5  | V    |

**RECOMMENDED OPERATING RANGE**

| SYMBOL                 | ITEMS  | VALUE     | UNIT |
|------------------------|--|-----------|------|
| V <sub>IN</sub>        | Power Supply Voltage                         | 6 ~30.1   | V    |
| V <sub>Bi(i=1~n)</sub> | V <sub>Bn</sub> - V <sub>B</sub> (n-1) n=1~7 | 2.0 ~ 4.3 | V    |
| V <sub>TS</sub>        |  | 0~2.5V    | V    |
| All other pins         | Terminal Voltage                             | < 5       | V    |
|                        | Cell Balance Current                         | <200      | mA   |
|                        | V <sub>DDD</sub> Output Current              | <.40      | mA   |
|                        | Temperature Range                            | -40 ~ +85 | °C   |

**ELECTRICAL CHARACTERISTICS**

 Table 2. V<sub>IN</sub> = 25V, T<sub>A</sub> = 25°C unless otherwise specified.

| SYMBOL              | ITEMS                            | CONDITIONS                              | Min. | Typ. | Max. | UNIT |
|---------------------|----------------------------------|---|------|------|------|------|
| V <sub>IN</sub>     | Input Voltage                    | whole function Guaranteed (Note1)       | 6    |      | 32   | V    |
|                     |                                  | For correct I2C operation (Note2)       | 5    |      | 32   | V    |
| I <sub>SLEEP</sub>  | Supply current in sleep mode     | WKUP bit = "0"                          |      | 8    | 12   | uA   |
| V <sub>UVLO</sub>   | Under-voltage lockout            | Vin falling                             | 5.4  |      | 6    | V    |
|                     | UVLO hysteresis                  | Vin rising                              |      | 0.1  |      |      |
| T <sub>UVLO</sub>   | Under voltage lock out delay     |   |      | 500  |      | uS   |
|                     | Chip Wake up Delay               | T = -40~85°C                            |      | 3    | 3.5  | ms   |
| T <sub>WCHDG</sub>  | Watch dog time-out               |   | 1.5  | 2    | 4    | s    |
| TSD                 | Internal Thermal Shut Down       |   |      | 150  |      | °C   |
| ΔTSD                | TSD Hysteresis                   |   |      | 20   |      |      |
| V <sub>VMON</sub>   | Overload Monitor input Threshold | Falling edge, LDMONEN bit = "1" (Note3) |      | 1.35 |      | V    |
| I <sub>VMON</sub>   | overLoad Monitor Current         |   |      | 20   |      | uA   |
| T <sub>LDFAIL</sub> | overload detection delay         |   |      | 0.5  | 1    | ms   |

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

| SYMBOL                          | ITEMS                             | CONDITIONS                  | Min.                  | Typ. | Max. | UNIT |
|---------------------------------|-----------------------------------|-----------------------------|-----------------------|------|------|------|
| <b>Charging/Discharging</b>     |                                   |                             |                       |      |      |      |
| V <sub>DSC</sub>                | Discharge Short Circuit Threshold | DSCV<2:0> = 000             |                       | 0.2  |      | V    |
|                                 |                                   | DSCV<2:0> = 001             |                       | 0.3  |      |      |
|                                 |                                   | DSCV<2:0> = 010             |                       | 0.4  |      |      |
|                                 |                                   | DSCV<2:0> = 011             |                       | 0.45 |      |      |
|                                 |                                   | DSCV<2:0> = 100             |                       | 0.55 |      |      |
|                                 |                                   | DSCV<2:0> = 101             |                       | 0.65 |      |      |
|                                 |                                   | DSCV<2:0> = 110             |                       | 0.75 |      |      |
|                                 |                                   | DSCV<2:0> = 111             |                       | 1.2  |      |      |
| T <sub>DSC</sub>                | Discharge Short Circuit delay     | DSCT<2:0> = 000             |                       | 60   |      | us   |
|                                 |                                   | DSCT<2:0> = 010             |                       | 120  |      |      |
|                                 |                                   | DSCT<2:0> = 010             |                       | 500  |      |      |
|                                 |                                   | DSCT<2:0> = 011             |                       | 1    |      | ms   |
|                                 |                                   | DSCT<2:0> = 100             |                       | 4    |      |      |
|                                 |                                   | DSCT<2:0> = 101             |                       | 8    |      |      |
|                                 |                                   | DSCT<2:0> = 110             |                       | 16   |      |      |
|                                 |                                   | DSCT<2:0> = 111             |                       | 32   |      |      |
| I <sub>BAL</sub>                | Charge Balance Current            | BC1 bit = "0" BC0 bit = "0" |                       | 25   |      | mA   |
|                                 |                                   | BC1 bit = "0" BC0 bit = "1" |                       | 50   |      |      |
|                                 |                                   | BC1 bit = "1" BC0 bit = "0" |                       | 100  |      |      |
|                                 |                                   | BC1 bit = "1" BC0 bit = "1" | 160                   | 200  | 240  |      |
| T <sub>R</sub>                  | DS_FET/CH_FET Rising Time         | Load=3.3nF                  |                       | 15   |      | us   |
| T <sub>F</sub>                  | DFET Falling Time                 | Load=3.3nF                  |                       | 15   |      |      |
| V <sub>h</sub>                  | DS_FET, CH_FET                    | V <sub>in</sub> > 15V       | 10                    | 12   | 15   | V    |
|                                 |                                   | 6V < V <sub>in</sub> < 15V  | V <sub>in</sub> -0.35 |      |      |      |
| V <sub>l</sub>                  |                                   |                             |                       | 0.1  |      |      |
| <b>Analog Regulator (TSREF)</b> |                                   |                             |                       |      |      |      |
| V <sub>TSREF</sub>              | Reference for temperature sensor  | T = -40~85°C                | 4.80                  | 5.0  | 5.20 | V    |
| I <sub>MAX</sub>                | Output Current                    |                             | 20                    |      |      | mA   |

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

| SYMBOL                                      | ITEMS  | CONDITIONS  | Min.                         | Typ. | Max. | UNIT |    |
|---|--|---|------------------------------|------|------|------|----|
| <b>5V Digital Regulator (VDDD)</b>          |  |   |                              |      |      |      |    |
| VDDD  | Output voltage                                 | T = -40~85°C  | VIN ≥ 7V                     | 4.8  | 5    | 5.2  | V  |
|   |  |   | 7 > VIN ≥ 5V                 | 3.2  |      |      |    |
| I <sub>vddd</sub>                           | Output Current                                 | Normal operation  | VIN ≥ 7V                     | 45   |      |      | mA |
|   |  |   | 7 > VIN ≥ 5V                 |      | 10   |      |    |
|   |  | Sleep mode  | 4                            |      |      | mA   |    |
| I <sub>sc</sub>                             | Short circuit current                          | VDDD=0  |                              | 10   |      | mA   |    |
| <b>ADC</b>                                  |  |   |                              |      |      |      |    |
|   | Conversion resolution                          |   |                              | 10   |      | Bits |    |
|   | Settling time                                  |   |                              | 2    |      | ms   |    |
| V <sub>ref</sub>                            | Reference voltage                              | T = -40~85°C  |                              | 2.5  |      | V    |    |
| ΔVB   | Battery voltage measurement Error              | VIN ≥ 7V<br>T = -40~85°C  | v <sub>bn</sub> =4.2V(n=1~7) |      | 25   | mV   |    |
|   |  |   | v <sub>bn</sub> =2V(n=1~7)   |      | 50   |      |    |
|   |  |   | v <sub>bn</sub> =4.5V(n=1~7) |      | 35   |      |    |
|   |  | VIN < 7V<br>T = -40~85°C  | v <sub>bn</sub> =3V(n=1~7)   |      | 75   |      |    |
|   |  | v <sub>bn</sub> =2V(n=1~7)  |                              | 100  |      |      |    |
| ΔV <sub>TS</sub>                            | Voltage error at TS pin                        | V <sub>IN</sub> > 6V, V <sub>TS</sub> = 2.5V                      |                              | 25   |      | mV   |    |
| G <sub>TEMP</sub>                           | External temperature Pre-amplifier Gain        | T = -40~85°C  |                              | 1    |      | V/V  |    |
| ΔV <sub>DS_CS</sub>                         | Voltage error at DS_CS pin                     | V <sub>DS_CS</sub> = 0.5V   |                              |      | 10   | %    |    |
| G <sub>IDS</sub>                            | Discharging Current Sensing Pre-amplifier gain | T = -40~85°C  |                              | 5    |      | V/V  |    |
| <b>Abnormal battery voltage measurement</b> |  |   |                              |      |      |      |    |
| V <sub>BREV</sub>                           | Reversed battery polarity                      | (Note 4)  |                              |      | 0.7  | V    |    |
| V <sub>BDC</sub>                            | Battery disconnected                           | The first battery needs an external resistor connecting to ground |                              |      | 0.7  | V    |    |
| <b>I<sup>2</sup>C Interface</b>             |  |   |                              |      |      |      |    |
| f <sub>CLK</sub>                            | SCL Clock Frequency                            |   |                              | 100  |      | KHz  |    |
| t <sub>HD:SDA</sub>                         | Input Data Setup Time                          |   | 1                            |      |      | us   |    |
| V <sub>IL</sub>                             | Digital Input Voltage Low                      |   |                              |      | 0.5  | V    |    |
| V <sub>IH</sub>                             | Digital Input Voltage High                     |   | 2.5                          |      |      |      |    |
| R <sub>P</sub>                              | SDA and SCL Internal Pull-up Resistor          |   |                              | 10   |      | k Ω  |    |

**Note1:** The ADC outputs correct code under such VIN input range;

**Note2:** I<sup>2</sup>C communication between chip and MCU is guaranteed under such VIN input voltage range;

**Note3:** Load monitor is only used to detect whether the load is removed, when light load or short-circuit is taking

place during discharge;

**Note4:** There will be a transient negative glitch voltage on a bad battery output terminal for heavy loading;

FUNCTIONAL BLOCK DIAGRAM

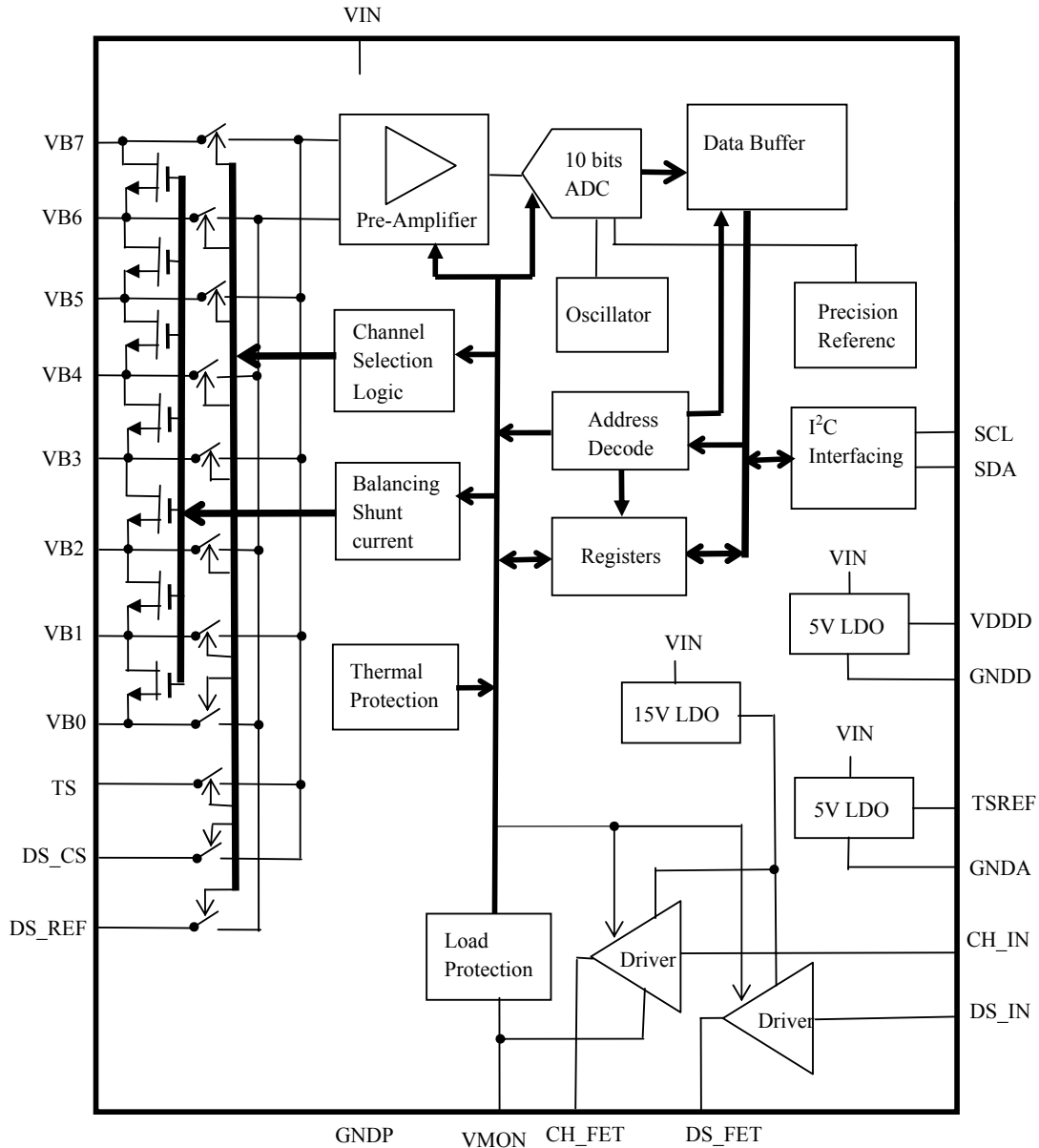


Figure 3. Simplified functional block diagram of PT6105

### REGISTERS

Table 1. Registers

| ADDR | REGISTER                 | READ/WRITE | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|------|--------------------------|------------|----------|----------|----------|----------|----------|----------|----------|----------|
| 00H  | Configuration and Status | READ/WRITE | Reserved | Reserved | WKUP     | CHSET    | DSSET    | CELLN2   | CELLN1   | CELLN0   |
| 01H  | Operating Status         | READ       | Reserved | Reserved | Reserved | UVLO     | ADCFAIL  | LDFAIL   | TSD      | DSC      |
| 02H  | Cell Balance             | READ/WRITE | CB7ON    | CB6ON    | CB5ON    | CB4ON    | CB3ON    | CB2ON    | CB1ON    | Reserved |
| 03H  | DSC Set                  | READ/WRITE | DSCV2    | DSCV1    | DSCV0    | DSCT2    | DSCT1    | DSCT0    | DSCEN    | LDMONEN  |
| 04H  | Balance Current Set      | READ/WRITE | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | BC1      | BC0      |
| 05H  | ADC Data                 | READ       | C1VD[7]  | C1VD[6]  | C1VD[5]  | C1VD[4]  | C1VD[3]  | C1VD[2]  | C1VD[1]  | C1VD[0]  |
| 06H  |                          |            | 0        | 0        | 0        | 0        | 0        | 0        | C1VD[9]  | C1VD[8]  |
| 07H  |                          |            | C2VD[7]  | C2VD[6]  | C2VD[5]  | C2VD[4]  | C2VD[3]  | C2VD[2]  | C2VD[1]  | C2VD[0]  |
| 08H  |                          |            | 0        | 0        | 0        | 0        | 0        | 0        | C2VD[9]  | C2VD[8]  |
| 09H  |                          |            | C3VD[7]  | C3VD[6]  | C3VD[5]  | C3VD[4]  | C3VD[3]  | C3VD[2]  | C3VD[1]  | C3VD[0]  |
| 0AH  |                          |            | 0        | 0        | 0        | 0        | 0        | 0        | C3VD[9]  | C3VD[8]  |
| 0BH  |                          |            | C4VD[7]  | C4VD[6]  | C4VD[5]  | C4VD[4]  | C4VD[3]  | C4VD[2]  | C4VD[1]  | C4VD[0]  |
| 0CH  |                          |            | 0        | 0        | 0        | 0        | 0        | 0        | C4VD[9]  | C4VD[8]  |
| 0DH  |                          |            | C5VD[7]  | C5VD[6]  | C5VD[5]  | C5VD[4]  | C5VD[3]  | C5VD[2]  | C5VD[1]  | C5VD[0]  |
| 0EH  |                          |            | 0        | 0        | 0        | 0        | 0        | 0        | C5VD[9]  | C5VD[8]  |
| 0FH  |                          |            | C6VD[7]  | C6VD[6]  | C6VD[5]  | C6VD[4]  | C6VD[3]  | C6VD[2]  | C6VD[1]  | C6VD[0]  |
| 10H  |                          |            | 0        | 0        | 0        | 0        | 0        | 0        | C6VD[9]  | C6VD[8]  |
| 11H  |                          |            | C7VD[7]  | C7VD[6]  | C7VD[5]  | C7VD[4]  | C7VD[3]  | C7VD[2]  | C7VD[1]  | C7VD[0]  |
| 12H  |                          |            | 0        | 0        | 0        | 0        | 0        | 0        | C7VD[9]  | C7VD[8]  |
| 13H  | DSCD[7]                  | DSCD[6]    | DSCD[5]  | DSCD[4]  | DSCD[3]  | DSCD[2]  | DSCD[1]  | DSCD[0]  |          |          |
| 14H  | 0                        | 0          | 0        | 0        | 0        | 0        | DSCD[9]  | DSCD[8]  |          |          |
| 15H  | ETMP[7]                  | ETMP[6]    | ETMP[5]  | ETMP[4]  | ETMP[3]  | ETMP[2]  | ETMP[1]  | ETMP[0]  |          |          |
| 16H  | 0                        | 0          | 0        | 0        | 0        | 0        | ETMP[9]  | ETMP[8]  |          |          |
| 17H  | Registers Writer Enable  | READ/WRITE | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | WR EN    |

1. A "1" written to a configuration bit causes the action to be taken. A "1" read from a status bit indicates that the condition exists.

Table 2. Configuration Register (ADDR:00H)

| ADDR  | REGISTER                 | READ/WRITE | 7        | 6        | 5    | 4     | 3     | 2      | 1      | 0      |
|---|--------------------------|------------|----------|----------|------|-------|-------|--------|--------|--------|
| 00H   | Configuration and Status | READ/WRITE | Reserved | Reserved | WKUP | CHSET | DSSET | CELLN2 | CELLN1 | CELLN0 |
| BIT 7,6: Reserved for future expansion.   |                          |            |          |          |      |       |       |        |        |        |
| BIT 5: This bit control the chip operates in sleep mode or wake up mode.<br>0 = Sleep mode; (Default)<br>1 = Wake up mode.  |                          |            |          |          |      |       |       |        |        |        |
| BIT 4: This bit prevents or allows write the charge set registers(02H,04H).<br>0 = Prevent;(Default)<br>1 = Allow.  |                          |            |          |          |      |       |       |        |        |        |
| BIT 3: This bit prevents or allows write the discharge set registers(03H).<br>0 = Prevent;(Default)<br>1 = Allow.   |                          |            |          |          |      |       |       |        |        |        |
| BITS 2,1,0: The two bits decide the number of cells in 7 cells mode.<br>000`011 = 3 cells;(Default)<br>1 0 0 = 4 cells;<br>1 0 1 = 5 cells;<br>1 1 0 = 6 cells;<br>1 1 1 = 7 cells. |                          |            |          |          |      |       |       |        |        |        |



Table 3. Operating Status Register (ADDR:01H)

| ADDR  | REGISTER         | READ/WRITE | 7        | 6        | 5        | 4    | 3       | 2      | 1   | 0   |
|---|------------------|------------|----------|----------|----------|------|---------|--------|-----|-----|
| 01H   | Operating Status | READ       | Reserved | Reserved | Reserved | UVLO | ADCFAIL | LDFAIL | TSD | DSC |
| BIT 7,6,5: Reserved for future expansion.   |                  |            |          |          |          |      |         |        |     |     |
| BIT 4: This bit indicates an VIN under voltage condition.<br>0 = VIN is greater than the UVLO threshold; (Default)<br>1 = VIN is below the UVLO threshold.<br>This bit is reset if the UVLO condition is cleared.   |                  |            |          |          |          |      |         |        |     |     |
| BIT 3: This bit indicates an ADC fail condition.<br>0 = ADC works well; (Default)<br>1 = ADC fail.<br>This bit is reset if ADC fail condition is cleared or this bit is read.   |                  |            |          |          |          |      |         |        |     |     |
| BIT 2: This bit indicates a load fail condition.<br>0 = Load is disconnected under discharge short circuit condition; (Default)<br>1 = Load is still connected under discharge short circuit condition.<br>This bit is reset if the load fail condition is cleared or this bit is read. |                  |            |          |          |          |      |         |        |     |     |
| BIT 1: This bit indicates an chip thermal shut down condition.<br>0 = Chip temperture is less than the thermal shut down threshold; (Default)<br>1 = Chip temperture is greater than or equal to the thermal shut down threshold.<br>This bit is reset if the TSD condition is cleared. |                  |            |          |          |          |      |         |        |     |     |
| BIT 0: This bit indicates a discharge short circuit condition.<br>0 = Discharge current is less than the short circuit threshold; (Default)<br>1 = Discharge current is greater than or equal to the short circuit threshold.<br>This bit is reset after this bit is read.              |                  |            |          |          |          |      |         |        |     |     |

**Note:** Neither the PT6105 nor MCU can write to the status register. It can only be set by abnormal operating conditions, and, of course, can be automatically reset when the abnormal conditions doesn't exist (One except is WDOG which is only reset by MUC).

Table 4. Cell Balancing Control Register (ADDR:02H)

| ADDR   | REGISTER     | READ/WRITE | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0        |
|--|--------------|------------|-------|-------|-------|-------|-------|-------|-------|----------|
| 02H  | Cell Balance | READ/WRITE | CB7ON | CB6ON | CB5ON | CB4ON | CB3ON | CB2ON | CB1ON | Reserved |
| BIT 7,6,5,4,3,2,1: The bits control the cell balance on or off.<br>0 = Off; (Default)<br>1 = On. |              |            |       |       |       |       |       |       |       |          |
| BIT 0: Reserved for future expansion.  |              |            |       |       |       |       |       |       |       |          |

**Note:** The Cell Balancing Control Register is blocked during discharge.

**Table 5. Discharge Short Circuit Register (ADDR:03H)**

| ADDR   | REGISTER | READ/WRITE | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0       |
|--|----------|------------|-------|-------|-------|-------|-------|-------|-------|---------|
| 03H  | DSC Set  | READ/WRITE | DSCV2 | DSCV1 | DSCV0 | DSCT2 | DSCT1 | DSCT0 | DSCEN | LDMONEN |
| BIT 7,6,5: The three bits define the discharge short circuit threshold voltage.<br>0 0 0 = 0.20V; (Default)<br>0 0 1 = 0.30V;<br>0 1 0 = 0.40V;<br>0 1 1 = 0.45V;<br>1 0 0 = 0.55V;<br>1 0 1 = 0.65V;<br>1 1 0 = 0.75V;<br>1 1 1 = 1.2V. |          |            |       |       |       |       |       |       |       |         |
| BIT 4,3,2: The two bits defines the discharge short circuit time out.<br>0 0 0 = 64us; (Default)<br>0 0 1 = 128us;<br>0 1 0 = 512us;<br>0 1 1 = 1ms;<br>1 0 0 = 4ms;<br>1 0 1 = 8ms;<br>1 1 0 = 16ms;<br>1 1 1 = 32ms.                   |          |            |       |       |       |       |       |       |       |         |
| BIT 1: This bit enables or disables the short circuit protection in discharging mode.<br>0 = Disable; (Default)<br>1 = Enable.   |          |            |       |       |       |       |       |       |       |         |
| BIT 0: This bit enables or disables the loadmonitor function in discharging mode.<br>0 = Disable; (Default)<br>1 = Enable.   |          |            |       |       |       |       |       |       |       |         |

**Table 6. Cell Balance set register**

| 04H   | Balance Current Set | READ/WRITE | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | BC1 | BC0 |
|---|---------------------|------------|----------|----------|----------|----------|----------|----------|----------|-----|-----|
| BIT 7,2: Reserved for future expansion.   |                     |            |          |          |          |          |          |          |          |     |     |
| BIT 1,0: The two bits defines the cells balance current threshold.<br>0 0 = 50mA; (Default)<br>0 1 = 100mA;<br>1 0 = 150mA;<br>1 1 = 200mA. |                     |            |          |          |          |          |          |          |          |     |     |

To avoid the PT6105 from over heating, please don't select the 200mA shut current if more than one battery needs balancing operation. If there are more than one "1" bits, then shut current value is the addition of them.

**Table 7. ADC data output registers**

| ADDR | REGISTER | READ/WRITE | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
|------|----------|------------|---------|---------|---------|---------|---------|---------|---------|---------|
| 05H  | ADC Data | READ       | C1VD[7] | C1VD[6] | C1VD[5] | C1VD[4] | C1VD[3] | C1VD[2] | C1VD[1] | C1VD[0] |
| 06H  |          |            | 0       | 0       | 0       | 0       | 0       | 0       | C1VD[9] | C1VD[8] |
| 07H  |          |            | C2VD[7] | C2VD[6] | C2VD[5] | C2VD[4] | C2VD[3] | C2VD[2] | C2VD[1] | C2VD[0] |
| 08H  |          |            | 0       | 0       | 0       | 0       | 0       | 0       | C2VD[9] | C2VD[8] |
| 09H  |          |            | C3VD[7] | C3VD[6] | C3VD[5] | C3VD[4] | C3VD[3] | C3VD[2] | C3VD[1] | C3VD[0] |
| 0AH  |          |            | 0       | 0       | 0       | 0       | 0       | 0       | C3VD[9] | C3VD[8] |
| 0BH  |          |            | C4VD[7] | C4VD[6] | C4VD[5] | C4VD[4] | C4VD[3] | C4VD[2] | C4VD[1] | C4VD[0] |
| 0CH  |          |            | 0       | 0       | 0       | 0       | 0       | 0       | C4VD[9] | C4VD[8] |
| 0DH  |          |            | C5VD[7] | C5VD[6] | C5VD[5] | C5VD[4] | C5VD[3] | C5VD[2] | C5VD[1] | C5VD[0] |
| 0EH  |          |            | 0       | 0       | 0       | 0       | 0       | 0       | C5VD[9] | C5VD[8] |
| 0FH  |          |            | C6VD[7] | C6VD[6] | C6VD[5] | C6VD[4] | C6VD[3] | C6VD[2] | C6VD[1] | C6VD[0] |
| 10H  |          |            | 0       | 0       | 0       | 0       | 0       | 0       | C6VD[9] | C6VD[8] |
| 11H  |          |            | C7VD[7] | C7VD[6] | C7VD[5] | C7VD[4] | C7VD[3] | C7VD[2] | C7VD[1] | C7VD[0] |
| 12H  |          |            | 0       | 0       | 0       | 0       | 0       | 0       | C7VD[9] | C7VD[8] |
| 13H  |          |            | DSCD[7] | DSCD[6] | DSCD[5] | DSCD[4] | DSCD[3] | DSCD[2] | DSCD[1] | DSCD[0] |
| 14H  |          |            | 0       | 0       | 0       | 0       | 0       | 0       | DSCD[9] | DSCD[8] |
| 15H  | ETMP[7]  | ETMP[6]    | ETMP[5] | ETMP[4] | ETMP[3] | ETMP[2] | ETMP[1] | ETMP[0] |         |         |
| 16H  | 0        | 0          | 0       | 0       | 0       | 0       | ETMP[9] | ETMP[8] |         |         |

Table8 registers write enable

| ADDR | REGISTER  | READ/WRITE | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0     |
|------|-----------|------------|----------|----------|----------|----------|----------|----------|----------|-------|
| 17H  | Test Mode | READ/WRITE | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | WR EN |

WR EN:

0 = Data can't be written into the write/read registers if the bit is "0".  
 1 = Data is written into the write/read registers after the bit is set to "1", this bit is auto reset after being set.

## DETAILED DESCRIPTION

### Charging Management

#### *Battery Balancing*

The charging voltage balancing only applies during the charging period. If an unbalanced over-charged battery voltage is detected by ADC, the shunt transistor connected across a battery will be turned on by a command from MCU to lower the battery voltage, Both the shunt current value and on/off of each shunt transistor are programmable via MCU. The shunt current for each battery can be programmable as 200mA, 100mA, 50mA, and 25mA. When more than one battery are detected as over-charged, please carefully the total shunt current to avoid the PT6105 being over heated.

#### *Safety protections*

Over-voltage protections for individual battery cells during charging is realized by

- sampling all 7 battery voltages into MCU through the I2C interface,
- comparing digitized voltages with programmed safety thresholds, and
- sending control signal to turn off MOSFETs after a programmed delay, if the voltage is over threshold.

A precision reference voltage source and a 10-bit ADC guarantee that error is less than  $\pm 25\text{mV}$  for 4.2V battery voltage detection, over the temperature range from  $-40\text{oC}$  to  $85\text{oC}$ .

### Discharging Management

#### *Safety protections*

The same as in the charging protection, individual battery voltage are digitized alternatively, transferred to MCU via I2C interface, and compared with programmed safety thresholds. If any cell voltage is bellow under-voltage protection threshold, Control signal is sent out and MOSFETs are turned off after a

certain delay time. The under-voltage protection function works together with the over-current protection to prevent batteries from over discharge.

The MOSFET's discharge current is sampled with the vds of discharge NMOSFET, Similar to the battery under-voltage protection, the over-current protection is performed by comparing the sampled and digitized data with a programmable threshold inside the MCU, and turn off MOSFETs .

#### *Driving the Motor*

The discharging wave form could be DC voltage or  $<20\text{k Hz}$  PWM pulses. The rising and falling times of gate driving voltages are limited by maxim driving currents from CH\_FET and DS\_FET pins. An external current limiting resistor R3 in Fig.2 could limit the gate driving speed further during discharging.

### Over Temperature Management

The battery pack temperature is sensed with a thermal resistor,  $R_t$ , in Fig. 2, plus two normal resistors linearizing the sensed voltage. The gain of the preamplifier for sensing external temperature is set at 1. The detected environmental temperature value is converted to digital data and collected by MCU. Within MCU, the data is compared to safety temperature limits on battery charging and discharging.

The PT6105 has an internal over temperature shutdown function if the chip's junction temperature is over  $140\text{oC}$ . If the chip enters over temperature protection mode, all functional blocks and external MOSFETs will be shutdown except the 5V LDO supplying MCU, I2C interface, and register blocks. There is a flag bit in the status register is set to "1". After the internal temperature cools down about  $20\text{ oC}$  bellow the shutdown threshold, the status register is reset. The MCU could not set or reset this flag bit

**Multi-cell Battery Management  
Front End with I<sup>2</sup>C Interface**

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**Watchdog for MCU**

The PT6105 monitors the communication function between the I<sup>2</sup>C interface and MCU. If there is no activity observed from the MCU for about 2sec. two external MOSFETs are turned off by MCU.

**Discharge Short Circuit Protection**

When PT6105 detects a discharge short circuit condition, both power MOSFETs are turned off and the DSC bit is set “1”. The DSC bit is reset after this bit is read by MCU. MCU can turn on the MOSFETs at any time but should turn on the load monitor function to detect that the short circuit condition has been removed.

**Load Monitor on Short Circuit**

The load monitoring and protection function is primarily used to guarantee that the load (mostly the motor) has been removed following an over-current or short circuit protection during discharge. This function will prevent the MOSFET from turning on while the short circuit is still present. As the benefit, the battery is avoided from starting discharge to a short circuit load. The load protection mechanism could be enabled or disabled by the MCU by setting LDMONEN bit as “1” or “0” in the configuration register. The discharge MOSFET will be switched off if short circuit load is detected during discharge, the LDFAIL bit in the status register will be set to “1” if the short circuit load is still connected under short circuit condition. When MCU detected this bit is “1”, both MOSFETs will be turned off and discharging procedure is terminated. This bit is self-reset after the short circuit condition is removed.

**Other Protections**

- The PT6105 could sustain a <1ms negative down-to-ground glitch from the battery pack at the start of discharge.
- VIN =5.7V triggers under-voltage lockout (UVLO). The UVLO bit in the status register is set as “1”, and MOSFETs are turned off. All analog functions in the PT6105 are also turned off. The UVLO bit will be reset if VIN rises above the UVLO threshold with a hysteresis.
- Power on reset function (POR = 1.5~2.0). Right after power on and then VIN above POR, all digital registers are guaranteed to be reset at the default sleep mode, waiting for the wake up signal from the MCU.

**ADC**

The ADC has 10-bit accuracy, sampling 7 battery voltages and environment temperature alternatively. The setting time of each channel is less than 7ms. All the sampled data is buffered in 9 data buffers and waits for being collected by MCU via I<sup>2</sup>C interface. If one data conversion encounters data overflow or saturation, the ADFAIL bit in the status register is set to “1”. The ADC could be powered down on three conditions: the sleep mode, internal over temperature protection, and UVLO=“1”. Each data buffer has a location address.

**LDOs**

There are two 5V LDO’s in the PT6105. One provides the supply voltage to external MCU and internal digital blocks. The other one provides the supply voltage to internal analog blocks, and is also used as a bias on the external thermal resistor.

Under no circumstance the digital LDO can be shutdown.

**I<sup>2</sup>C interface**

The I<sup>2</sup>C interface in the PT6105 works in the slave mode with the clock frequency of 100 kHz. The interfacing block can not be turned off under any condition.

**Sleep Mode and Wake up**

The MCU fully controls the PT6105’s entering and out from sleep mode by reset and set the WKUP bit in the configuration register. Right after power up, the PT6105 is set initially at sleep mode. If VIN rises above UVLO threshold and the WAKE bit set as “1”, the chip is allowed to wake up and start to work following commands from the MCU, after a short time delay.

At the sleep mode, digital LDO, I<sup>2</sup>C interface, and all register could not be powered down.

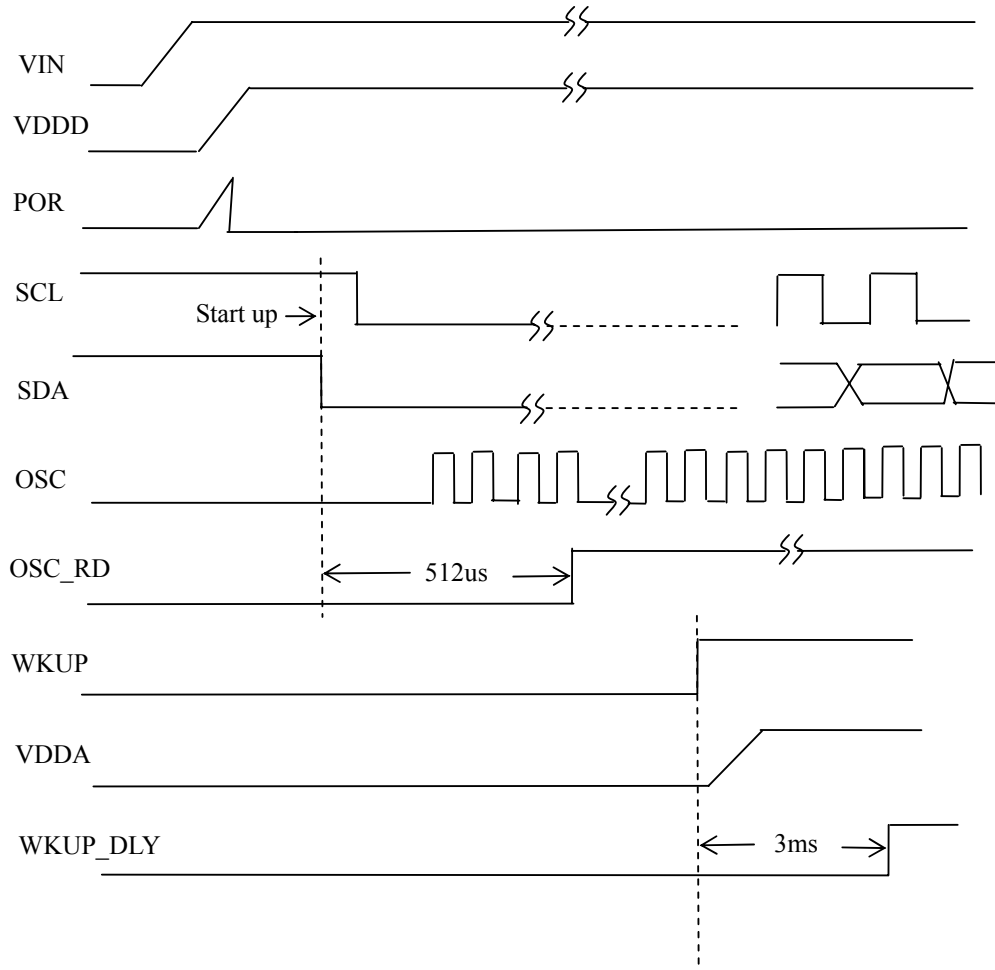
**MOSFET driver control**

Even though the PT6105 can not directly control the turning on/off of two external MOSFETs, it has the ability to power on/off the two MOSFET drivers. Two drivers will be power down at the following conditions, and will be powered on after these conditions disappear.

- Sleep mode
- Internal over temperature protection
- Load protection at short circuit condition
- MCU watchdog bit is set to “1”, i.e. there has been no activity from the MCU for 2s.

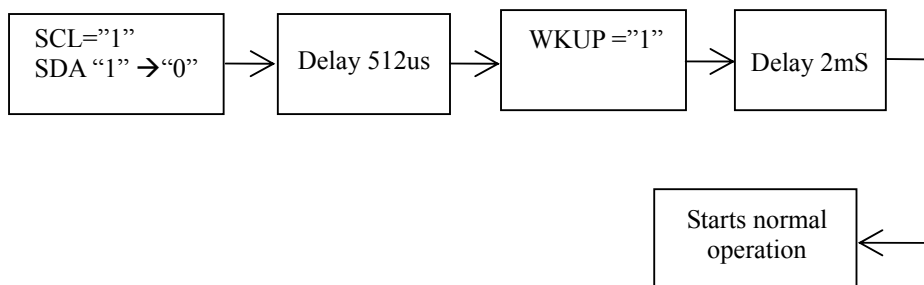
### TIMING DIAGRAMS

#### Power-on Sequences

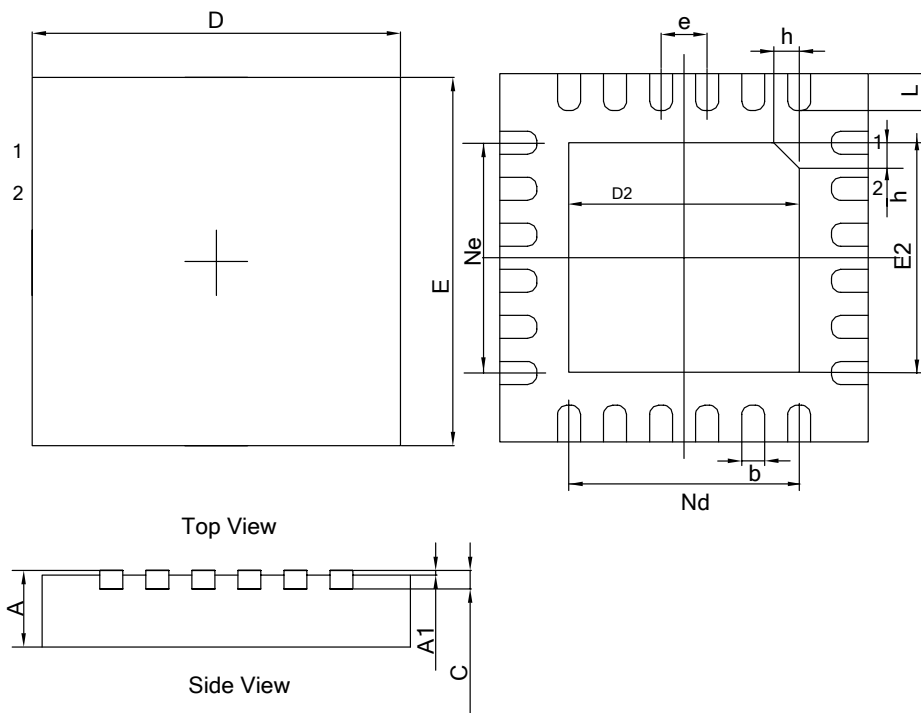


**Figure 4. Power on timing sequence**

#### Wake-up from Sleep Mode Flow Chart



### PACKAGE INFORMATION



| SYMBOL   | MILLIMETER |      |      |
|----------|------------|------|------|
|          | MIN        | NOM  | MAX  |
| A        | 0.70       | 0.75 | 0.80 |
| A1       | -          | 0.01 | 0.05 |
| b        | 0.18       | 0.25 | 0.30 |
| c        | 0.18       | 0.20 | 0.25 |
| D        | 3.90       | 4.00 | 4.10 |
| D2       | 2.50REF    |      |      |
| e        | 0.50BSC    |      |      |
| Ne       | 2.50BSC    |      |      |
| Nd       | 2.50BSC    |      |      |
| E        | 3.90       | 4.00 | 4.10 |
| E2       | 2.50REF    |      |      |
| L        | 0.35       | 0.40 | 0.45 |
| h        | 0.30       | 0.35 | 0.40 |
| L/F 载体尺寸 | 110×110    |      |      |