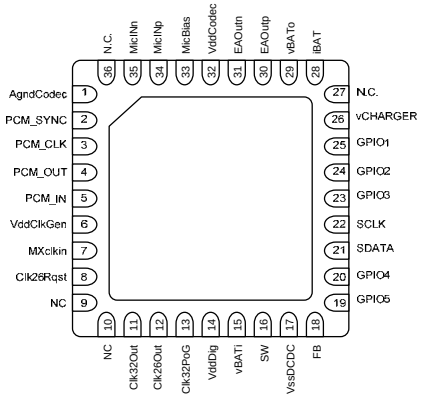
Headset Voice and Power Solution

IA3513

PIN ASSIGNMENT



36-pin QFN

DESCRIPTION

This IC is a complete Voice/Power solution for wireless headsets. A PCM Codec is included to perform the transmit encoding analog to digital (A/D) and the receive decoding digital to analog (D/A). Filtering and gain conditioning suitable for voice band communication systems are also built into the Codec.

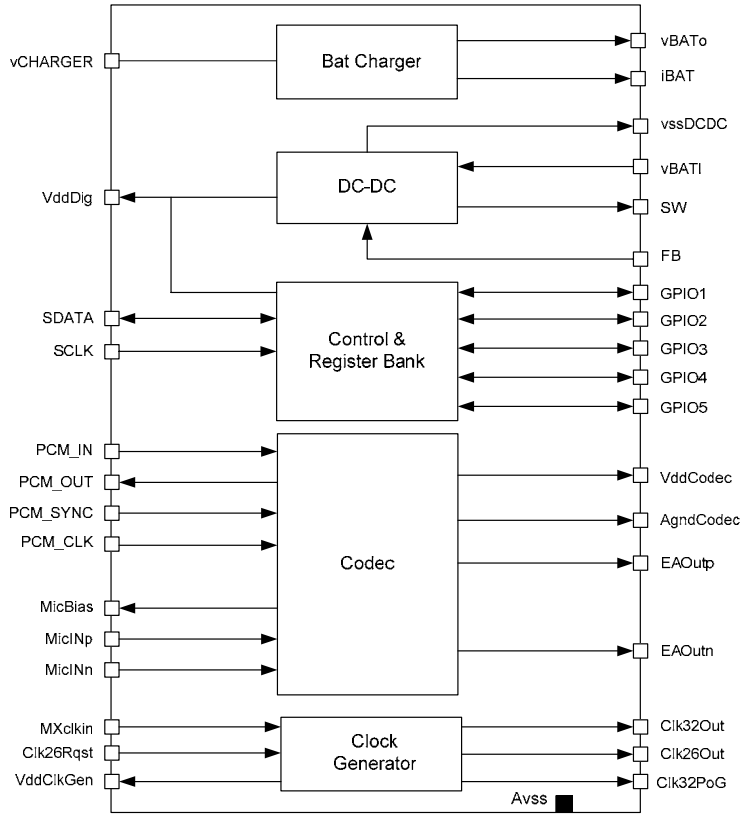
The Power management features of this IC include a Li-Ion/Li-Pol Battery charger that operates from either a power adaptor or from USB power and an internal DC-DC converter which powers the complete chipset of the headset.

For increased flexibility, programmable GPIOs are also included that can be configured for a variety of functions such as external power or charge phase signaling by driving LEDs, press button reading, and vibration motor driver. A power good (PG) output pin is also available.

To protect valuable PCB "real-estate" in the target application, the IC has a small pin count because of the programmable I2C interface, rather than dedicated control pins.

The IA3513 also includes a Clock Generation Block for increased flexibility; it generates both 26MHz and 32kHz output clocks.

BLOCK DIAGRAM



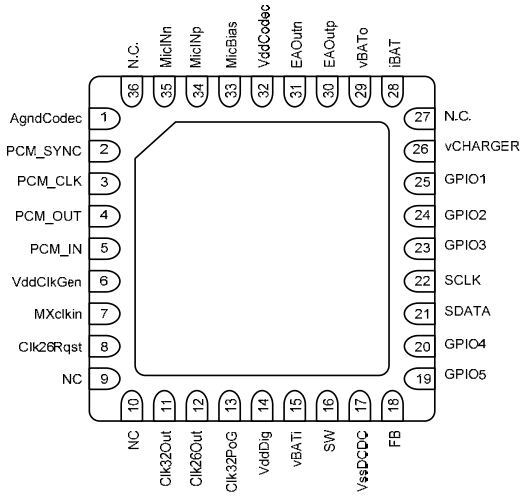
FEATURES

- PCM Codec
- Li-Ion/Li-Pol battery charger
- 5 GPIOs
- POR
- DC-DC Buck Converter
- 26MHz and 32kHz Clock Generation

TYPICAL APPLICATION

- Bluetooth headset

PACKAGE PIN DEFINITIONS



Pin Number	Name	Direction	Type[1]	Function
0 (back paddle)	Avss	I/O	Pwr	Negative Power Supply (Package exposed ground paddle)
1	AgndCodec	I/O	A	Codec Analog ground (VddCodec/2)
2	PCM_SYNC	I	D	PCM frame sync
3	PCM_CLK	I	D	PCM clock
4	PCM_OUT	O	D	PCM interface Transmit (AD) output
5	PCM_IN	I	D	PCM interface Receive (DA) input
6	VddClkGen	I/O	A	Clock Generator Positive Power Supply for decoupling
7	MXclkin	I	A	26MHz Crystal Oscillator input pin
8	Clk26Rqst	I	D	On signal for 26Mhz Crystal Oscilator
9	N.C.			Not Connected
10	N.C.			Not Connected
11	Clk32Out	O	D	32kHz Clock Output
12	Clk26Out	O	D	26MHz Clock Output
13	Clk32PoG	O	D	DC-DC Power Good and Clk32 OK flag
14	VddDig	I/O	Pwr	Digital Positive Power Supply for decoupling (internally Generated)
15	vBATi	I/O	Pwr	DCDC Converter Input voltage from Battery
16	SW	O	A	DCDC Converter Output Current to inductor
17	VssDCDC	I/O	Pwr	DCDC Converter Negative Power Supply
18	FB	I	A	DCDC Converter Feed Back voltage from smoothed output
19	GPIO5	I/O	D	General Purpose Input/Output 5
20	GPIO4	I/O	D	General Purpose Input/Output 4
21	SDATA	I/O	D	I2C data port
22	SCLK	I	D	I2C clock port
23	GPIO3	I/O	D	General Purpose Input/Output 3
24	GPIO2	I/O	D	General Purpose Input/Output 2
25	GPIO1	I/O	D	General Purpose Input/Output 1
26	vCHARGER	I/O	Pwr	Battery Charger Input voltage
27	N.C.			Not Connected
28	iBAT	I	A	Battery Charger Charge Current set point
29	vBATo	O	Pwr	Battery Charger output
30	EAOutp	O	A	Codec Earphone Amplifier Positive Output
31	EAOutn	O	A	Codec Earphone Amplifier Negative Output
32	VddCodec	I/O	Pwr	Codec Positive Power Supply for decoupling (internally Generated)
33	MicBias	O	A	Codec Microphone Bias Voltage
34	MicINp	I	A	Codec Microphone Amplifier Positive Input
35	MicINn	I	A	Codec Microphone Amplifier Negative Input
36	N.C.			Not Connected

[1] A=Analog, D=Digital, Pwr=Power

MAXIMUM RATINGS

Characteristics	Symbol	Value	Units
Charger voltage pins		Avss-0.3 to 17	V
Battery Voltage pins	Vbat	Avss-0.3 to 5	V
Earphone amplifier outputs pins		Avss-0.3 to Vbat + 0.3 < 5	V
GPIO pins		Avss-0.3 to Vbat + 0.3 < 5	V
DC-DC output		Avss-0.3 to Vbat + 0.3 < 5	V
Digital pins		Avss-0.3 to (Vbat + 0.3)< 3.6	V
Analog Pins		Avss-0.3 to (Vbat + 0.3)< 3.6	V
Operating Temperature	TA	-20 to 85	ºC
Storage Temperature		-55 to 125	ºC

PCM CODEC

Description

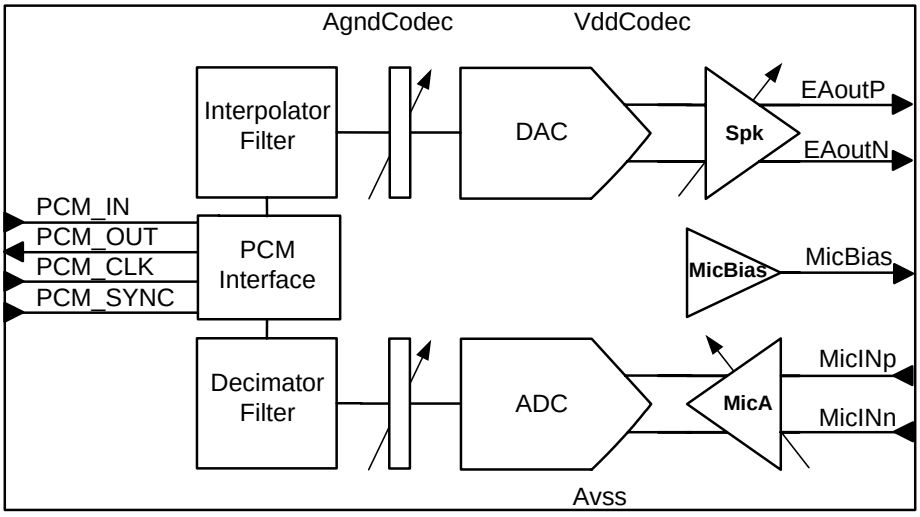
The PCM Codec comprises complete AD and DA channels, including direct interface to the microphone and earphone. The Codec SNR specification is adjusted to accommodate the Dynamic Range of companded signals used in the target application, guaranteeing at the same time a comfortable level of idle channel noise.

Both Receive and Transmit channels feature filtering functions and programmable gain. The transmit channel includes an anti-aliasing filter function in the microphone amplifier to eliminate high frequency signal components that would affect the AD conversion by being aliased to the voice band.

In the Receive channel, a smoothing filter is included to reduce the out-of band power present at the earphone Amplifier (EA) output.

The Codec includes sidetone processing, to release the host controller from external signal processing and microphone bias voltage generation. The gain in both channels is controlled using two segments for flexibility, a coarse gain implemented in the analog block (EA and MicA) and a fine gain implemented in the digital block to allow precise tuning of amplitudes.

Detailed Functional Diagram



For detailed codec specifications, including supporting curves, see this document, appendix A.

BATTERY CHARGER

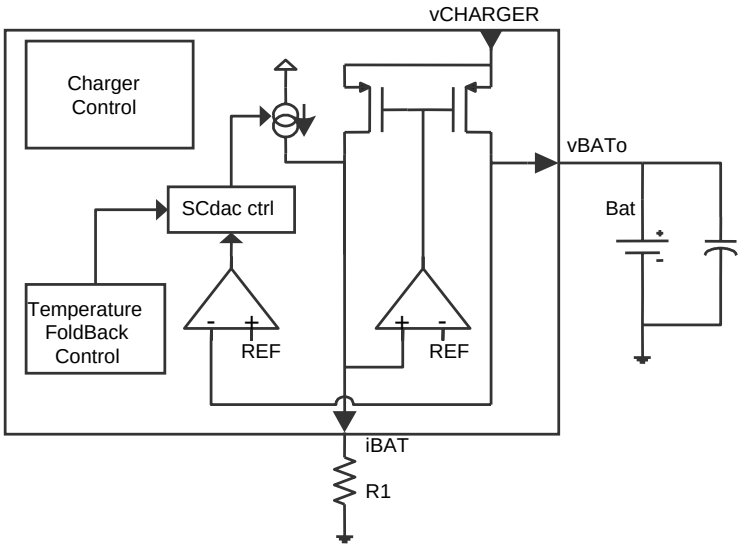
Description

The high-accuracy battery charger supports Li-Ion or Li-Pol batteries. No external FETs, current sensing resistor, or reverse-blocking diode are required. The circuit permits pre-charge for deeply discharged batteries, constant current charging followed by constant voltage and charge termination by minimum current.

Protection schemes include maximum and minimum voltage, as well as time-out termination for added safety. IC temperature is also monitored, allowing temperature fold-back and shutdown. The charger automatically starts charging cycles when the AC adaptor or USB are plugged-in, and shuts down when removed.

Battery status monitor is included. Charge status is available through register read.

Functional Block Diagram



Electrical Characteristics

TA=0° to 85°

General	Min	Typ	Max	Units
vCHARGER Supply Voltage	Vbat +100mV		12 (functional@17)	V
Maximum Charge Current C		90	150	mA
Charge Current definition[2]		IC= 119.3/R1		A
Charge Voltage (VbatSet)	4.158	4.2	4.242	V
Voltage Droupout from vCHARGER (Iout=90mA)	100			mV
VbatShort (below this value battery is shorted)		0.4		V
VbatOpen (above this value battery is open)		4.3		
VbatLowest (below this value is deeply discharged)		3		V
Vrestart (value for charge restart after charge complete)		4.0		V
Ipre (precharge current for deeply discharged cells)		1/10 C		
Ifinal (current value for constant voltage termination)		1/10 C		
PM timer (precharge safety timer)		1800		s
CC timer (constant current safety timer)		7200		s
CV timer (constant voltage safety timer)		18000		s
Safety Mode Timer		1800		s
FoldBack Mode timer (FB timer)		5		s
IC temperature to enter CC fold-back mode (FBTemp)			100	ºC
IC temperature foldback hysteresis (FBHys)		5		ºC
vCHARGER pin decoupling capacitor		10		uF

Temperature , vCHARGER and Maximum charge current

The circuit includes a foldback mode to protect against thermal failure, this way no worst case power dissipation scenarios need to be considered since the circuit reduces the charge current to maintain the die temperature below approximately 100 ºC.

As the charger is dominant in terms of power dissipation in the circuit, the temperature for which the charge current begins to be reduced can be, approximately calculated as follows:

$$TA < 100° - (vCHARGER - 3) \times IC \times \theta_{JA}$$

$\theta_{JA} = \theta_{JB} + \theta_{JBA}$

θ_{JA} = Junction to ambient thermal resistance

θ_{JB} = Junction to board thermal resistance

θ_{JBA} = Board to ambient thermal resistance

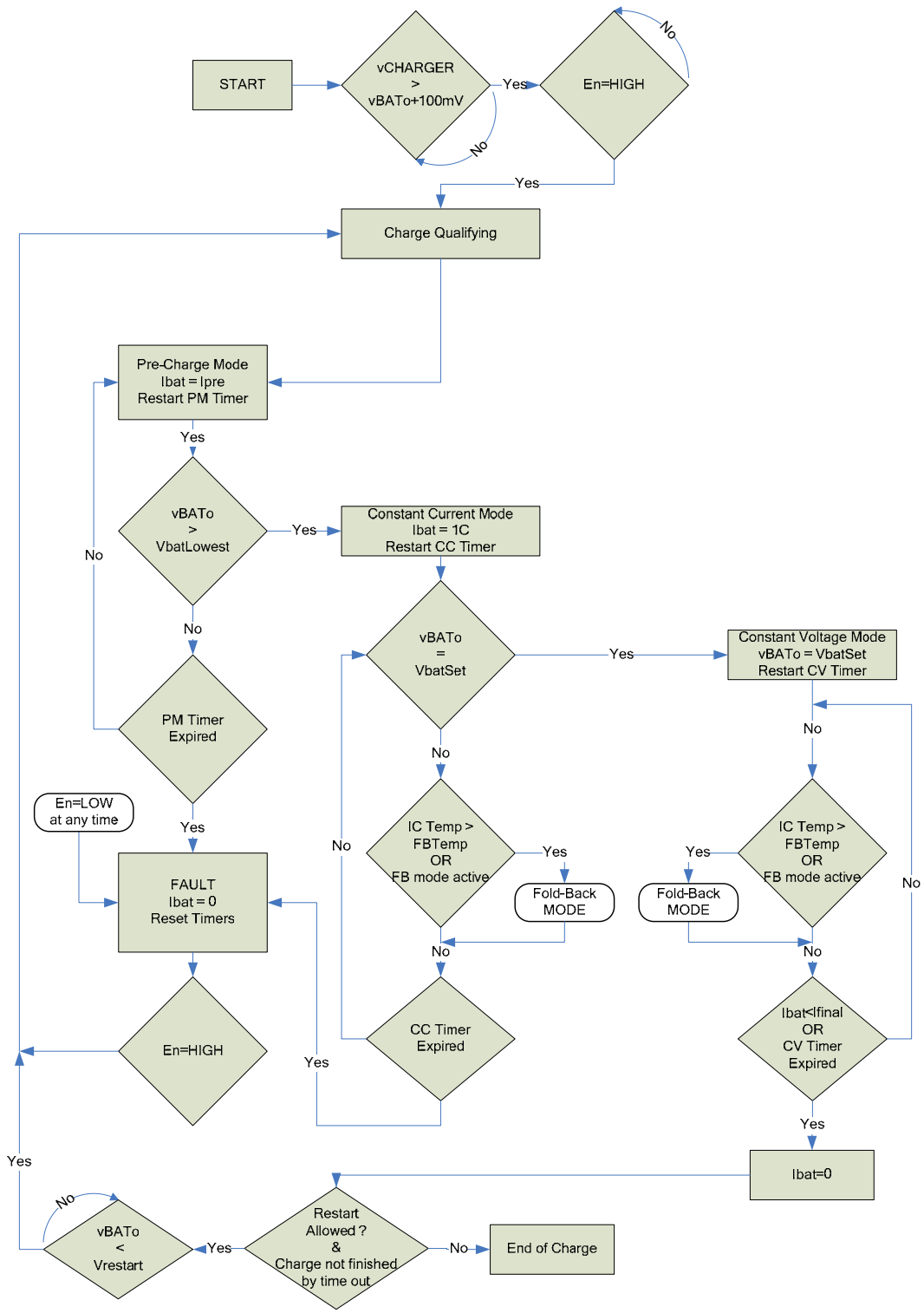
Using a small board (aprox: 10cm²) with 4 layers and the package back paddle soldered to the ground plain, with maximum via placement, the typical values for thermal resistance are θ_{JB}=14 C°/W and θ_{JA} = 35 C°/W.
θ_{JA} is dependent on the θ_{JBA} value for each application.
Although the circuit is otherwise within specification at -20C° the charge voltage accuracy is reduced to 1.5% below 0 °C.

This must be taken into consideration together with battery thermal security guidelines if by any reason the charger is to be operated bellow 0 °C.

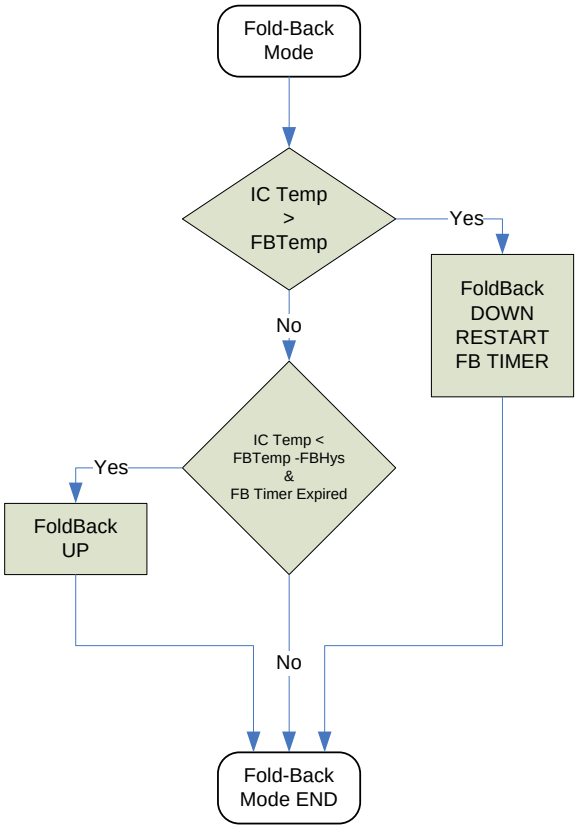
The above reference to the battery specification is valid for any other temperature value outside the battery maximum ratings for charge or discharge as the battery temperature is not monitored by the IC.

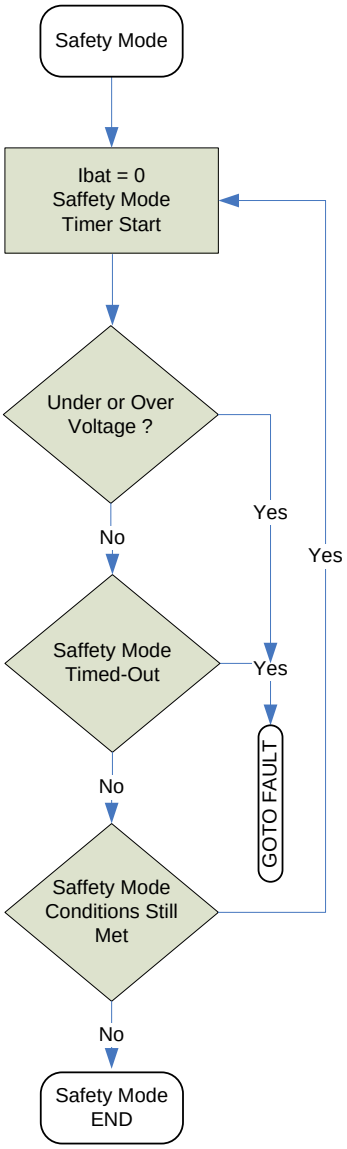
Note 2 R1 resistor connected between the iBAT pin and ground (page 4)

Battery Charger Flow Diagram



Detail on Fold-Back and Safety Modes





Battery Charger Functional Descriptions

Charge Qualifying

During qualifying, a small current (C/100) is injected into the battery; if the battery pin is above *VbatOpen* then the battery is open. If the battery voltage is below *VbatShort* then the battery is shorted. In either case charge is terminated with the appropriate error code. During qualifying, IC temperature and supply voltage are also checked.

Safety Mode

All the conditions checked during Qualifying Mode are also monitored during the rest of the charge cycle. If at any time the safeties are triggered, the charger enters Security Mode, where it waits for the acceptable conditions to be restored, or a time-out. If the time-out is reached, charge is terminated with the appropriate error code.

Pre-charge Mode

Before Fast Charge, the charger applies a Pre-charge current of C/10 to safely "revive" deeply discharged batteries. This mode is terminated when the battery voltage reaches VbatLowest or by time-out. In the first case the charger goes to Constant Current Mode, in the second, charge is terminated with the appropriate error code.

Constant Current Mode (Fast Charge)

The Battery is charged at 1C (externally defined current). This mode is terminated when battery voltage reaches VbatSet, or by time-out. The first case changes the charger to Constant Voltage mode, the later yields an error, with the appropriate code. During this mode current fold-back (due to high IC temperature) can occur.

Constant Voltage Mode

The Battery is charged with a constant voltage, but the current is still limited to 1C. This mode is terminated either by minimum current, or by time-out. This is the last mode, charge termination. Although in this case time-out is not an error, the charge termination method is still available by register read. During this mode current fold-back (due to high IC temperature) can occur.

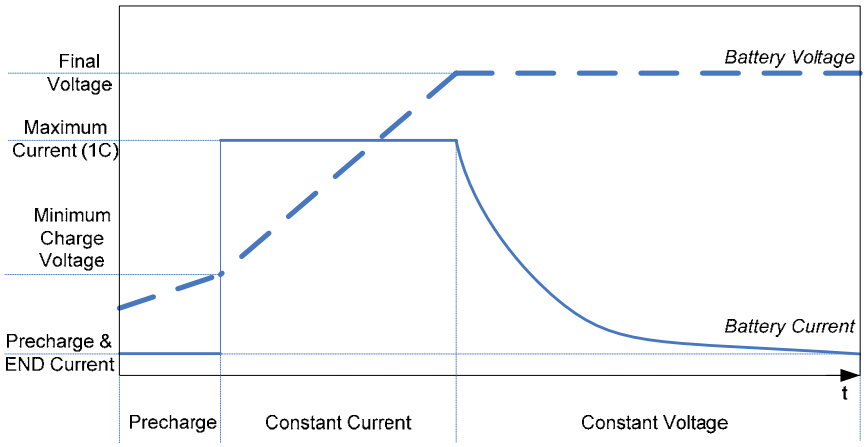
Restart Mode

If the "Restart Allowed" flag is high, the circuit enters a battery monitoring mode, where it waits for the battery voltage to reach *Vrestart* and then charge restarts. If the flag is low, charge is terminated.

Fold-Back Mode

During the charging procedure, the IC temperature can increase to unsafe temperatures due to higher dropout in the pass-device. To allow charging with higher input voltages, IC temperature is monitored when it reaches *FBTemp* the charge current is lowered until a safe operating temperature is reached. This is not a mode per se, it operates in the constant current and constant voltage modes.

Charge Profile



DC-DC CONVERTER

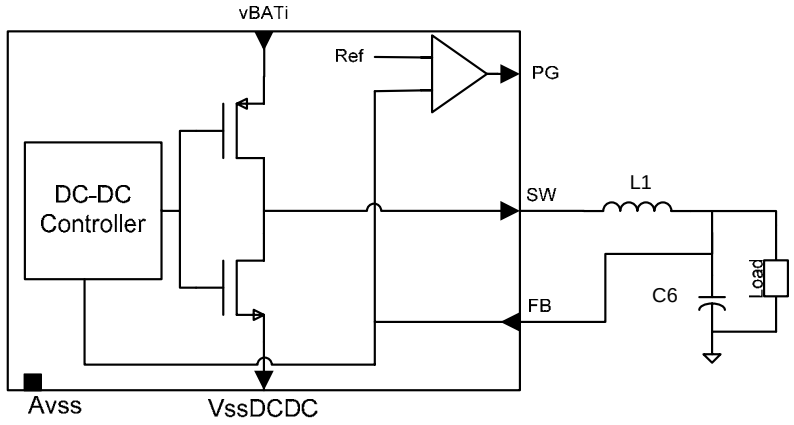
Description

The DC-DC is a 100 mA voltage mode controlled buck converter with internal power switches. It has the flexibility of several fixed output voltages and pulse skipping for low power operation. The following are the key considerations for the design:

- 700 mΩ PMOS power switch
- 500 mΩ NMOS synchronous rectifier
- Internal PID Loop Compensation
- Internal Soft Start
- Low quiescent current in both standby & PWM modes, non-switching
- Pulse skipping for high efficiency at light loads
- Anti-ring FET for low noise during pulse skipping & bulk diode protection
- Internal or external oscillator
- 1MHz switching frequency
- 10 mVrms output ripple
- 20 us settling time
- Over current protected

Functional Block Diagram

The internal block diagram for the DC-DC is shown below. The PWM voltage control loop comprises: the feedback DAC, the sigma delta modulator, digital PID compensator, pulse width modulator (PWM), gate drivers, and power FETs. When light loads are sensed and pulse skipping is enabled, the loop control is shut down and the output switches are turned off. The output voltage is then monitored by the comparator and the loop is re-enabled when the output voltage drops below a low threshold limit. During the shutdown time, everything except the output sensing comparator is disabled. Supply switch over-current protection is provided to protect the chip against overloads. Soft-start is provided by ramping up the internal reference from zero to the target value after power on reset.

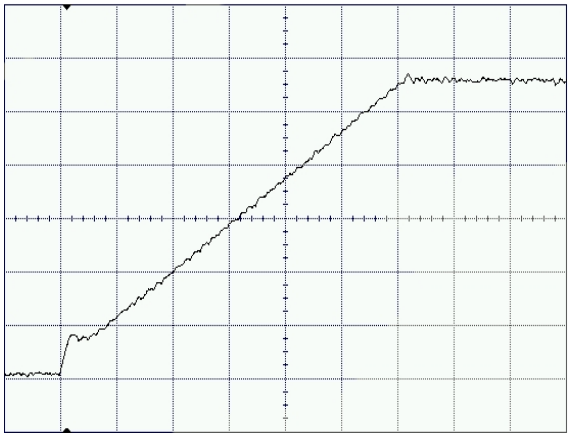


Top Level Block Diagram of the DC-DC Buck Converter

Electrical Characteristics

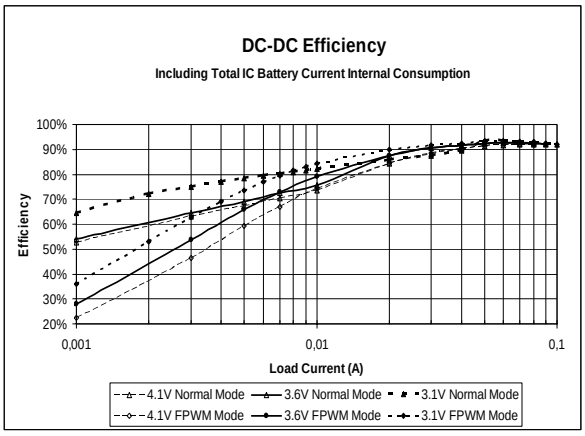
Generic	Min	Typ	Max	Units
vBATi Supply Voltage	2.9		4.242	V
Maximum Output Current			100	mA
Switching Frequency		1.024		MHz
Output Voltage	2.65	2.75	2.85	V
Output Ripple		10		mVrms
Output Voltage static error		3.63		%
Line Regulation		0.6		%

Startup (50Ω load)

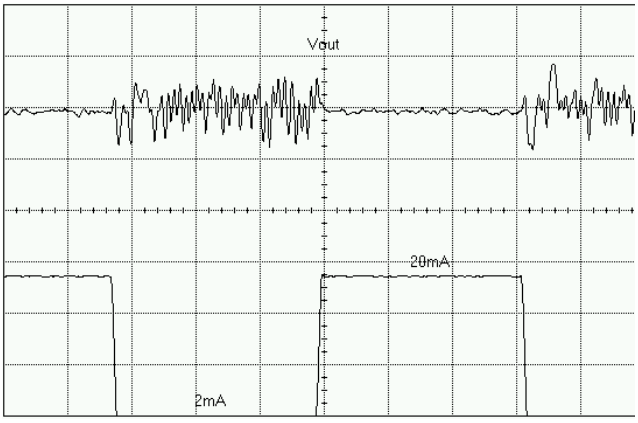


Output Voltage 0.5V/div Time scale 200us/div

DC-DC Efficiency
Including Total IC Battery Current Internal Consumption

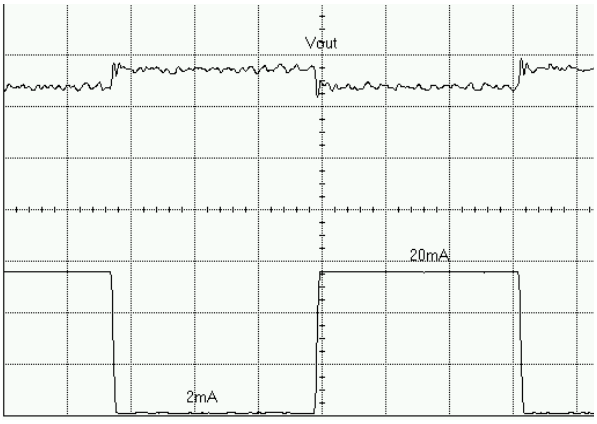


Load step 2mA to 20mA



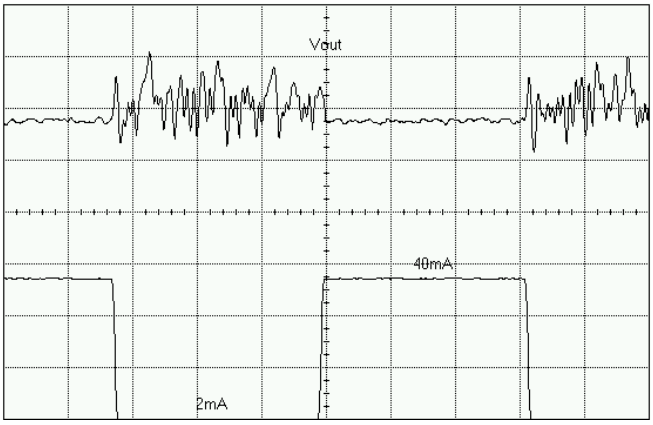
Output voltage 50mV/div Time scale 5ms/div

Load step 2mA to 20mA in forced PWM mode



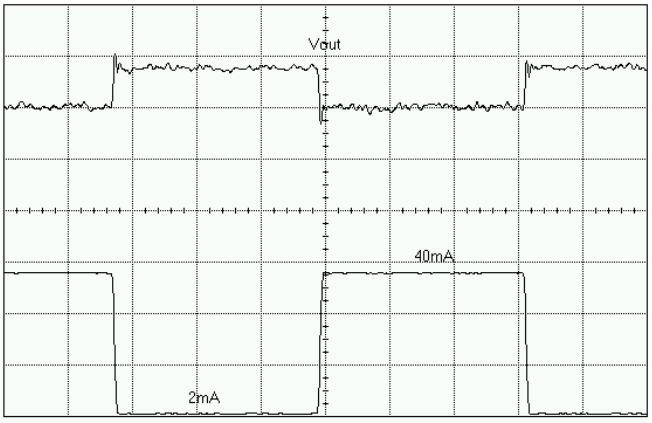
Output voltage 20mV/div Time scale 5ms/div

Load step 2mA to 40mA



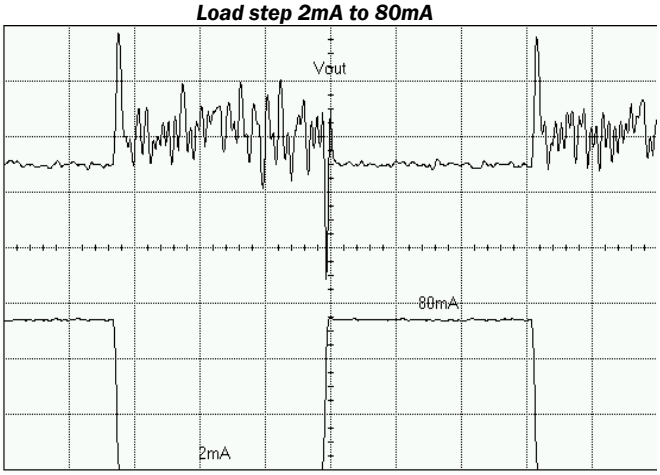
Output voltage 50mV/div Time scale 5ms/div

Load step 2mA to 40mA in forced PWM mode



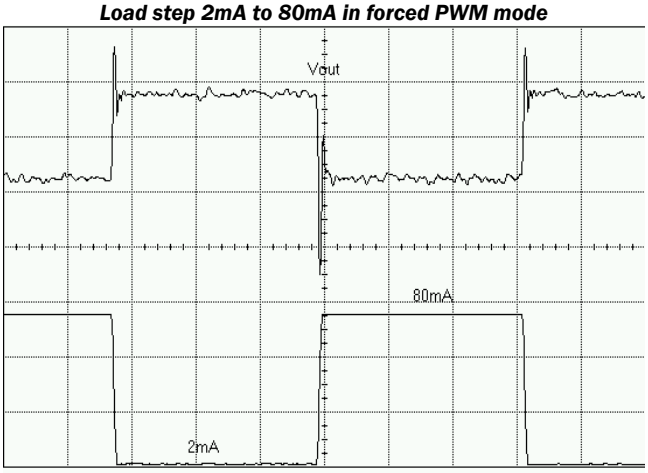
Output voltage 20mV/div Time scale 5ms/div

Load step 2mA to 80mA



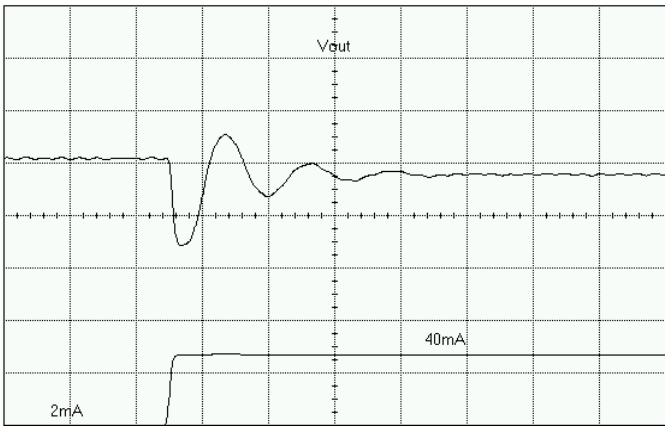
Output voltage 50mV/div Time scale 5ms/div

Load step 2mA to 80mA in forced PWM mode



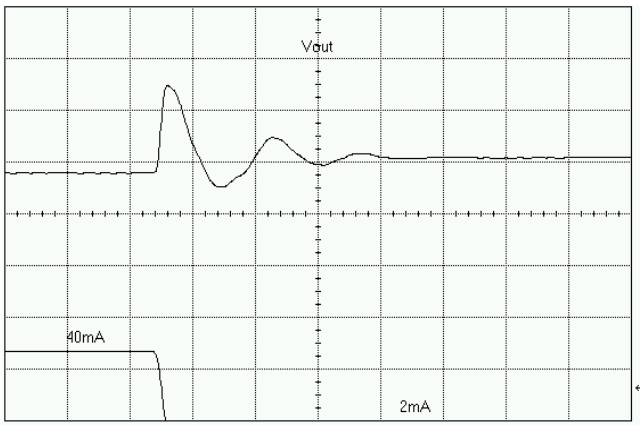
Output voltage 20mV/div Time scale 5ms/div

Load step 2mA to 40mA in forced PWM mode (zoom)



Output voltage 50mV/div Time scale 200us/div

Load step 2mA to 40mA in forced PWM mode (zoom)



Output voltage 50mV/div Time scale 200us/div

Operation in PWM Mode

In normal operation, the feedback voltage is scaled and the reference voltages subtracted to create an error signal. This error signal is digitized by a simple continuous-time sigma delta modulator. The resulting bit stream is processed by the digital compensator and the digital output word is presented to the pulse width modulator. The pulse width modulator switches the supply switch and synchronous rectifier at the switching frequency with an adjustable duty cycle control which is controlled by the PWM input word. The digital compensator determines the correct duty cycle to provide for the correct output voltage while ensuring stability.

The PWM mode operation can be forced by the host using two mechanisms.

Forced PWM

When bit 6 (FPWM) of register 25 is set , the DC-DC will operate always in PWM mode.

Forced PWM by Clock Request

When the bit 5 (CPWM) of register 25 is set the DC-DC will operate in forced PWM when the Clk26Rqst pin is high.
This guarantees that the DC-DC is running in PWM mode when the RF device is operating.

The default setting is FPWM=0 and CPWM=1, the DC-DC is by default in Forced PWM by Clock Request mode.

Operation in Pulse-Skipping Mode

The DC-DC can operate in a low power pulse skipping mode. In this mode, the synchronous rectifier current is sensed and when the synchronous rectifier current is sufficiently negative and the output voltage is on spec, the voltage mode control loop, PWM, and oscillator are shutdown. Everything is re-enabled when the output voltage drops below the error threshold. Then the system is re-enabled without soft-start.

Start Up and PowerDown

The DC-DC is automatically powered up without any intervention from the host, as the host can not operate without the DC-DC output voltage.

The DC-DC power up is triggered by one of the following events:

-Charger insertion when the IA3513 is in sleep mode

-On button push event when the IA3513 is in sleep mode.

To shutdown the DC-DC the bit 7 of register 25 must be cleared. When this is done the DC-DC is shut down and the IA3513 enters sleep mode powering down all blocks, but still being able to start a charge or detect the on button push.

Passive Network Selection

To allow for a fixed internal compensator, the external inductor and capacitor need to be specified and are not allowed to be chosen by the user of the regulator. The following table provides the only acceptable inductor and capacitor options:

Frequency = 1024 kHz

Component	Value	Recommended Maximum ESR	Tolerance
Inductor	10 μH	200 mΩ	20 %
Capacitor	10 μF	50 mΩ	20 %

HOST SYSTEM RESET - CLK32POG

Description

The IA3513 has the ability to reset the host in order to enforce safe startup operation, to do this the Clk32PoG pin of the IA3513 should be connected to the host reset pin.

Startup

The Clk32PoG pin stays low while the host supply voltage supplied by the IA3513 DC-DC is below 90% of its final value or the 32kHz clock is not available at the Clk32Out pin. With this logic functionality the host is guaranteed not to startup before the clock is available and the supply voltage is stable.

Start of Charge

Besides the startup functionality the Clk32PoG can also be used to reset the host during normal operation. This functionality is based on the charger start of charge event and interruption acknowledge mechanism.

The charge event is notified trough the standard IA3513 interruption mechanism and the status bit for this interruption is bit CHI on register 10.

If the interruption is not acknowledged within a 100ms period after the notification the IA3513 will reset the host.

The reset cycle is done by puling low the Clk32Pog during two cycles of the 32kHz clock.

A charge restart event does not trigger the interruption.

Software RESET

The Clk32PoG pin can be pulled low by register write.

This functionality is aimed for the production stage of the application, if there is a specific need for the primary host to be shut down in order for a secondary host to take control of the I2C bus (e.g. to program an E2PROM).

The reset control bit is bit 7 of register 49. This bit must be set to 1 to originate a reset (Clk32PoG low) and then set to 0 to release the reset (Clk32PoG high).

A software reset is triggered by the primary master and then released by the secondary master.

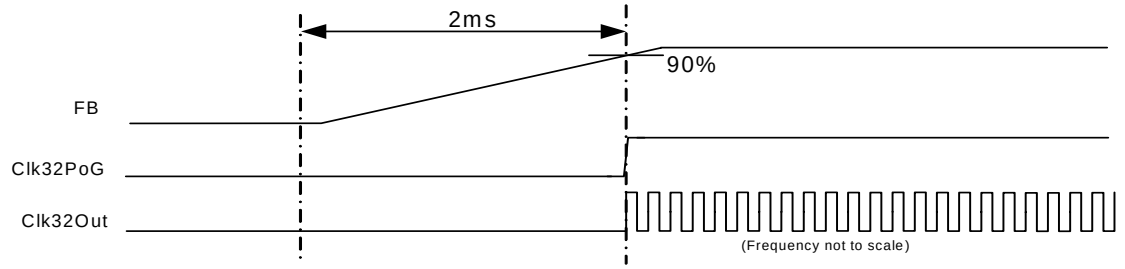
In order to avoid accidental write to this register position, register 49 is protected by a code word.

To enable access to this register, the “01101001” word must be written to register 48, any write to register 48 with a different content will disable the access to register 49.

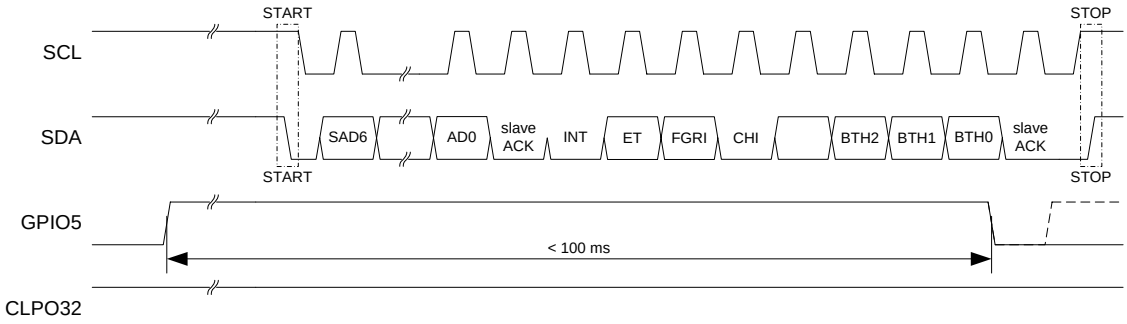
External RESET

The Clk32PoG output pin has pull-up capability limited to 1mA.This makes possible the external pull down of the Clk32PoG pin.

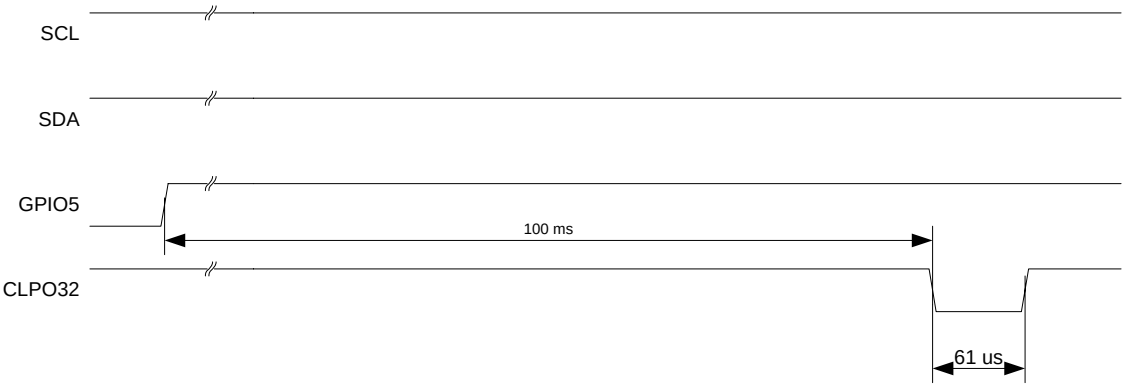
Timing Diagrams



Startup



Charge event with interruption acknowledged



Charge event with interruption not acknowledged

CLOCK GENERATOR

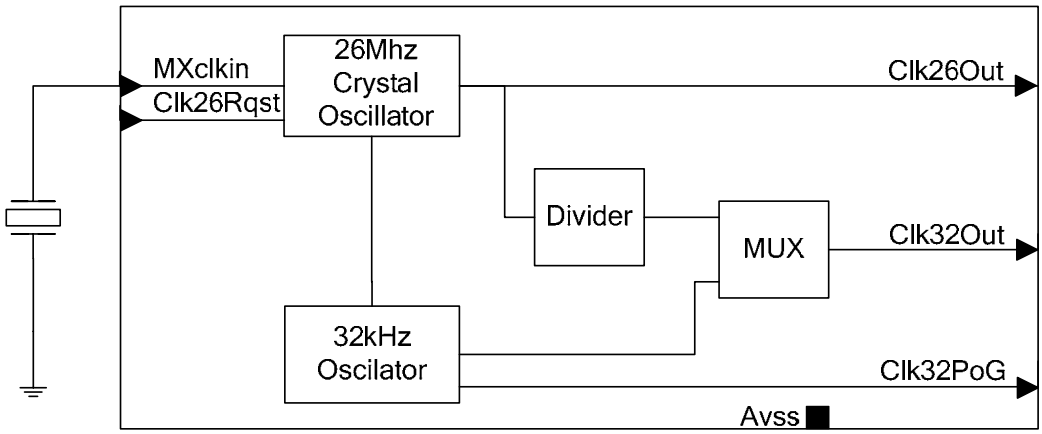
Description

The clock generator block, comprises a 26 MHz crystal oscillator and an internal low power 32 kHz oscillator. Various modes of operation are available for the generation of the 32 kHz clock, including division from the 26 MHz clock, when this clock is available and direct output from the calibrated 32 kHz internal oscillator.

Trimming of the 26MHz oscillator is available using 6 bits in register 23.

The 26MHz Oscillator is powered on and off by the Clk26Rqst input signal, the 32kHz clock is on by default but can be disabled using the I2C interface.

Clock Generator Functional Block Diagram

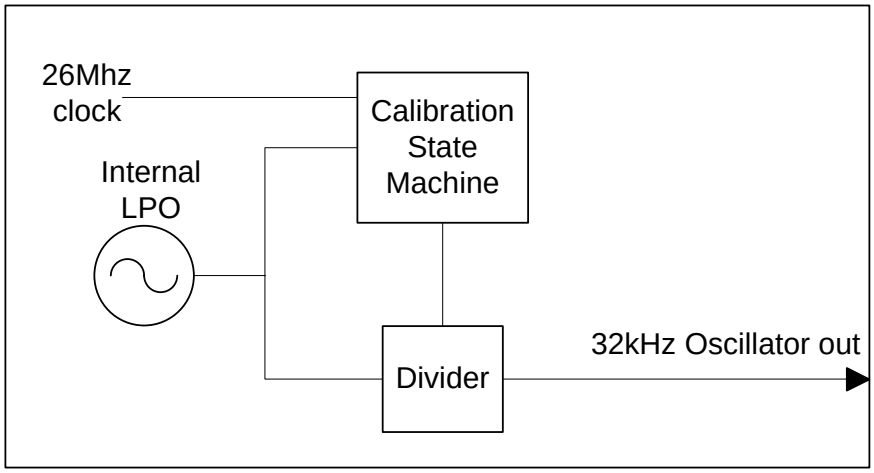


32kHz Oscillator Functional Description

The 32kHz oscillator is composed by 3 main blocks, a calibration state machine, a divider and a low power oscillator (LPO) with low temperature coefficient and high PSR in order to achieve the 250ppm accuracy specification.

During calibration the state machine compares the LPO frequency with the 26Mhz frequency generated by the crystal oscillator, in order to determine the correct modulo for the divider. At the end of a calibration cycle, the new divider modulo is loaded into the divider to obtain the 32kHz output.

32kHz Oscillator Functional Block Diagram



32 kHz Oscillator Modes of Operation

1) Power Up

This mode is valid after power up before any calibration has occurred.
In this mode the frequency of the Clk32Out output is guaranteed to be below 50kHz.

2) 26MHz Oscillator on Direct division Mode

The specification for the Clk32kHz clock is stated on the Electrical Characteristics table.

3) Calibrated Operation

During a time frame of up to 1.28s after the calibration of the 32 kHz Oscillator, the specification for the Clk32Out clock is stated on the Electrical Characteristics table.

32 kHz Oscillator Calibration modes

The internal 32kHz oscillator calibration can be done with 2 different approaches.

- **Continuous Calibration**
- **Calibration on Request**

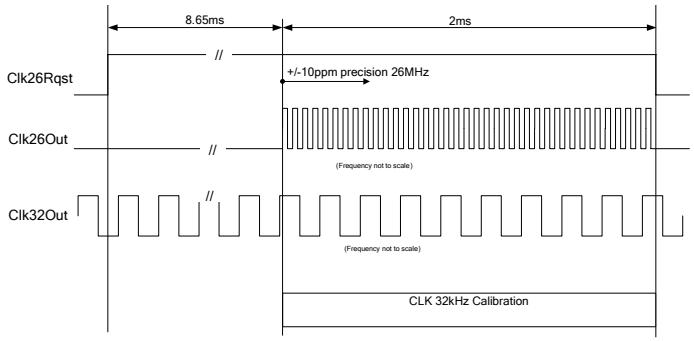
In continuous calibration mode the internal oscillator is always running calibration cycles whenever the 26MHz clock is available, this is the default mode.

If desired, calibration can also be run on request by I2C command, although the use of this mode is not advised.

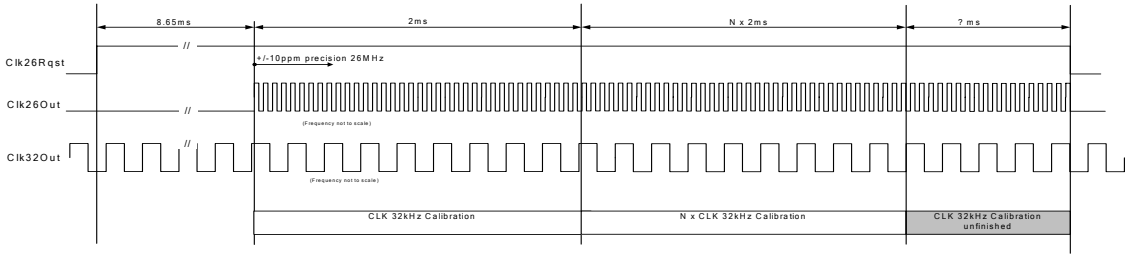
Independently of the calibration mode selected a calibration cycle is done after the rising edge of Clk26Rqst in order to enable correct sniff mode operation. This initial calibration cycle is only disabled if the calibration is turned off by register write to register 24.

The 32kHz internal oscillator control is done trough I2C using register 24.

When the 26MHz oscillator is enabled the 32kHz clock is generated by direct division of this clock. The transition between clock domains,26MHz division and internal oscillator, is guaranteed to be glitchless.



Calibration in sniff mode

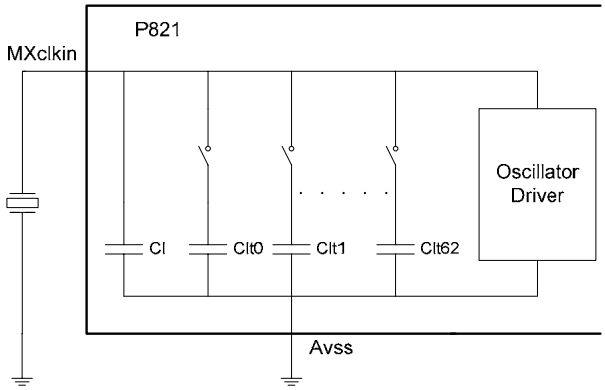


Continuous mode calibration

Crystal Oscillator frequency trimming

The 26 MHz crystal oscillator frequency can be trimmed using a 6bit word in register 23.

The frequency adjustment is done by changing the IA3513 internal load capacitance array connected to pin MXclkin.



The total trim capacitance is 3.465pF, and the LSB capacitance value is 55fF. For the midrange code the total capacitance is 9pF (Cl + Clt), in order to be compatible with the specification for the crystal typically used on the application.

Typical crystal specification

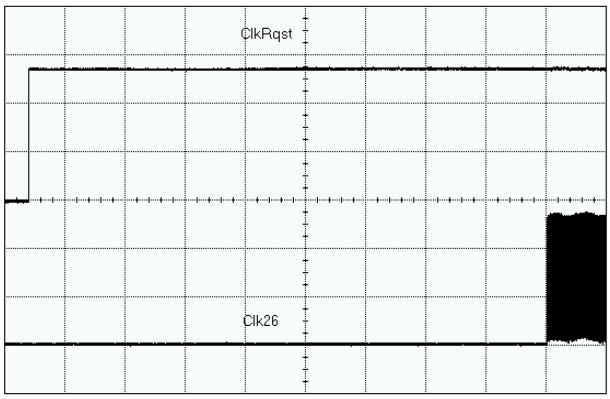
Parameter	Min
Nominal Frequency	26Mhz
Tolerance	+/-10ppm
Load Capacitance	9pF
Pulling sensitivity	15.5ppm/pF+/-10%

For the typical crystal, the tuning range is 53.7 ppm. This will guarantee the +/- 10ppm post trimming accuracy needed in the application.

The Clk26Out clock output will settle to the final frequency value 2ms after the occurrence of a write to the 6 bit trim word.

Crystal Oscillator Startup

The crystal oscillator is enabled by input pin CLK26Rqst. The clock CLK26out becomes active after converging to its final precision 8.65ms after the CLK26Rqst transition.



1V/div 1ms/div

Electrical Characteristics

Clk32out clock output

Generic	Min	Typ	Max	Units
Output Frequency		32.768		kHz
Duty cycle	30		70	%
Accuracy	-250		250	ppm
Load Capacitance	1		2.5	pF
Rise Time			1	us
Fall Time			1	us
Total jitter (measured for any 2 edges separated by at least 10ms)			250	ppm

Clk26out clock output

Generic	Min	Typ	Max	Units
Output Frequency		26		MHz
Rise time 10%-90%		1.5	6	ns
Fall time 10%-90%		1.5	6	ns
Duty Cycle	45	50	55	%
Phase noise at 10KHz			-121	dBc/Hz

DIGITAL INTERFACE

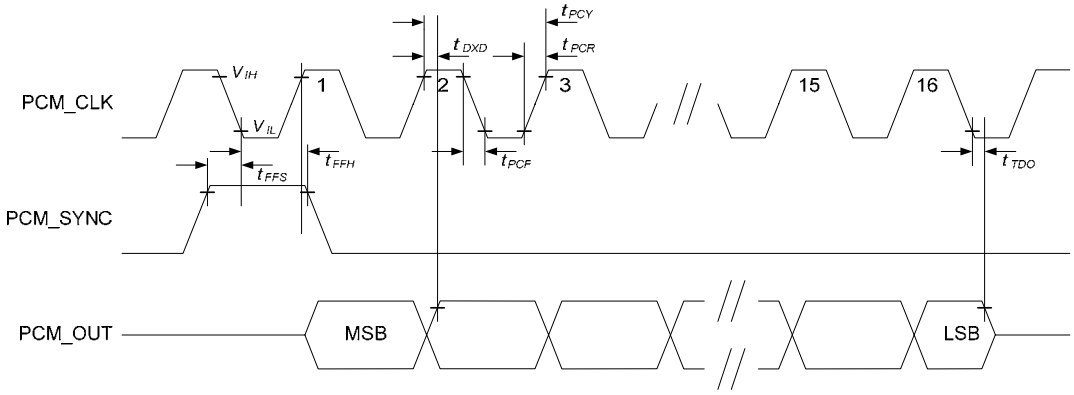
PCM Interface

Description

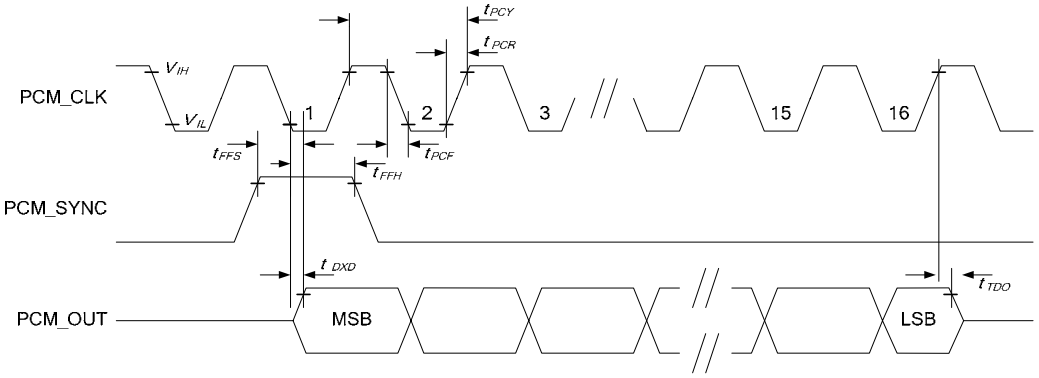
The PCM interface included in the IC is a flexible programmable data interface. The 16 bit linear PCM data transfer, both in the transmit and receive, is controlled by the PCM_SYNC and PCM_CLK inputs as well as the PCM control registers. The input and output words are 2's complement format.

The transmit and receive data start can be independently selected by using the transmit and receive data offset registers. Transmit output digital data can be selected to be present either on the positive or negative edge of the PCM_CLK. The PCM_CLK input supports a frequency range of 1024kHz, 2048kHz and 4096kHz; this frequency is auto detected by comparison with the 8 kHz PCM_SYNC input. The internal clock generator adjusts to the correct ratios at startup. The PCM_OUT output is tri-stated when valid output data is not present.

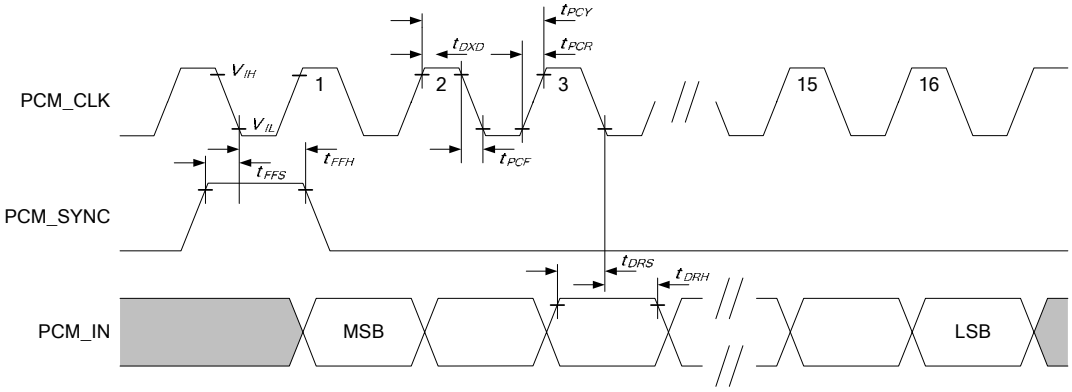
Timing Diagrams



Data Transmit timing diagram for output on positive edge



Data Transmit output on negative edge



Data Receive

Symbol	Parameter	Min	Typ	Max	Unit
tFSY	PCM_SYNC period	125		125	us
tPCY	PCM clock period	1/(8 x 512)		1/(8 x 128)	ns
tPCD	PCM clock duty cycle	45		55	%
tPCF	Fall time of clock			30	ns
tPCR	Rise time of clock			30	ns
tFFS	FS setup time to falling edge of clock	60			ns
tFFH	FS hold time to falling edge of clock	60			ns
tDXD	PCM data output delay			60	ns
tTDO	Delay from clock neg. edge to data off			60	ns
tDRS	PCM data input setup time	60			ns
tDRH	PCM data input hold time	60			ns

I2C Interface

Description

The I2C-IF block is configured to act as a slave device hanging on a standard I2C bus version 2.1. This bus uses a two wire only interface, with bidirectional clock and data lines. All devices hanging on the I2C bus (either masters or slaves) should only drive it using open drain (or alike) transceivers, which results in a wired-AND functionality when multiple devices try to drive the bus simultaneously.

The I2C address of the IA3513 is 1001111.

The clock stretching functionality isn't implemented in this slave, since it is not needed, because this is a relatively fast device. Thus, the SCL clock line can be considered as input only for this slave.

The SDA line is bidirectional and is both sampled, and driven by this slave. When driving the SDA line this slave only forces it low, relying on an external resistor to pull the line high.

Start and Stop conditions

Normally the SDA line is only allowed to change state when the SCL line is low. Whenever the SDA line transitions during SCL high, it is interpreted as a start or a stop condition, depending on the direction of the change: falling for a start condition, or rising for a stop condition.

Acknowledge

All 8 bit transfers either from master to slave, or the other way around, are terminated by an acknowledge bit (active low) driven by the receiving device.

Protocol Reset

As a failsafe mechanism, whenever there is a failure in the protocol (power loss, system reset, and so on) the slave can be reset by applying the following sequence:

1) Clock up to 9 cycles

2) Look for SDA high

3) Create start condition and slave will start listening for its slave address, or create stop condition and slave will go to the idle state (will wait for a new start condition)

Write operations

Random write

To perform a random write to a register, two words must be sent to the slave (after it has received the proper slave address). The first 8 bit word contains the address of the register that will be written. The following 8 bit word contains the data to write into the register. To end the random write, the master then sends a stop condition.

Sequential write

By starting with a random write, if the master keeps clocking in data words (8 bits each), then the address register keeps getting incremented and the data is written into the following registers in sequence. The slave always acknowledges each byte written (even if to invalid registers), as this indicates that the data was received properly (and not that was stored into a register). The current address rolls over from 255 to 0.

Read operations

Random read

To start a random register read, the master first starts with a dummy write cycle, specifying the address to be read. After sending the register address word (8 bits), a repeated start is generated and a read cycle follows, returning the contents of the addressed register. The master then does not acknowledge the read (acknowledge bit high), and follows with a stop condition, thus ending the cycle.

Sequential read

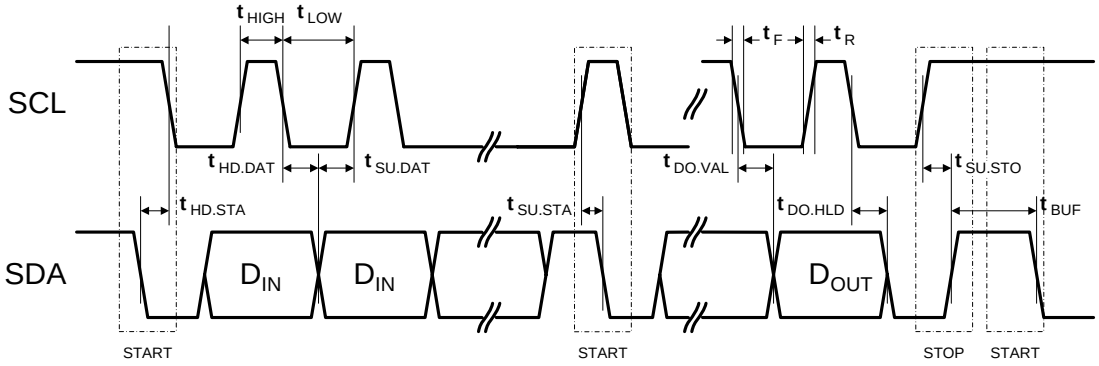
After some other read operation (random or current address read), if the master continues to acknowledge the read (acknowledge bit low) and clocking the slave's data out, then the address register keeps getting incremented and the registers are read in sequence until the master stops acknowledging and sends a stop condition. The register address is incremented by 1 every time the master acknowledges a read, and will roll over from 255 to 0 (this means that after reading the last valid register address, garbage will be read until the roll over happens).

Current address read

The address register keeps track of the last register accessed. A simple I2C read cycle always reads the last accessed register (either trough a read or through a write), as long as power is maintained, and a system reset isn't issued.

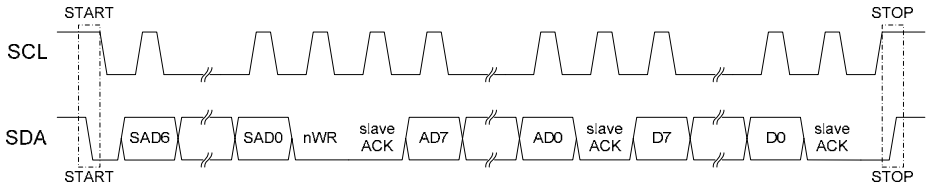
Timing Diagrams

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	Clock Frequency			400	kHz
t_{LOW}	Clock Pulse Width Low	1.3			µs
t_{HIGH}	Clock Pulse Width High	0.6			µs
t_R	Rise Time	20		300	ns
t_F	Fall Time	20		300	ns
$t_{HD.STA}$	Start Condition Hold Time	0.6			us
$t_{SU.STA}$	Start Condition Setup Time	0.6			us
$t_{HD.DAT}$	Input Data Hold Time	0		0.9	us
$t_{SU.DAT}$	Input Data Setup Time	100			ns
$t_{SU.STO}$	Stop Condition Setup Time	0.6			us
$t_{DO.VAL}$	Data Output Valid (from clock low)	45		245	ns
$t_{DO.HLD}$	Data Output Hold Time (from clock low)	45		245	ns
t_{BUF}	Time the bus must be free between transfers	1.3			us

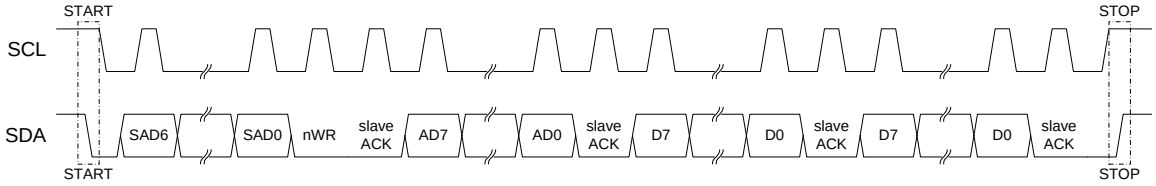


Bus Timing Diagram

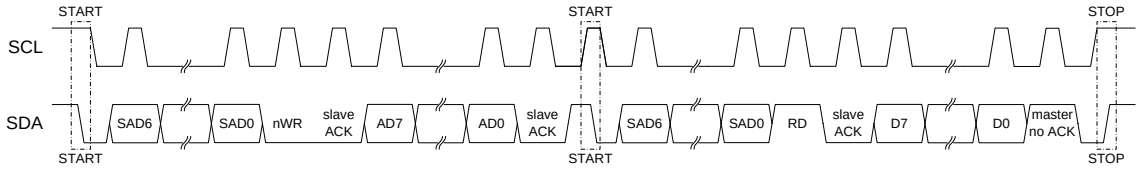
Field	Width (bits)	Description
SAD[6:0]	7	Slave address
AD[7:0]	8	Register address
D[7:0]	8	Register data



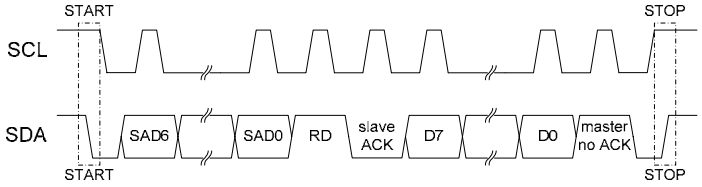
Timing Diagram for a Random Write



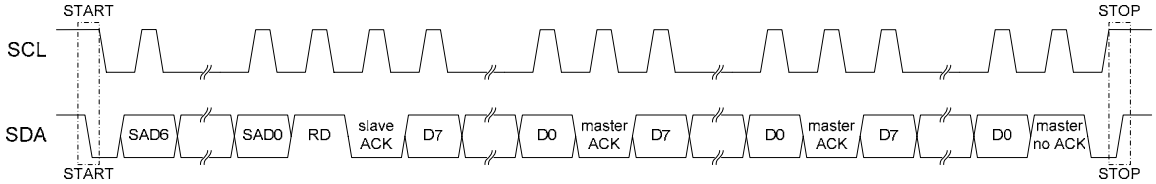
Timing Diagram for a Sequential Write



Timing Diagram for a Random Read



Timing Diagram for a Current Address Read



Timing Diagram for a Sequential Read (start from Current Address Read)

Note: Instead of a current address read, a random read may also precede a sequential read.

GENERAL PURPOSE I/Os

The five General Purpose Input Outputs (GPIOS) included in the IC enable high flexibility and the possibility to interact with various external devices such as leds and push buttons.

Hardware modes

The GPIOS are programmable in 6 different hardware modes:

- CMOS input, and output modes are standard modes operating based on the DC-DC output voltage.
- Low current open drain output, used to drive digital signals that can be referred to any voltage in the application by usage of a pull up resistor.
- Open drain mode is intended for switching output devices that require sink current up to 10mA; leds are the targeted devices in this application.
- High current open drain mode is intended for switching output devices needing sink currents up to 25mA; vibration motors are the targeted devices in this application.
- Wake up input is an enhanced CMOS input mode intended to read the state of the on/off button. This mode operates on the battery voltage and can be active and will be functional when the DC-DC is off.
- Charge notification Led driver. GPIO3 can be configured to automatically turn on an external Led whenever the Charge function is activated.

The availability of these modes for each GPIO is specified in the following table:

- • -available
- ❖ -default

GPIO	CMOS input	CMOS output	Low Current Open Drain	Open Drain	High Current Open Drain	Blink	Wake up input	Charge notification LED	Interruption Notification
1	•		•				❖		
2	•		•	•	❖	•			
3	•		•	❖		•		❖	
4	•		•	❖		•			
5	•	•		•		•			❖

All GPIO inputs include 1ms to 5ms input debounce protections. When in Wake up mode, GPIO1 activates a 100ms to 500ms debounce protection timer for this input.

Software modes

In addiction to the hardware modes, software programmable modes are also available. The GPIOS can be set to function in the following software modes:

- Normal mode, a high value in the pin is mapped to a high value in the register and vice-versa. The same is valid for a low value.
- Complementary mode, a high value in the pin is mapped to a low value in the register and vice-versa. The same is valid for a low value.
- Sticky mode, which is valid only for input configured GPIO pins. The corresponding GPIO status bit will only toggle to high once the input pin changes to high if in normal mode, or once the input pin changes to low if in complementary mode, and remain sticky to high independently of further changes in the value of the input pin. In order to change the status value back to low, a write must be made to the status register at the corresponding position. By writing '1' to a sticky GPIO the old value is kept, by writing '0' the sticky value is cleared. This mode is especially useful because it is possible to identify the interruption origin only by reading the status bits.
- Blink mode (valid only for output hardware mode in GPIOS 2, 3, 4, and 5), the GPIO will toggle continuously with on and off times set by register position. In this mode the GPIO state (high or low) written in the status register will be ignored.

Electrical Characteristics

Characteristics	Min	Typ	Max	Units
Maximum input voltage GPIO 1,2,3 and 4			4.242 (Battery Voltage)	V
Maximum input voltage GPIO 5			2.75 (DC-DC output)	V
VOL , CMOS mode (sink current 0.5mA)			0.185	V
VOH, CMOS mode (no load)	2.65 (DC-DC output)			V
VOH , CMOS mode (source current 0.5mA)	2.25			V
VIL ,CMOS mode (rising input)		1.5		V
VIH, CMOS mode (falling input)		1		V
Hysteresis , CMOS mode		0.5		V
Input impedance, open drain mode		25.5		Ω
Input impedance , open drain high current mode		13		Ω
Input impedance , open drain low current mode		220		Ω

GPIO Interruption Handling

Interruption signaling and notification is also available in the GPIO functionality. There is an interruption mask available by register write for all the GPIOS; when the correspondent mask bit is set, a transition in the GPIO will assert the interruption bit in Register 11.

Additional interruption sources

Besides the GPIOs there are five additional sources of interruption which are related with battery level.

Deeply discharged Battery interruption

When the Battery has crossed the deeply discharged threshold (2.9V), the DD bit in Register 11 will be set to 1. Upon this action the IC will start a 5 s countdown and shutdown.

Battery threshold interruption

An interruption will be notified when the battery has crossed the predefined battery level, in this case the LB bit in Register 11 will be set. The trigger level can be changed by register write on bits BTH of register 11 and the output of the comparator can be monitored on bit THO of register 6.

Battery charge termination interruption

When the battery charge is terminated an interruption is issued and bit CHT of 10 is set.
The battery status and control register (register 6) can be read to obtain information on the charge termination status,
Bit CF will be set if the charge has finished and bit Fault will be set if the charge has terminated abnormally.

Fuel gauge interruption

The Battery fuel gauge ADC can also be programmed to generate an interruption.
The ADC is activated on demand by asserting bit FGR of register 9, once the acquisition is concluded and the result available at bits FGB of register 9, the FGR bit is cleared to indicate that the operation has concluded.
In order to avoid the need for constant reading of register 9, the FGI bit can be set, to generate an interruption whenever an ADC acquisition is concluded. This interruption is notified on bit FGRI of register 10.
All interruptions previously mentioned can be enabled or disabled be using the interrupt mask register 16.

Charger Insertion (charge start) /Charger removal interruption

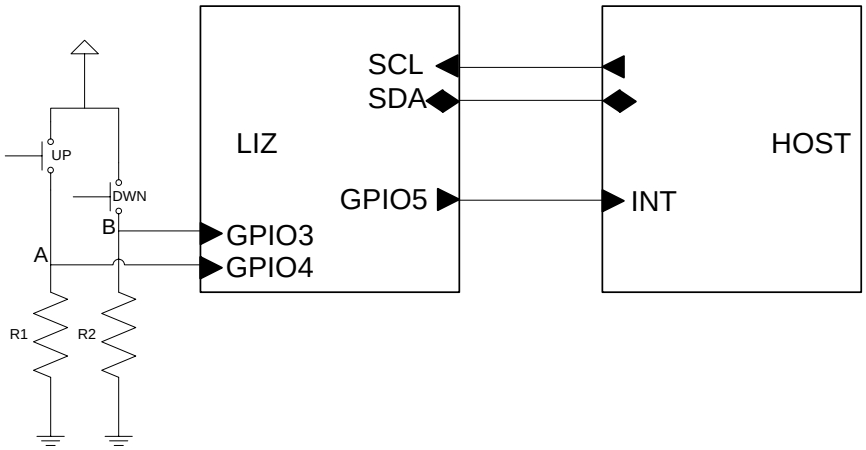
The CHI interruption is triggered both when the charger is inserted (plugged into the system), and when the charger is removed (unplugged from the system). Whenever such event happens, the CHI bit of register 10 will go high, as well as the INT bit. To ascertain which of the two events occurred, the register 6 should be read in addition, and if the charger was inserted, the ACHP bit will be at 1, or if it was removed the ACHP bit will be at 0.

Upon a charger insertion (charge start) event (ACHP bit at 1), if the CHI interrupt is not acknowledged within a 100 ms time window, a reset will be issued to the host as described in further details in the Host System Reset section.

Application Example 1 - Push Button Handling

The following example depicts the configuration and instruction set to handle two push buttons.

Receive (DA) channel volume UP/DOWN buttons are used in the example.



Configuration

The GPIOs used in this example are 3, 4 and 5.

GPIOs 3 and 4 are configured as CMOS inputs, with sticky mode enabled. This is done by setting the bits GPD3 and GPD4 of register 12 to '0' for input direction, and the bits GST3 and GST4 of register 15 to '1' in order to enable the sticky mode. The bits GPC3 and GPC4 of register 14 must be set to '0' also.

After the previous configurations are made, in order to clear any previous events on the inputs, a '0' should be written to bits GPS3 and GPS4 of register 11. This way GPIOS 3 and 4 status bits are cleared, and set to trigger when the inputs change from '0' to '1', which is compatible with the external pull downs implemented with resistors R1 and R2.

The interruption mask is set for GPIOS 3 and 4 by setting bits GI3 and GI4 of register 16. This will avoid the need for the host to be constantly reading the GPIO status as it can be notified by an interruption.

To enable the interruption notification through GPIO5, the bit GIN5 of register 13 must be set to '1' and the direction of this GPIO must be set to output by setting bit GPD5 of register 12 to '1'.

Operation

When the UP button is pushed, node A is pulled high. This transition will be detected by GPIO4, which will set the correspondent status bit (GPS4) of register 11 to '1'. As this GPIO is set to sticky mode, this value will be kept even when the button is depressed.

The change in GPS4 will trigger an interruption because GPIO4 was selected in the interruption mask; this interruption will be notified by GPIO5 which was selected for the interruption notification. The host will detect the interruption request, and read the contents of the GPIO status register.

The status register when read will have the GPS4 bit equal to '1', triggering the volume up action event. Then the host will perform the associated action to pressing this button (e.g. write the receive channel gain register).

This next step is optional and can be used if after detecting that the button was pressed, there is also the need to detect when the button is released. For this to be possible, the bit GPC4 of register 14 must first be set to '1' after the press action is detected. Afterwards the interrupt and push notification (sticky bit) of GPIO4 must be cleared by writing a '0' to the bits INT and GPS4 of register 11. Now the interrupt is set to trigger when the push button is released. When this happens GPIO5 will notify a new interruption, and the GPS4 will read '1' indicating that the GPIO4 has changed from '1' to '0' (due to the complementary mode being on). The host can then perform the associated action to releasing this button, and then should clear the GPC4 on register 14 (disable complementary mode).

To finalize the push button handling, the host acknowledges the interruption and the GPIO4 push/release notification by writing a '0' to the bits INT and GPS4 of register 11, thus clearing the interruption and the sticky bit value. Then the whole cycle can be restarted.

The operation of the DWN button is analogous.

Application Example 2 - Sticky Mode and Interruption Handling

To better illustrate how the sticky mode and the interruption should be handled the next example is depicted.

The following GPIO configuration is assumed:

- GPIO 1 - input, interruption unmasked, and sticky mode enabled for button handling
- GPIO 2, 3 and 4 - outputs, open drain
- GPIO 5 - output, interruption notification

The interrupt notification bits INT, DDB and LB of the register 11 can only be changed (cleared) by writing a '0'. When writing '1', their status remains unchanged. The GPS1 bit, because is configured as a sticky bit, behaves in the same way.

The GPIO5 can not be changed because it is an output, and is controlled by the interruption notification logic.

So if there is the need to change the GPIO 2, 3, or 4 output values, without disturbing the interrupt, and the sticky bits statuses, the safe value to be written to the register 11 (GPIO status and interruption handling register) is: "1 1 1 1 GPS2 GPS3 GPS4 1", where the GPSx values are the new values for the GPIO configured as outputs.

Application Example 3 – Interruption Notification, Single Register

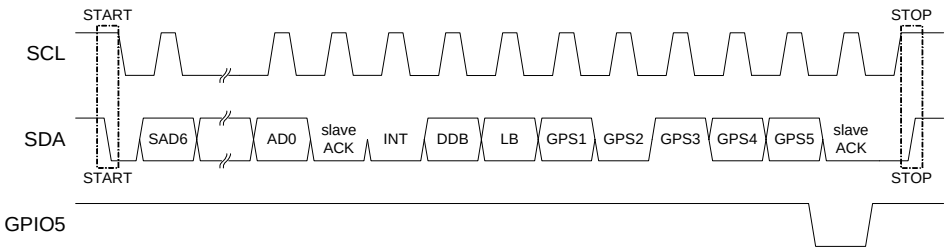
The recommended way to handle interruptions generated by the GPIO pins is to configure the corresponding bits in register 15 as sticky bits. In this way a status is kept on the interruption source, since the bit remains high (sticky) even if the signal at the GPIO pin changes its value. In the following example it is illustrated what happens when a new interruption is generated before an old one is acknowledged.

The following GPIO configuration is assumed:

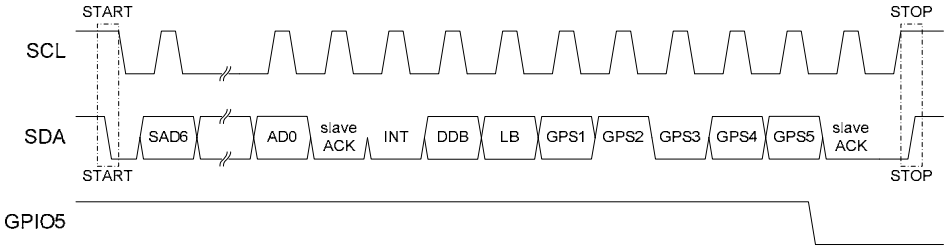
- GPIO 2 and 3 - inputs, with sticky mode enabled, and with interruption generation enabled (register 16)
- GPIO 5 - output, interruption notification

Then this chain of events takes place:

1) GPIO2 goes high, triggering an interruption.
2) GPIO5 goes high because it is configured for interrupt notification.
3) The host receives the interrupt request a proceeds to read register 11 (GPIO - Status and Interruption Handling) to determine the triggering event. I detects that GPS2 bit is high, thus it is responsible for the interrupt.
4) While the ISR runs on the host a new interrupt is generated on GPIO3.
5) After the ISR finishes handling the GPIO2 interruption, it proceeds to acknowledge it, by clearing bits INT and GPS2 in register 11. Because there is another pending interrupt in GPIO3, the GPIO5 interrupt notification pin is pulsed low like it is illustrated in the next figure (the size of this pulse is one SCL clock cycle):



6) The host detects a new interruption due to the pulse action on GPIO5 a proceeds to read register 11 again. It detects that GPS3 bit is high, thus it is responsible for this new interrupt.
7) After the ISR finishes handling the GPIO2 interruption, it proceeds to acknowledge it, by clearing bits INT and GPS3 in register 11. Because there is no other pending interrupt, the GPIO5 interrupt notification pin goes low as illustrated in the next figure:

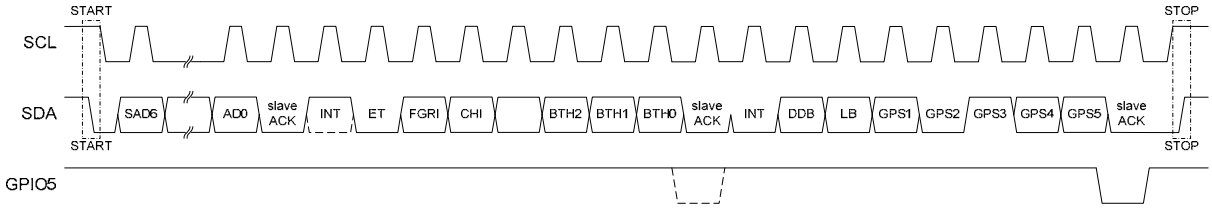


Application Example 4 – Interruption Notification, Dual Registers

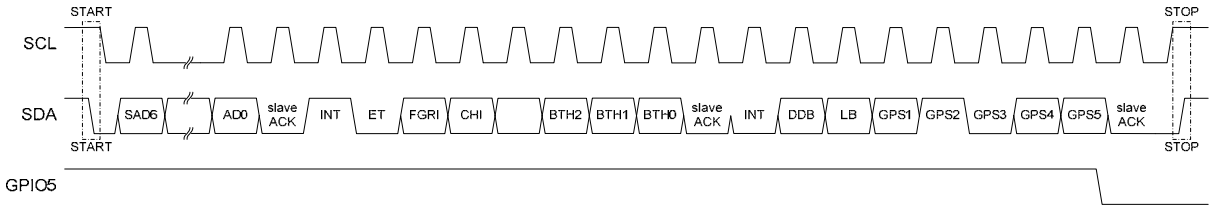
Interrupt sources must be detected from the two possible interrupt handling registers (register 10, and register 11) thus, it is recommended that the host determines the source of the generated interrupt by doing a burst read on both registers simultaneously.

Supposing that after reading these registers, the host detects an ET ("End of Tone") interruption, and a GPIO2 interruption, the best way to acknowledge them is by doing a burst write, clearing bit ET on register 10 and clearing bits INT and GPS2 on register 11. Care should be taken not to clear the bit INT on register 10 also, because on doing so a pulse on GPIO5 would be generated at the end of the register 10 data word (since the GPS2 was not yet acknowledged).

The following diagram illustrates what happens in the case that a new interrupt is generated on GPIO3, before the ISR acknowledges the previously detected sources (during the previous read).



This next diagram shows what happens, when acknowledging the interrupts on ET, and GPS3, if there are no more pending interrupts.



REGISTER BANK

Register Map

Description	Address	D7	D6	D5	D4	D3	D2	D1	D0
PCM Codec – Status / Control	0	PD	TM	RM	SDM	RDE	HP1	HP0	HPO
PCM Codec – Gain 1	1	RAG2	RAG1	RAG0	RDG1	RDG0	RSTDF	TDG1	TDG0
PCM Codec – Gain 2	2	TAG3	TAG2	TAG1	TAG0	STG3	STG2	STG1	STG0
PCM Interface – Status /Control	3	Dc	CFR1	CFR0	TE	Dc	Dc	Dc	Dc
PCM Interface – TX serial data offset	4	TOF7	TOF6	TOF5	TOF4	TOF3	TOF2	TOF1	TOF0
PCM Interface – RX serial data offset	5	ROF7	ROF6	ROF5	ROF4	ROF3	ROF2	ROF1	ROF0
Battery Charger – Status / Control	6	CF	FAULT	ACHP	THO	Dc	FBE	ARS	ENC
Battery Charger – Error Status	7	CVTO	CCTO	PTO	FBT	Dc	LCH	BOV	BUV
Battery Charger – Mode	8	TFB	CV	CC	PCM	SFM	FBB2	FBB1	FBB0
Battery Charger – Fuel Gauge and FoldBack	9	FGR	FGI	Dc	Dc	FGB3	FGB2	FGB1	FGB0
Battery Charger - Threshold and Interrupt Handling	10	INT	CHT	FGRI	CHI	BTH3	BTH2	BTH1	BTH0
GPIOS – Status and Interruption handling	11	INT	DDB	LB	GPS1	GPS2	GPS3	GPS4	GPS5
GPIOS – Direction	12				GPD1	GPD2	GPD3	GPD4	GPD5
GPIOS – HW Mode	13	GCL3	GIN5	GWU1	GOD2	GHD2	GOD3	GOD4	GOD5
GPIOS – Complementary Mode	14	Dc	Dc	Dc	GPC1	GPC2	GPC3	GPC4	GPC5
GPIOS – Sticky mode	15	Dc	Dc	Dc	GST1	GST2	GST3	GST4	GST5
GPIOS/General – Interruption Mask	16	CHT	DDB	LB	GI1	GI2	GI3	GI4	GI5
GPIOS2 Blink Control	17	BN22	BN21	BN20	BON21	BON20	BOFF22	BOFF21	BOFF20
GPIOS3 Blink Control	18	BN32	BN31	BN30	BON31	BON30	BOFF32	BOFF31	BOFF30
GPIOS4 Blink Control	19	BN42	BN41	BN40	BON41	BON40	BOFF42	BOFF41	BOFF40
GPIOS5 Blink Control	20	BN52	BN51	BN50	BON51	BON50	BOFF52	BOFF51	BOFF50
Tone Generator Control	21	FS1	FS0	EN1	EN0	EON1	EON0	EOFF	EOFF
Tone Generator Gain and Mix Mode	22	GG3	GG2	GG1	GG0	MM1	MM0		
Crystal Oscillator Control	23	XCT5	XCT4	XCT3	XCT2	XCT1	XCT0	Res (1)	Res (1)
Internal Oscillator Control	24	EN	CMO1	CMO0	CRQ	Res (1)	Res (1)		
DC-DC – Status	25	ON	FPWM	CPWM	Res (1)	Res (1)	DCT2	DCT1	DCT0
Host reset control access code register	48	HRC7	HRC6	HRC5	HRC4	HRC3	HRC2	HRC1	HRC0
Host reset Control	49	HRST	Dc	Dc	Dc	Dc	Dc	Dc	Dc
PCM Codec test path Control 1	62	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
PCM Codec test path Control 2	63	Res (1)	SP9	SP8	Res (1)	Res (1)	Res (1)	Res (1)	Res (1)
Internal Configuration Access Control	127	IAC7	IAC6	IAC5	IAC4	IAC3	IAC2	IAC1	IAC0
Internal Configuration	100	Res (1)	Res (1)	Res (1)	XTSD1	XTSD0	Res (1)	Res (1)	Res (1)

Note 1): Reserved bits should be kept at their default values for optimum performance of the circuit. No deadlocks should occur if they are changed to a different value. These bits are reserved for future use and are not to be used by the application software.

Register Description

Register 0 - PCM Codec Register – Status / Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PD	TM	RM	SDM	RDE	HP1	HP0	HPO
Default Values	1	1	1	1	1	1	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7]	PD	Codec Power Down
D[6]	TM	TX channel mute
D[5]	RM	RX channel mute
D[4]	SDM	SideTone mute
D[3]	RDE	RX dither enable 0-> disabled 1->enabled
D[2:1]	HP	High pass filter cutoff frequency and bypass control 00->HP bypassed 01->100Hz 10->200Hz 11->300Hz
D[0]	HPO	High pass filter order 0-> 2nd order 1->4th order

Register 1 - PCM Codec Register – Gain 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RAG2	RAG1	RAG0	RDG1	RDG0	RSTDF	TDG1	TDG0
Default Values	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W

Bit	Name	Functions
D[7:5]	RAG	Receive Analog gain control 0->-24 dB 100->0 6dB steps
D[4:3]	RDG	Receive Digital gain control 0->-3 dB 11->6dB 3dB steps
D[2]	RSTDF	Reset to the digital filters (write 1 to issue a reset pulse)
D[1:0]	TDG	Transmit Digital gain control 0->0dB 10->+2dB 1dB steps

Register 2 - PCM Codec Register – Gain 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TAG3	TAG2	TAG1	TAG0	STG3	STG2	STG1	STG0
Default Values	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7:4]	TAG	Transmit Analog gain control 0->0dB 1000->+24 3dB steps
D[3:0]	STG	Side tone gain control 0->-30dB 1010->0 3dB steps

Note: The sidetone processing is done in the digital block, the TX signal that is fed into the RX channel will be affected by the RX gain.

Register 3 - PCM Interface Register – Status /Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Dc	CFR1	CFR0	TE	Dc	Dc	Dc	Dc
Default Values	0	0	0	0	0	0	0	0
Read/Write	R	R	R	W/R	R	R	R	R

Dc- Read only bits which are don't care bits and will have no effect if written.

Bit	Name	Functions
D[6:5]	CFR	PCM_CLK to PCM_SYNC ratio. Ratio 00-> unknown 01->128 10->256 00->512
D[4]	TE	Transmit edge 0-> positive 1-> negative

Register 4 - PCM Interface Register – TX serial data offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TOF7	TOF6	TOF5	TOF4	TOF3	TOF2	TOF1	TOF0
Default Values	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7:0]	TOF	TX serial data offset

Register 5 - PCM Interface – RX serial data offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ROF7	ROF6	ROF5	ROF4	ROF3	ROF2	ROF1	ROF0
Default Values	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7:0]	ROF	RX serial data offset

Register 6 - Battery Charger – Status / Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CF	FAULT	ACHP	THO	Dc	FBE	ARS	ENC
Default Values	0	0	0	0	0	1	1	1
Read/Write	R	R	R	R	R	R/W	R/W	R/W

Bit	Name	Functions
D[7]	CF	Charge Finished –Status bit-
D[6]	FAULT	Charge Error (FAULT)
D[5]	ACHP	vCHARGER Voltage present (vCHARGER > 4.35)
D[4]	THO	Threshold comparator output 0->below threshold 1->above threshold -Status bit-
D[2]	FBE	Fold Back enable 0->disable 1-> enable
D[1]	ARS	Allow auto-restart of charge
D[0]	ENC	Enable Charger

Status bits state results from external conditions and will be updated dependent on the current condition.

This implies that the state is not guaranteed on wake up.

Register 7 - Battery Charger – Error Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CVTO	CCTO	PTO	FBT	Dc	LCH	BOV	BUV
Default Values	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bit	Name	Functions
D[7]	CVTO	Constant Voltage Mode Time Out
D[6]	CCTO	Constant Current Mode Time Out
D[5]	PTO	Precharge Time-Out
D[4]	FBT	FoldBack Mode Termination
D[3]	Dc	
D[2]	LCH	Low Charger Voltage
D[1]	BOV	Battery Overvoltage (open)
D[0]	BUV	Battery Undervoltage (short)

Register 8 - Battery Charger – Mode and FoldBack Information

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TFB	CV	CC	PCM	SFM	FBB2	FBB1	FBB0
Default Values	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bit	Name	Functions
D[7]	TFB	Thermal FoldBack Mode
D[6]	CV	Constant Voltage Mode
D[5]	CC	Constant Current mode
D[4]	PCM	Precharge Mode
D[3]	SFM	Safety Mode
D[2]	FBB2	Fold Back information bit 2
D[1]	FBB1	Fold Back information bit 1
D[0]	FBB0	Fold Back information bit 0 (000 means no foldback, 111 is 87.5% foldback on) → step 12.5%

Register 9 - Battery Charger – Fuel Gauge

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FGR	FGI	Dc	Dc	FGB3	FGB2	FGB1	FGB0
Default Values	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R	R	R	R	R	R

Bit	Name	Functions
D[7]	FGR	Fuel Gauge Reading request 1-> request 0-> reading available on FGB.
D[6]	FGI	Fuel Gauge Reading available interrupt mask 1-> interruption active 0->inactive
D[3:0]	FGB	Fuel Gauge information 4 bit ADC with range 3.15V to 4V (same range as the threshold interruption)

Register 10 - Battery Charger - Threshold and Interrupt Handling

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INT	CHT	FGRI	CHI	BTH3	BTH2	BTH1	BTH0
Default Values	0	0	0	0	0	1	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7]	INT	Interruption notification bit - 0-> inactive 1-> active
D[6]	CHT	Charge Termination interrupt notification
D[5]	FGRI	Fuel Gauge Reading available interrupt notification
D[4]	CHI	Charge event interrupt notification
D[3:0]	BTH	Battery threshold selection for interrupt generation 4 bit selection range 3.15V to 4V

Register 11 - GPIOS – Status and Interruption Handling

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INT	DDB	LB	GPS1	GPS2	GPS3	GPS4	GPS5
Default Values	0	0	0	0	1	1	1	0
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7]	INT	Interruption notification bit - 0-> inactive 1-> active
D[6]	DDB	Deeply discharged battery interrupt notification
D[5]	LB	Battery threshold crossing interrupt notification (threshold set in register 10 bits BTH)
D[4:1]	GPS	GPIO state 0-> low 1-> high
D0		GPIO state 0-> low 1-> high When the interruption notification mode is selected GPS5 is a copy of the INT bit.

Register 12 - GPIOS - Direction

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Dc	Dc	Dc	GPD1	GPD2	GPD3	GPD4	GPD5
Default Values	0	0	0	0	1	1	1	1
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[4:0]	GPD	GPIO direction 0-> input 1->output

Register 13 - GPIOS – HW Mode

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	GCL3	GIN5	GWU1	GOD2	GHD2	GOD3	GOD4	GOD5
Default Values	1	1	1	0	1	1	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7]	GCL3	GPIO3 Charger led function 0->disable 1->enable
D[6]	GIN5	GPIO5 Interrupt notification 0-> disable 1-> enable
D[5]	GWU1	GPIO 1 wake up mode 0->disable 1->enable
D[4]	GOD2	GPIO 2 open drain mode 0->disable 1->enable
D[3]	GHD2	GPIO 2 high current open drain mode 0->disable 1->enable
D[2]	GOD3	GPIO 3 open drain mode 0->disable 1->enable
D[1]	GOD4	GPIO 4 open drain mode 0->disable 1->enable
D[0]	GOD5	GPIO 5 open drain mode 0->disable 1->enable

Register 14 - GPIOS – Complementary Mode

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Dc	Dc	Dc	GPC1	GPC2	GPC3	GPC4	GPC5
Default Values	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[4:0]	GPC	GPIO complementary mode 0-> disabled 1->enabled

Register 15 - GPIOS – Sticky Mode

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Dc	Dc	Dc	GST1	GST2	GST3	GST4	GST5
Default Values	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[4:0]	GST	GPIO Sticky mode 0-> disabled 1->enabled

Register 16 - GPIOS/General – Interruption Mask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CHT	DDB	LB	GI1	GI2	GI3	GI4	GI5
Default Values	1	1	1	1	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7]	CHT	Charge Termination interruption mask 0-> disabled 1->enabled
D[6]	DDB	Deeply discharged battery Interruption mask 0-> disabled 1->enabled
D[5]	LB	Battery threshold Interruption mask 0-> disabled 1->enabled
D[4:0]	GI	GPIO Interruption mask 0-> disabled 1->enabled

Register 17 - GPIO2 Blink Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BN22	BN21	BN20	BON21	BON20	BOFF22	BOFF21	BOFF20
Default Values	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7:5]	BN2	Number of blink cycles 000->off 001->1 cycle ….110->6 cycles 111->continuous
D[4:3]	BON2	On time 00->50ms 01->100ms 10->150ms 11->300ms
D[2:0]	BOFF2	Off Time 000->50ms 001->200ms 010->500ms 011->1s 100->2s 101->3s 110->4s 111->5s

Register 18 - GPIO3 Blink Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BN32	BN31	BN30	BON31	BON30	BOFF32	BOFF31	BOFF30
Default Values	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7:5]	BN3	Number of blink cycles 000->off 001->1 cycle ….110->6 cycles 111->continuous
D[4:3]	BON3	On time 00->50ms 01->100ms 10->150ms 11->300ms
D[2:0]	BOFF3	Off Time 000->50ms 001->200ms 010->500ms 011->1s 100->2s 101->3s 110->4s 111->5s

Register 19 - GPIO4 Blink Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BN42	BN41	BN40	BON41	BON40	BOFF42	BOFF41	BOFF40
Default Values	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7:5]	BN4	Number of blink cycles 000->off 001->1 cycle ….110->6 cycles 111->continuous
D[4:3]	BON4	On time 00->50ms 01->100ms 10->150ms 11->300ms
D[2:0]	BOFF4	Off Time 000->50ms 001->200ms 010->500ms 011->1s 100->2s 101->3s 110->4s 111->5s

Register 20 - GPIO5 Blink Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BN52	BN51	BN50	BON51	BON50	BOFF52	BOFF51	BOFF50
Default Values	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7:5]	BN5	Number of blink cycles 000->off 001->1 cycle ….110->6 cycles 111->continuous
D[4:3]	BON5	On time 00->50ms 01->100ms 10->150ms 11->300ms
D[2:0]	BOFF5	Off Time 000->50ms 001->200ms 010->500ms 011->1s 100->2s 101->3s 110->4s 111->5s

Register 21 - Tone Generator Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FS1	FS0	EN1	EN0	EON1	EON0	EOFF	EOFF
Default Values	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7:5]	FS	Tone Frequency 00->off 01->1kHz 10->500Hz 11->250Hz
D[4:3]	EN	Tone Mode 00->continuous 01-> 1 beep 10-> 2 beeps 11->3 beeps
D[2:0]	EON	On Time 00->25ms 01-> 50ms 10-> 75ms 11->100ms
D[2:0]	EOFF	On Time 00->50ms 01-> 100ms 10-> 300ms 11->500ms

Register 22 - Tone Generator Gain and Mix Mode

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	GG3	GG2	GG1	GG0	MM1	MM0	Dc	Dc
Default Values	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Name	Functions
D[7:4]	GG	Tone Generator gain 0000->dB 0001->-3dB 0010->-6dB 1111->-60dB
D[3:2]	MM	Mix mode 00->no mixing PCM data is muted 01->tone added to PCM data 10->tone added to PCM data and the result of the addition is attenuated 6dB to avoid clipping.

Register 23 - Crystal Oscillator Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	XCT5	XCT4	XCT3	XCT2	XCT1	XCT0	Res	Res
Default Values	1	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7:2]	XCT	Crystal Oscillator trim bits
D[1:0]	Res	Reserved (must be kept at the default value)

Register 24 - Internal Oscillator Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	EN	CMO1	CMO0	CRQ	Res	Res	Dc	Dc
Default Values	1	1	1	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Name	Functions
D[7]	EN	32 KHz clock output enable
D[6:5]	CMO	Calibration mode: 11 -> continuous mode; 10 -> continuous mode; 01 -> request mode; 00 -> calibration off
D[4]	CRQ	Calibration request (only valid in request mode): write 1 to start calibration (read 0 when calib. Ends)
D[3:2]	Res	Reserved (must be kept at the default value)

Register 25 –DC-DC Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	EN	FPWM	CPWM	Res	Res	DCT2	DCT1	DCT0
Default Values	1	0	1	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7]	EN	DC-DC enable 1-> enable 0-> disable When the DC-DC is disabled the IC enters power down mode
D[6]	FPWM	Forced PWM mode enable 1-> enable 0-> disable
D[5]	CPWM	Forced PWM by clock request mode enable 1-> enable 0-> disable
D[4:3]	Res	Reserved (must be kept at the default value)
D[2:0]	DCT	DC-DC offset correction trim bits [-100mV , +100mV] 000->0V 001->+50mV 010->+100mV 111->-50mV 110->-100mV

Register 48 – Host reset control access code register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HRC7	HRC6	HRC5	HRC4	HRC3	HRC2	HRC1	HRC0
Default Values	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bit	Name	Functions
D[7:0]	HRC	Control code “01101001” to access register 49. Register read = 0 implies locked state Register read = 1 implies unlocked state

Register 49 – Host reset Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HRST	Dc	Dc	Dc	Dc	Dc	Dc	Dc
Default Values	0	0	0	0	0	0	0	0
Read/Write	R/W	R	R	R	R	R	R	R

Bit	Name	Functions
D[7]	HRST	Host reset 1-> reset (Clk32PoG=0) 0->no reset (Clk32PoG=1)

Register 62 -PCM Codec Test Path Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Default Values	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7:0]	SP[7:0]	Enable for Test path SP0 to SP7

Register 63 – PCM Codec Test Path Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Res	SP9	SP8	Res	Res	Res	Res	Res
Default Values	1	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Functions
D[7]	Res	Reserved (must be kept at the default value)
D[6:5]	SP[9:8]	Enable for Test path SP9 and SP8
D[4:0]	Res	Reserved (must be kept at the default value)

Register 127- Internal Configuration Access Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IAC7	IAC6	IAC5	IAC4	IAC3	IAC2	IAC1	IAC0
Default Values	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

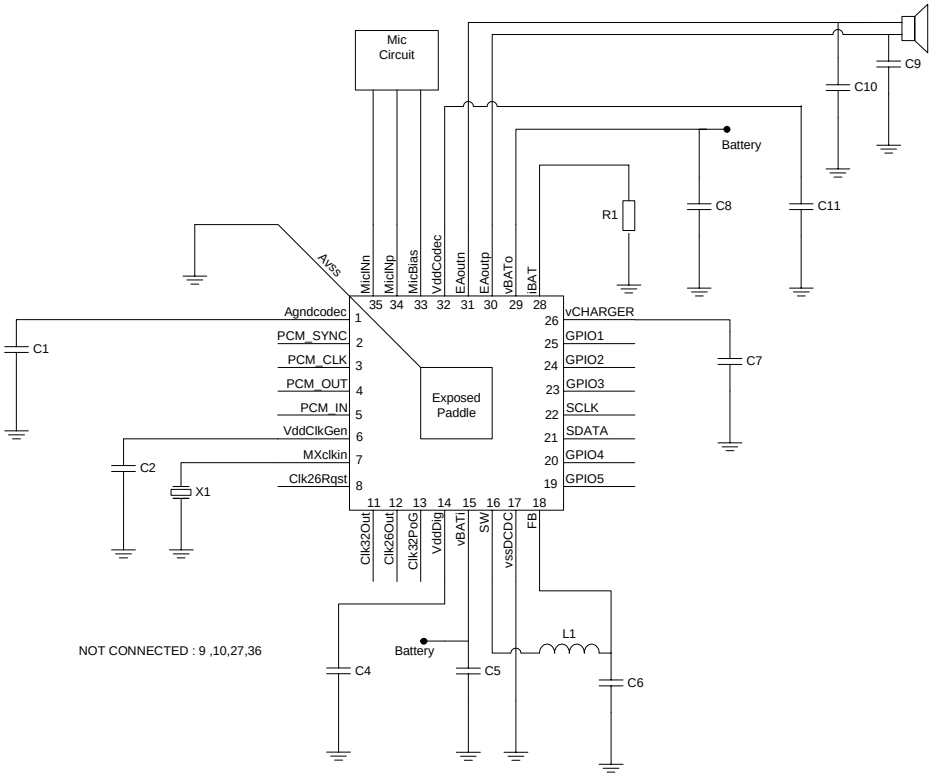
Bit	Name	Functions
D[7:0]	IAC	Control code sequence to access register 100 , CA Hex followed by FE Hex Any other value written to this register locks the access again Register read = 0 implies locked state Register read = 1 implies unlocked state

Register 100- Internal Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Res	Res	Res	XTSD1	XTSD0	Res	Res	Res
Default Values	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

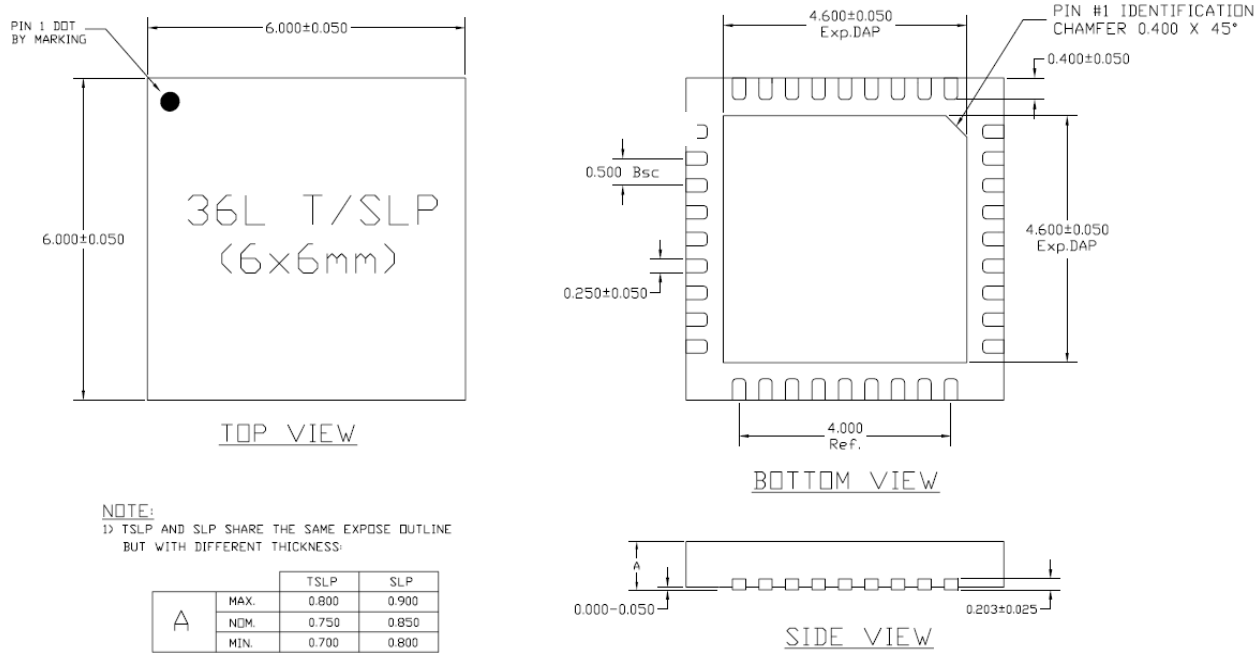
Bit	Name	Functions
D[7:5]	Res	Reserved (must be kept at the default value)
D[4:3]	XTSD[1:0]	Crystal Oscillator wake up delay selection: 00->8.65ms 01->4.35ms 10 -> 17.15ms 11->13ms. This value needs to be updated only once after power up if a delay value different than the default is needed.
D[2:0]	Res	Reserved (must be kept at the default value)

APPLICATION SCHEMATIC



Component	Value	Comment
C1	2.2µF	
C2	1µF	
C4	1µF	
C5,C6	10µF	DC-DC capacitor Maximum ESR 50mΩ
C7	10µF	
C8	10µF	Might be reduced due to the combination with C5
C9,C10	300pF	300pF for RF filtering can be increased up to 33nF dependent on the application
C11	1µF	
C12,C13	200nF	May be changed to tune the HP pole in the application.
C14,C15	2.2µF	(optional) strongly application noise and microphone configuration dependent.
R1	1.33kΩ	Battery charger current programming resistor
L1	10µH	DC-DC Inductor Maximum ESR 200mΩ
X1	26MHz	26MHz Crystal

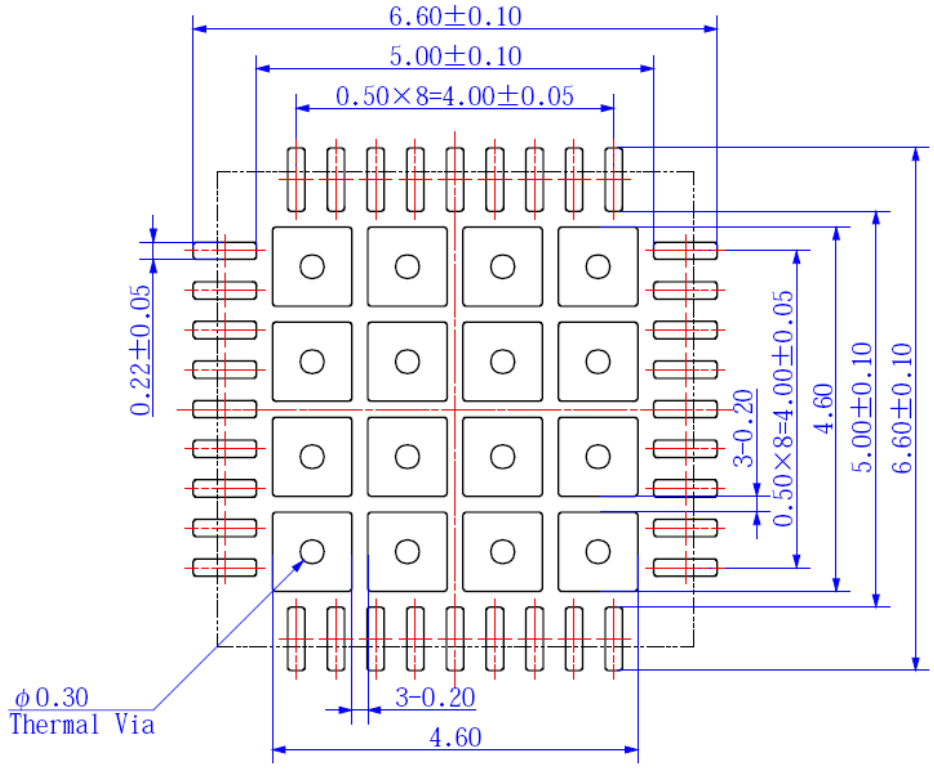
PACKAGE INFORMATION



NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS.

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

RECOMMENDED PCB FOOTPRINT



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In conformance with the EU directive on the "Restriction of the Use of Hazardous Substances in Electrical and Electronic Equipment" (RoHS, 2002/95/EC), Silicon Labs is proud to provide Pb-Free/Green packaging for our standard product customers. Consistent with the directive's requirement that electronic components not contain lead, mercury, cadmium, hexavalent chromium, poly-brominated biphenyls (PBB) or poly-brominated diphenyl ethers (PBDE), Silicon Labs now provides standard products in packages using 100% matte tin (Sn) plating, for forward compatibility with Pb-Free solders, and backwards compatibility with SnPb solders. In addition to being Pb-Free, Silicon Labs standard product packages are also Green (halogen free, Sumitomo G600 compound, Ablebond 8340A epoxy).

All Silicon Labs lead-free products have passed qualification testing (passes MSL 1 using IR reflow temperature at 260°C, with long term reliability testing). Additionally, qualification includes moisture sensitivity to J-STD-20C, and solderability to JEDEC level 1.

Per JEDEC requirement (JESD97), Silicon Labs products are shipped with Pb-Free category symbol (e3) marked on a second level interconnect label affixed to component packing, with Pb-Free label affixed to the shipping box.

Silicon Labs provides standard product customers with a banned substances report corresponding to the die/package being shipped.

Silicon Labs, Inc.
400 West Cesar Chavez
Austin, Texas 78701
Tel: 512.416.8500
Fax: 512.416.9669
Toll Free: 877.444.3032
www.silabs.com/integration
siDAAinfo@silabs.com