# ML12509
# ML12511
# ML12513

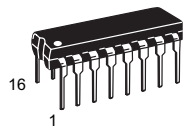
## MECL PLL Components
## Dual Modulus Prescaler

**Legacy Device:** *Motorola 12509, 12511, 12513*

These devices are two–modulus prescalers which will divide by 5 and 6, 8 and 9, respectively. A MECL–to–MTTL translator is provided to interface directly with the Motorola MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

- ML12509 480 MHz (÷5/6), ML12511 550 MHz (÷8/9), ML12513 550 MHz (÷10/11)
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- 5.0 or –5.2 V Operation*
- Buffered Clock Input — Series Input RC Typ, 20 Ω and 4.0 pF
- VBB Reference Voltage
- 310 mW (Typ)

* When using a 5.0 V supply, apply 5.0 V to Pin 1 ($V_{CCO}$), Pin 6 (MTTL $V_{CC}$), Pin 16 ($V_{CC}$), and ground Pin 8 ($V_{EE}$). When using –5.2 V supply, ground Pin 1 ($V_{CCO}$), Pin 6 (MTTL $V_{CC}$), and Pin 16 ($V_{CC}$) and apply –5.2 V to Pin 8 ($V_{EE}$). If the translator is not required, Pin 6 may be left open to conserve DC power drain.

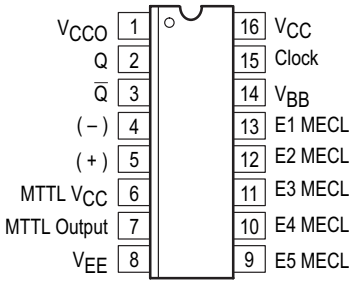



**CERDIP 16 = E**
CERAMIC PACKAGE
CASE 620

**CROSS REFERENCE/ORDERING INFORMATION**

| PACKAGE | MOTOROLA | LANSDALE |
|---|---|---|
| CERDIP 16 | 12509/BEA | ML12509/BEA |
| CERDIP 16 | 12511/BEA | ML12511/BEA |
| CERDIP 16 | 12513/BEA | ML12513/BEA |

**PIN CONNECTIONS**




(Top View)

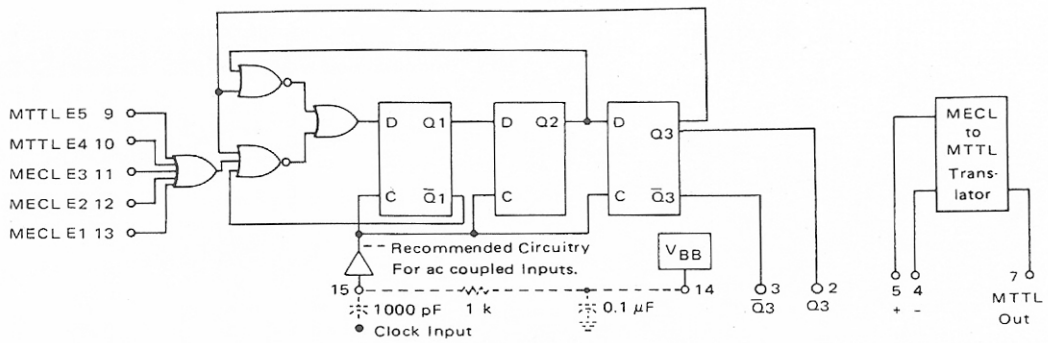
**MAXIMUM RATINGS**

| Characteristic | Symbol | Rating | Unit |
|---|---|---|---|
| (Ratings above which device life may be impaired) | | | |
| Power Supply Voltage ($V_{CC}$ = 0) | $V_{EE}$ | –8.0 | Vdc |
| Input Voltage ($V_{CC}$ = 0) | $V_{in}$ | 0 to $V_{EE}$ | Vdc |
| Output Source Current<br>Continuous<br>Surge | $I_O$ | <br>< 50<br>< 100 | mAdc |
| Storage Temperature Range | $T_{stg}$ | –65 to 175 | C |
| (Recommended Maximum Ratings above which performance may be degraded) | | | |
| Operating Temperature Range | $T_A$ | –55 to 125 | C |
| DC Fan–Out (Note 1)<br>(Gates and Flip–Flops) | n | 70 | — |

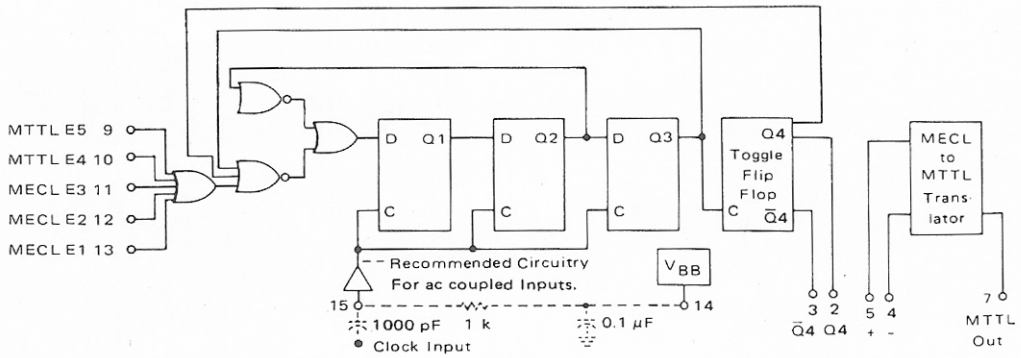
**NOTES:** 1. AC fan–out is limited by desired system performance.

FIGURE 1 – LOGIC DIAGRAMS

ML12509




ML12511




ML12513

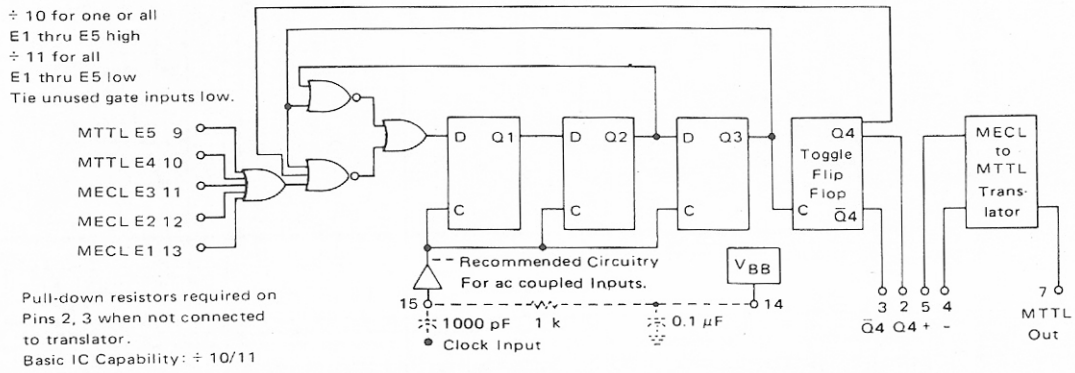
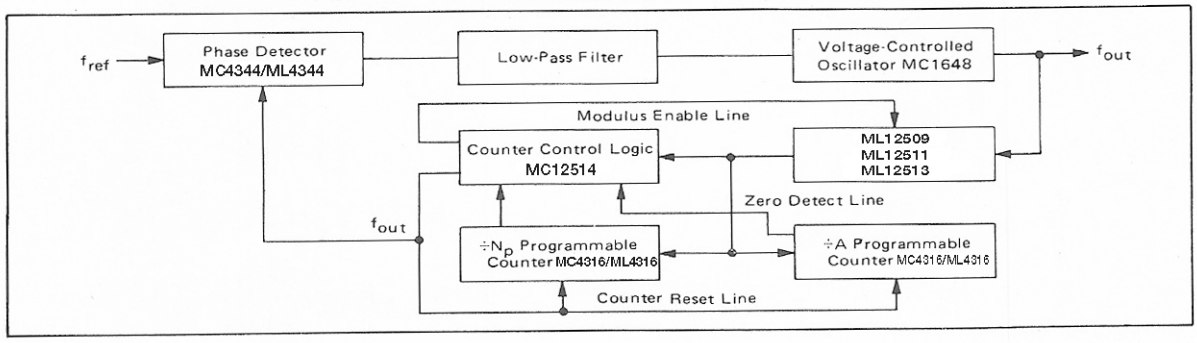



FIGURE 2 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



# ELECTRICAL CHARACTERISTICS

| Test Temperature | Test Voltage Values (Volts) | | | | | | | | | | | | | | | Test Current Values (mA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{IH}$ | $V_{IL}$ | $V_{IHA}$ | $V_{ILA}$ | $V_{IHB}$ | $V_{ILB}$ | $V_{IHT}$ | $V_{ILT}$ | $V_{EE}$ | $V_{CC}$ | $V_{IHmin}$ | $V_{ILmin}$ | $V_{ILL}$ | $V_{EEL}$ | $V_{CCA}$ | $I_L$ | $I_{OL}$ | $I_{OH}$ |
| $T_A$ = 25 °C | + 2.4 | + 0.5 | + 3.895 | + 3.525 | + 4.22 | + 3.11 | + 2.0 | + 0.8 | 0.0 | + 5.0 | + 1.15 | + 0.215 | - 3.0 | - 3.0 | + 2.0 | - 0.25 | + 16 | - 0.4 |
| $T_A$ = 125 °C | + 2.4 | + 0.5 | + 4.0 | + 3.6 | + 4.37 | + 3.14 | + 2.0 | + 0.8 | 0.0 | + 5.0 | + 1.27 | + 0.26 | - 3.0 | - 3.0 | + 2.0 | - 0.25 | + 16 | - 0.4 |
| $T_A$ = -55 °C | + 2.4 | + 0.5 | + 3.745 | + 3.5 | + 4.12 | + 3.04 | + 2.0 | + 0.8 | 0.0 | + 5.0 | + 1.02 | + 0.165 | - 3.0 | - 3.0 | + 2.0 | - 0.25 | + 16 | - 0.4 |

| Symbol | Parameter | Limits | | | | | | Units | TEST VOLTAGE APPLIED TO PINS BELOW | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Functional Parameters: | + 25 °C | | + 125 °C | | - 55 °C | | | Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 3.0 V | | | | | | | | | |
| | | Subgroup 1 | | Subgroup 2 | | Subgroup 3 | | | | | | | | | | | | |
| | | Min | Max | Min | Max | Min | Max | | $V_{IH}$ | $V_{IL}$ | $V_{IHA/B}$ | $V_{ILA/B}$ | $V_{CC}$ | $V_{EE}$ | $C_{P1}$ | $I_{OH/OL}$ | $I_L$ | P.U.T. |
| $V_{OH1}$ | Output Voltage High | 4.03 | 4.22 | 4.135 | 4.37 | 3.88 | 4.12 | V | 9, 10 | 9, 10 | 11 - 13 | 11 - 13 | 1, 16 | 8 | 15 | | | 2, 3 (Note 2) |
| $V_{OH2}$ | Output Voltage High | 2.70 | 4.5 | 3.00 | 4.5 | 2.40 | 4.5 | V | | | 5 | 4 | 6 | 8 | | 7 $I_{OH}$ | | 7 |
| $V_{OL1}$ | Output Voltage Low | 3.11 | 3.44 | 3.14 | 3.515 | 3.04 | 3.405 | V | 9, 10 | 9, 10 | 11 - 13 | 11 - 13 | 1, 16 | 8 | 15 | | | 2, 3 (Note 2) |
| $V_{OL2}$ | Output Voltage Low | 0.10 | 0.80 | 0.10 | 0.66 | 0.10 | 1.00 | V | | | 4 | 5 | 6 | 8 | | 7 $I_{OL}$ | | 7 |
| $V_{OHA}$ | Output Voltage High | 4.01 | 4.5 | 4.115 | 4.5 | 3.86 | 4.5 | V | | 9, 10 | 11 - 13 | 11 - 13 | 1, 16 | 8 | 15 | | | 2, 3 (Note 3) |
| $V_{OLA}$ | Output Voltage Low | 3.11 | 3.46 | 3.14 | 3.535 | 3.04 | 3.425 | V | | 9, 10 | 11 - 13 | 11 - 13 | 1, 16 | 8 | 15 | | | 2, 3 (Note 3) |
| $V_{BB1}$ | Reference Bias Supply Voltage | 3.67 | 3.87 | | | | | V | | | | | 1, 16 | 8 | | | 14 | 14 |
| $I_{OS}$ | Output Short Circuit Current | - 65 | - 20 | - 65 | - 20 | - 65 | - 20 | mA | | 7 | 5 | 4 | 6 | 8 | | | | 7 |
| $I_{CC1}$ | Power Supply Current | - 80 | | - 80 | | - 88 | | mA | | | | | 1, 16 | 8 | | | | 8 |
| $I_{CC2}$ | Power Supply Current | | 5.2 | | 5.2 | | 5.2 | mA | | | 4 | 5 | 6 | 8 | | | | 6 |

1. Power Supply Voltage = 5.0 V, Power Supply Voltage = - 5.2 V is guaranteed but not tested.
2. See Sequence Table 1.
3. See Sequence Table 2.

## ELECTRICAL CHARACTERISTICS

| Test Temperature | Test Voltage Values (Volts) | | | | | | | | | | | | | | | Test Current Values (mA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{IH}$ | $V_{IL}$ | $V_{IHA}$ | $V_{ILA}$ | $V_{IHB}$ | $V_{ILB}$ | $V_{IHT}$ | $V_{ILT}$ | $V_{EE}$ | $V_{CC}$ | $V_{IHmin}$ | $V_{ILmin}$ | $V_{ILL}$ | $V_{EEL}$ | $V_{CCA}$ | $I_L$ | $I_{OL}$ | $I_{OH}$ |
| $T_A$ = 25 °C | + 2.4 | + 0.5 | + 3.895 | + 3.525 | + 4.22 | + 3.11 | + 2.0 | + 0.8 | 0.0 | + 5.0 | + 1.15 | + 0.215 | - 3.0 | - 3.0 | + 2.0 | - 0.25 | + 16 | - 0.4 |
| $T_A$ = 125 °C | + 2.4 | + 0.5 | + 4.0 | + 3.6 | + 4.37 | + 3.14 | + 2.0 | + 0.8 | 0.0 | + 5.0 | + 1.27 | + 0.26 | - 3.0 | - 3.0 | + 2.0 | - 0.25 | + 16 | - 0.4 |
| $T_A$ = -55 °C | + 2.4 | + 0.5 | + 3.745 | + 3.5 | + 4.12 | + 3.04 | + 2.0 | + 0.8 | 0.0 | + 5.0 | + 1.02 | + 0.165 | - 3.0 | - 3.0 | + 2.0 | - 0.25 | + 16 | - 0.4 |

| Symbol | Parameter | Limits | | | | | | Units | TEST VOLTAGE APPLIED TO PINS BELOW | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Functional Parameters: | + 25 °C Subgroup 1 | | + 125 °C Subgroup 2 | | - 55 °C Subgroup 3 | | | Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 3.0 V | | | | | | |
| | | Min | Max | Min | Max | Min | Max | | $V_{IH}$ | $V_{IL}$ | $V_{IHA/B}$ | $V_{ILA/B}$ | $V_{CC}$ | $V_{EE}$ | P.U.T. |
| $I_{INH1}$ | Input Current High | | 250 | | 400 | | 400 | µA | | 9, 10 | 11 - 13, 15 | | 1, 16 | 8 | 11, 12, 13, 15 |
| $I_{INH2}$ | Input Current High | 2.0 | 6.0 | 2.0 | 6.4 | 1.7 | 6.0 | mA | | | 4, 5 | 4, 5 | 6 | 8 | 4, 5 |
| $I_{INH3}$ | Input Current High | 1.0 | 3.0 | 1.0 | 3.6 | 0.7 | 3.0 | mA | | | 4 | 5 | 6 | 8 | 5 |
| $I_{INH4}$ | Input Current High | | 100 | | 100 | | 100 | µA | 9, 10 | | | | 1, 16 | 8 | 9, 10 |
| $I_{INI1}$ | Input Current Low | - 10 | | - 10 | | - 10 | | µA | | | | | 1, 16 | 8, 15, 11 - 13 | 11, 12, 13, 15 |
| $I_{INI1}$ | Input Current Low | - 1.6 | | - 1.6 | | - 1.6 | | mA | | 9, 10 | | | 1, 16 | 8 | 9, 10 |

1. Power Supply Voltage = 5.0 V, Power Supply Voltage = - 5.2 V is guaranteed but not tested.

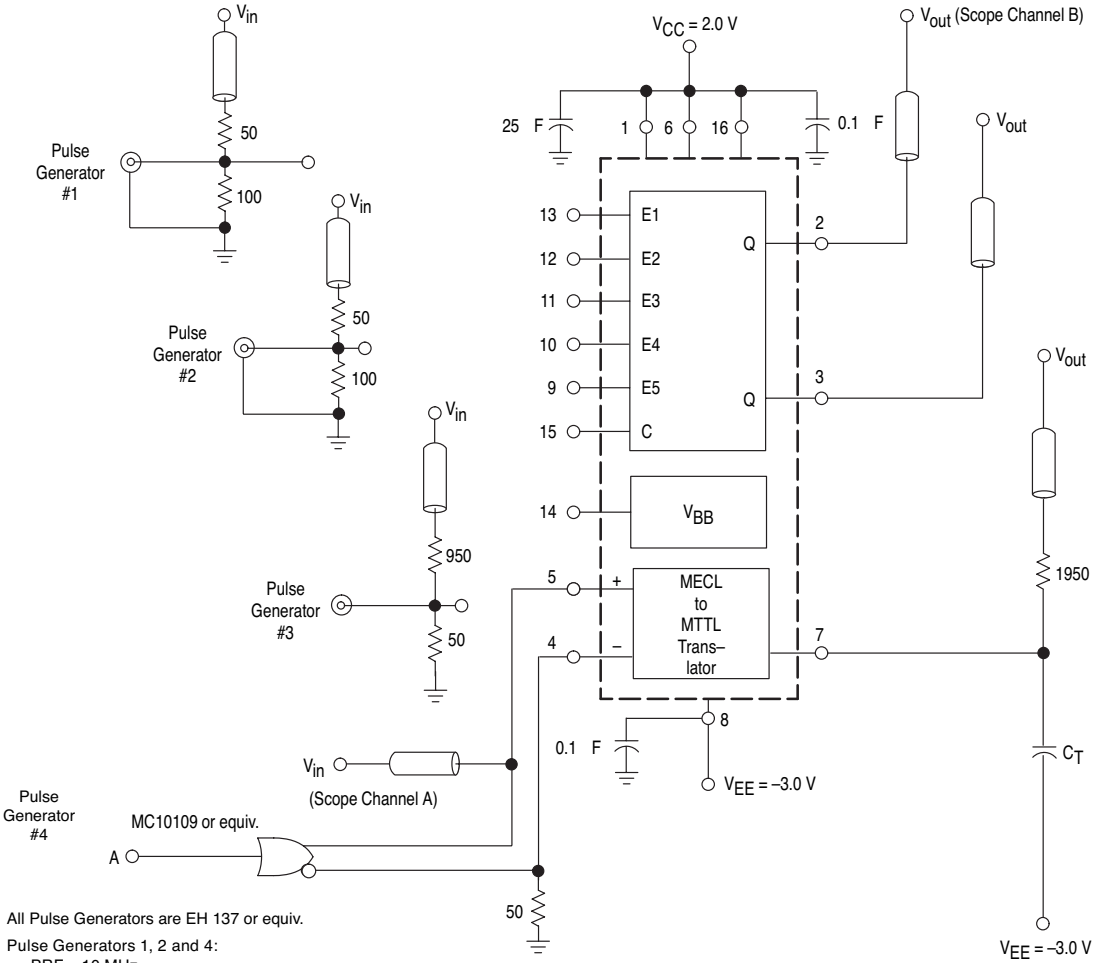
* **ELECTRICAL CHARACTERISTICS:** This device is designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100 Ω resistor to + 3.0 V.

| Test Temperature | Test Voltage Values (Volts) | | | | | | | | | | | | | | | Test Current Values (mA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{IH}$ | $V_{IL}$ | $V_{IHA}$ | $V_{ILA}$ | $V_{IHB}$ | $V_{ILB}$ | $V_{IHT}$ | $V_{ILT}$ | $V_{EE}$ | $V_{CC}$ | $V_{IHmin}$ | $V_{ILmin}$ | $V_{ILL}$ | $V_{EEL}$ | $V_{CCA}$ | $I_L$ | $I_{OL}$ | $I_{OH}$ |
| $T_A$ = 25 °C | + 2.4 | + 0.5 | + 3.895 | + 3.525 | + 4.22 | + 3.11 | + 2.0 | + 0.8 | 0.0 | + 5.0 | + 1.15 | + 0.215 | - 3.0 | - 3.0 | + 2.0 | - 0.25 | + 16 | - 0.4 |
| $T_A$ = 125 °C | + 2.4 | + 0.5 | + 4.0 | + 3.6 | + 4.37 | + 3.14 | + 2.0 | + 0.8 | 0.0 | + 5.0 | + 1.27 | + 0.26 | - 3.0 | - 3.0 | + 2.0 | - 0.25 | + 16 | - 0.4 |
| $T_A$ = -55 °C | + 2.4 | + 0.5 | + 3.745 | + 3.5 | + 4.12 | + 3.04 | + 2.0 | + 0.8 | 0.0 | + 5.0 | + 1.02 | + 0.165 | - 3.0 | - 3.0 | + 2.0 | - 0.25 | + 16 | - 0.4 |

## SWITCHING CHARACTERISTICS

| Symbol | Parameter | Limits | | | | | | Units | TEST VOLTAGE APPLIED TO PINS BELOW | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Functional Parameters: (Fig. 5) | + 25 °C Subgroup 9 | | + 125 °C Subgroup 10 | | - 55 °C Subgroup 11 | | | Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 3.0 V | | | | | | |
| | | Min | Max | Min | Max | Min | Max | | $V_{ILL}$ | $V_{ILmin}$ | $V_{IN}$ | $V_{OUT}$ | $V_{CCA}$ | $V_{EEL}$ | P.U.T. |
| $t_{PHH}$ | Propagation Delay (15+ 2+) | | 8.1 | | 9.4 | | 8.1 | ns | 9, 10 | 11 - 13 | 15 | 2, 3 | 1, 6, 16 | 8 | 2, 3 |
| $t_{PHH}$ | Propagation Delay (5+ 7+) | | 8.1 | | 9.4 | | 8.1 | ns | 9, 10 | 11 - 13 | 15 | 2, 3 | 1, 6, 16 | 8 | 2, 3 |
| $t_{PLL}$ | Propagation Delay (15+ 2-) | | 7.5 | | 8.7 | | 7.5 | ns | 9, 10 | 11 - 13 | 15 | 2, 3 | 1, 6, 16 | 8 | 7 |
| $t_{PLL}$ | Propagation Delay (5- 7-) | | 6.5 | | 7.6 | | 6.5 | ns | 9, 10 | 11 - 13 | 15 | 2, 3 | 1, 6, 16 | 8 | 7 |
| | | Min | Typ | Min | Max | Min | Max | | $V_{ILL}$ | $V_{ILmin}$ | $V_{IN}$ | $V_{OUT}$ | $V_{CCA}$ | $V_{EEL}$ | P.U.T. |
| $t_{Setup\ 1}$ | Setup Time MECL | 5.0 | | 5.0 | | 5.0 | | ns | 9, 10 | 11 - 13 | 9 - 13 | | 1, 6, 16 | 8 | 9 - 13 |
| $t_{Setup\ 2}$ | Setup Time MTTL | 5.0 | | 5.0 | | 5.0 | | ns | 9, 10 | 11 - 13 | 9 - 13 | | 1, 6, 16 | 8 | 9 - 13 |
| $t_{Rel\ 1}$ | Release Time MECL | 5.0 | | 5.0 | | 5.0 | | ns | 9, 10 | 11 - 13 | 9 - 13 | | 1, 6, 16 | 8 | 9 - 13 |
| $t_{Rel\ 2}$ | Release Time MTTL | 5.0 | | 5.0 | | 5.0 | | ns | 9, 10 | 11 - 13 | 9 - 13 | | 1, 6, 16 | 8 | 9 - 13 |
| | | Min | Typ | Min | Typ | Min | Typ | | $V_{ILL}$ | $V_{ILmin}$ | $V_{IN}$ | $V_{OUT}$ | $V_{CCA}$ | $V_{EEL}$ | P.U.T. |
| $f_{max}$ ÷5/6 | (Fig. 6) Toggle Frequency ML12509 | 480 | 520 | 420 | 440 | 420 | 500 | MHz | | | 15 | 2 | 1, 6, 16 | 8 - 13 | 2 |
| ÷8/9 | ML12511 | 500 | 550 | 500 | 550 | 500 | 550 | MHz | | | 15 | 2 | 1, 6, 16 | 8 - 13 | 2 |
| ÷10/11 | ML12513 | 550 | 600 | 500 | 540 | 500 | 600 | MHz | | | 15 | 2 | 1, 6, 16 | 8 - 13 | 2 |

**Figure 5. AC Test Circuit**



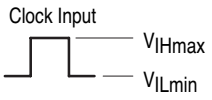

All Pulse Generators are EH 137 or equiv.

Pulse Generators 1, 2 and 4:
PRF = 10 MHz
PW = 50% Duty Cycle
t+ = t– = 2.0 ± 0.2 ns

Pulse Generator 3:
PRF = 2.0 MHz
PW = 50% Duty Cycle
t+ = t– = 5.0 ± 0.5 ns

All resistors are +1%.
All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
The 1950 Ω resistor at Pin 7 and the scope termination impedance constitute a 40 :1 attenuator probe.
$C_T$ = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.
Unused output connected to a 50 Ω resistor to ground.

**NOTES:** 1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
2. In addition to meeting the output levels specified, the device must divide by 5 or 8 during this test. The clock input is the waveform shown.
3. In addition to meeting the output levels specified, the device must divide by 6 or 9 during this test. The clock input is the waveform shown.




Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to –2.0 V. Test procedures are shown for only one gate. The other gates are tested in the same manner.

**Figure 3. AC Voltage Waveforms**

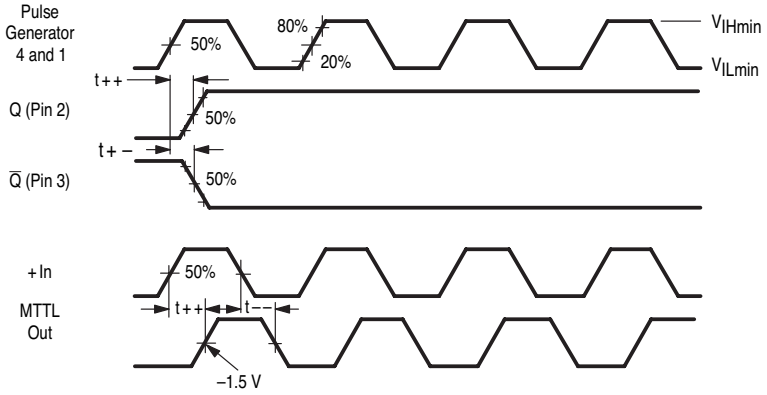
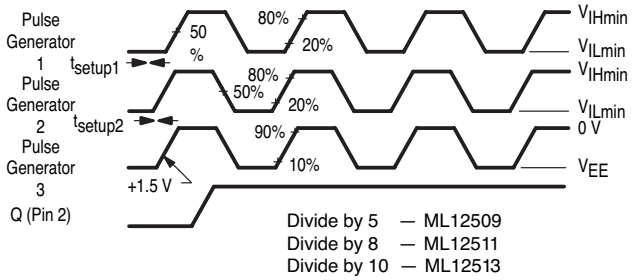



**Figure 4. Setup and Release Time Waveforms**



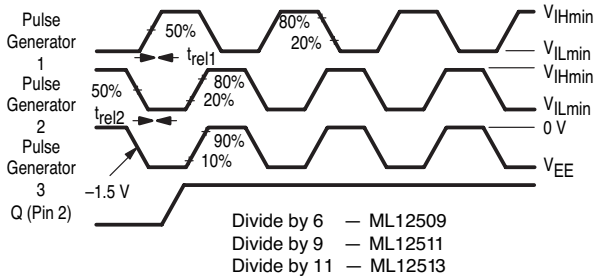
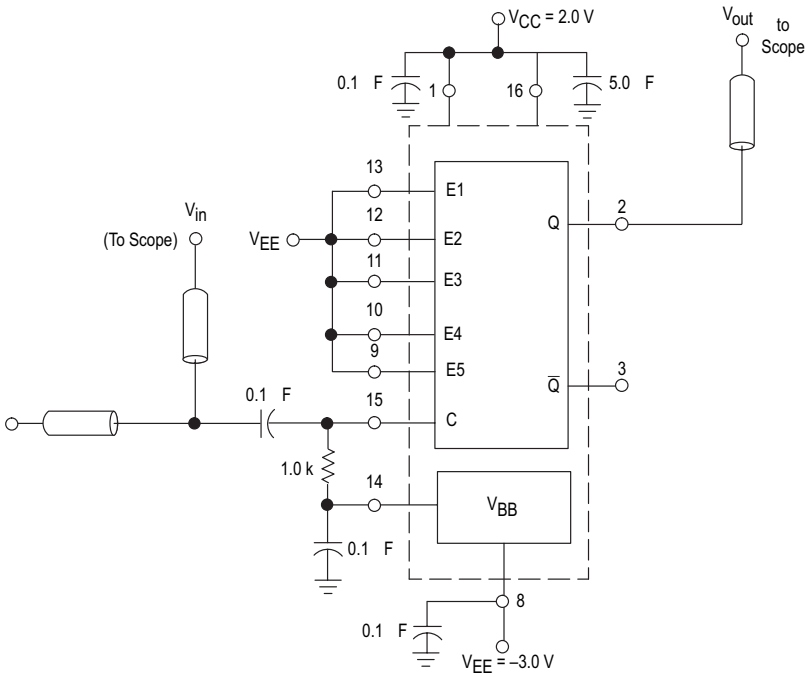
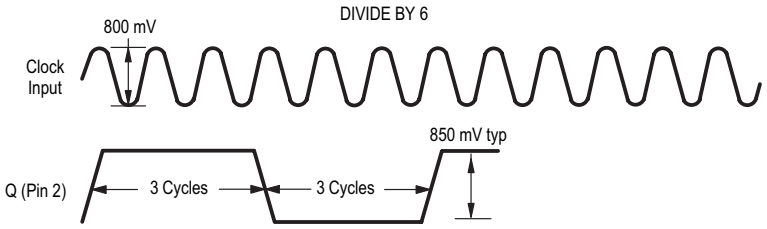



**Figure 6. Maximum Frequency Test Circuit**




Unused output connected to a 50 Ω resistor to ground



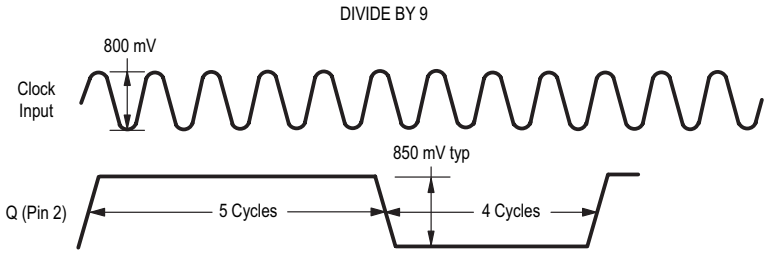



FIGURE 7 – STATE DIAGRAM

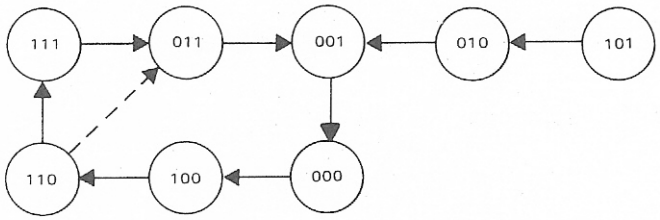
DIVIDE BY 5/6 (ML12509)

| Q1 | Q2 | Q3 |
|---|---|---|
| 1 | 1 | 1 |
| 0 | 1 | 1 |
| 0 | 0 | 1 |
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Enable = 0

Enable = 1

— — — Enable = 1



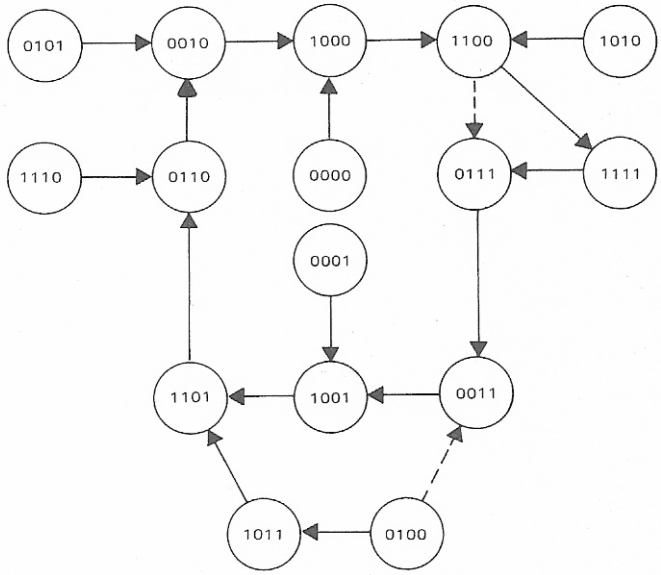

DIVIDE BY 8/9 (ML12511)

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |

Enable = 0

Enable = 1

— — — Enable = 1




DIVIDE BY 10/11 (ML12513)

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |

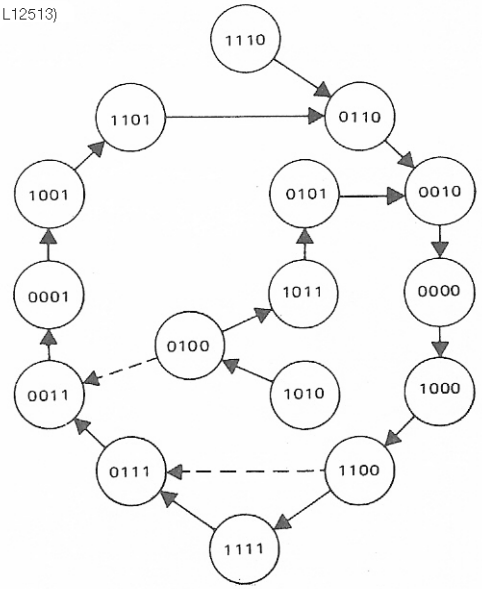
Enable = 0

Enable = 1

NOTES:

— — — Enable = 1.

The State of the Enable is important only for the positive Clock Transition when the counter is in state 1100.



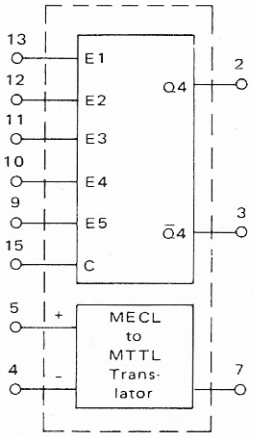
## APPLICATIONS INFORMATION

The primary application of these devices is as a high-speed variable modulus prescaler in the divide by N section of a phase-locked loop synthesizer used as the local oscillator of two-way radios. The theory and advantages of variable modulus prescaling, along with typical applications, are covered in Motorola's "Electronic Tuning Address Systems" (SG72).

Proper VHF termination techniques should be followed when the clock is separated from the prescaler by any appreciable distance.

In their basic form, these devices will divide by 5/6, 8/9, or 10/11. Division by 5, 8, or 10 occurs when any one or all of the five gate inputs E1 through E5 are high. Division by 6, 9, or 11 occurs when all inputs E1 through E5 are low. (Unconnected MTTL inputs are normally high, unconnected MECL inputs are normally low). With the addition of extra parts, many different division configurations may be obtained (20/21, 40/41, 50/51, 100/101, etc.) A few of the many configurations are shown below, only for the ML12513

**FIGURE 8 — DIVIDE BY 10/11 (ML12513)**

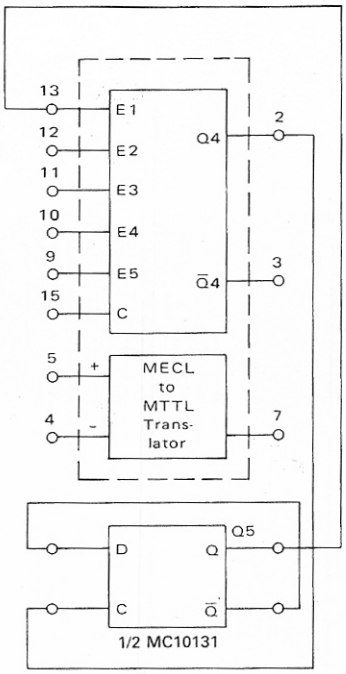



| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |

Enable = 0

Enable = 1

**FIGURE 9 — DIVIDE BY 20/21 (ML12513)**




| COUNT | Q1 | Q2 | Q3 | Q4 | Q4 |
|---|---|---|---|---|---|
| 31 | 1 | 1 | 1 | 1 | 1 |
| 30 | 0 | 1 | 1 | 1 | 1 |
| 28 | 0 | 0 | 1 | 1 | 1 |
| 24 | 0 | 0 | 0 | 1 | 1 |
| 25 | 1 | 0 | 0 | 1 | 1 |
| 27 | 1 | 1 | 0 | 1 | 1 |
| 22 | 0 | 1 | 1 | 0 | 1 |
| 20 | 0 | 0 | 1 | 0 | 1 |
| 16 | 0 | 0 | 0 | 0 | 1 |
| 17 | 1 | 0 | 0 | 0 | 1 |
| 19 | 1 | 1 | 0 | 0 | 1 |
| 14 | 0 | 1 | 1 | 1 | 0 |
| 12 | 0 | 0 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 |
| 11 | 1 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 | 0 |

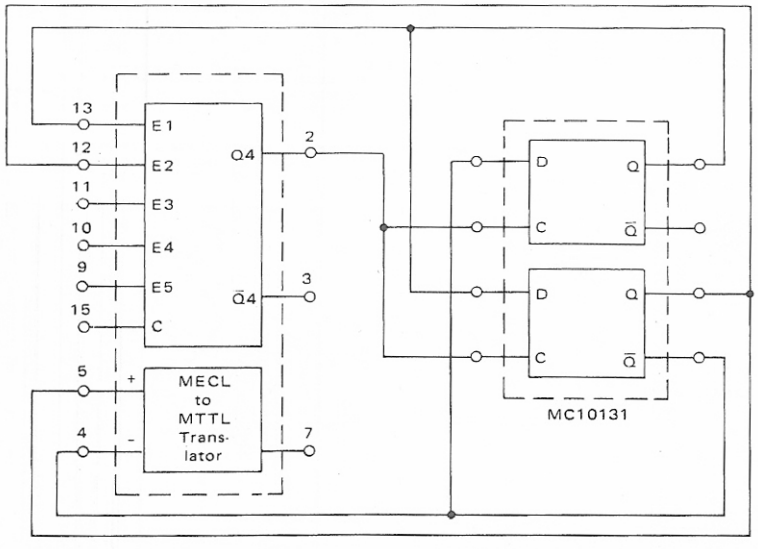
E2 + E3 + E4 + E5 = 0

E2 + E3 + E4 + E5 = 1

To obtain an MTTL output, connect Pins 5 and 4 to Pins 2 and 3 respectively. Termination resistors for the MECL outputs are not shown, but are required except for the flip-flop driving the translator section.

The ÷ 20/21 counter may also be built using an MTTL flip-flop by connecting Pins 5 and 4 to Pins 2 and 3 respectively, and driving the MTTL flip-flop with Pin 7. ML12513 inputs E4 and E5 are used rather than E1. With E1 + E2 + E3 = 0, operation remains as shown.

**FIGURE 10 — DIVIDE BY 40/41 (ML12513)**

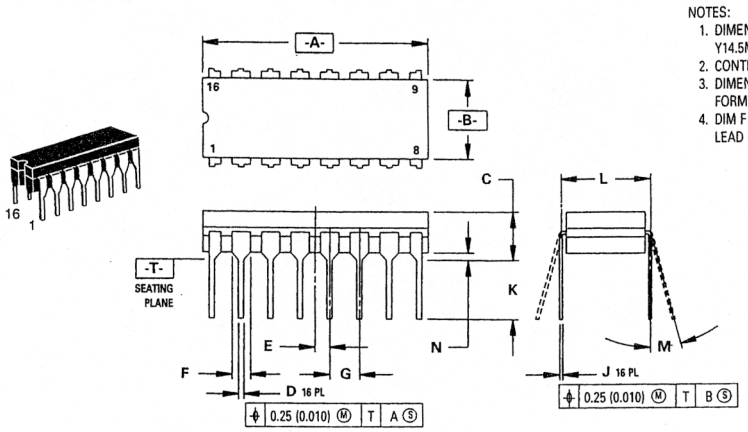



For ÷40: E4 + E5 = 1
For ÷41: E4 +E5 = 0

Termination resistors for MECL outputs are not shown, but are required except for the flip-flop driving the translator section.

## OUTLINE DIMENSIONS

CERDIP 16 = E
CERAMIC PACKAGE
(ML12509/BEA, ML12511/BEA, ML12513/BEA)
CASE 620




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 19.05 | 19.93 | 0.750 | 0.785 |
| B | 6.10 | 7.49 | 0.240 | 0.295 |
| C | — | 5.08 | — | 0.200 |
| D | 0.39 | 0.50 | 0.015 | 0.020 |
| E | 1.27 BSC | | 0.050 BSC | |
| F | 1.40 | 1.65 | 0.055 | 0.065 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.21 | 0.38 | 0.008 | 0.015 |
| K | 3.18 | 4.31 | 0.125 | 0.170 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.01 | 0.020 | 0.040 |