

Legacy Device: *Motorola MC12009, MC12011*

These devices are two-modulus prescalers which will divide by 5 and 6, 8 and 9, respectively. A MECL-to-MTTL translator is provided to interface directly with the Motorola MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

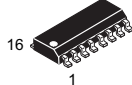
- ML12009 480 MHz ($\div 5/6$), ML12011 550 MHz ($\div 8/9$)
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- 5.0 or -5.2 V Operation*
- Buffered Clock Input — Series Input RC Typ, 20 Ω and 4.0 pF
- VBB Reference Voltage
- 310 mW (Typ)

* When using a 5.0 V supply, apply 5.0 V to Pin 1 (VCCO), Pin 6 (MTTL VCC), Pin 16 (VCC), and ground Pin 8 (VEE). When using -5.2 V supply, ground Pin 1 (VCCO), Pin 6 (MTTL VCC), and Pin 16 (VCC) and apply -5.2 V to Pin 8 (VEE). If the translator is not required, Pin 6 may be left open to conserve DC power drain.

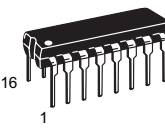
MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
(Ratings above which device life may be impaired)			
Power Supply Voltage (VCC = 0)	V _{EE}	-8.0	Vdc
Input Voltage (VCC = 0)	V _{in}	0 to V _{EE}	Vdc
Output Source Current Continuous Surge	I _O	< 50 < 100	mAdc
Storage Temperature Range	T _{stg}	-65 to 175	°C
(Recommended Maximum Ratings above which performance may be degraded)			
Operating Temperature Range ML12009, ML12011	T _A	-30 to 85	°C
DC Fan-Out (Note 1) (Gates and Flip-Flops)	n	70	—

NOTES: 1. AC fan-out is limited by desired system performance.



SO 16 = -5P
PLASTIC PACKAGE
CASE 751B



P DIP 16 = EP
PLASTIC PACKAGE
CASE 648

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 16	MC12009P	ML12009EP
SOIC 16	MC12009D	ML12009-5P
P DIP 16	MC12011P	ML12011EP
SO 16W	MC12011D	ML12011-5P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

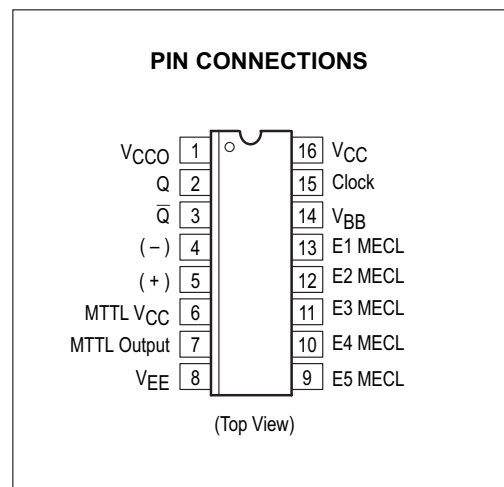


Figure 1. Logic Diagrams

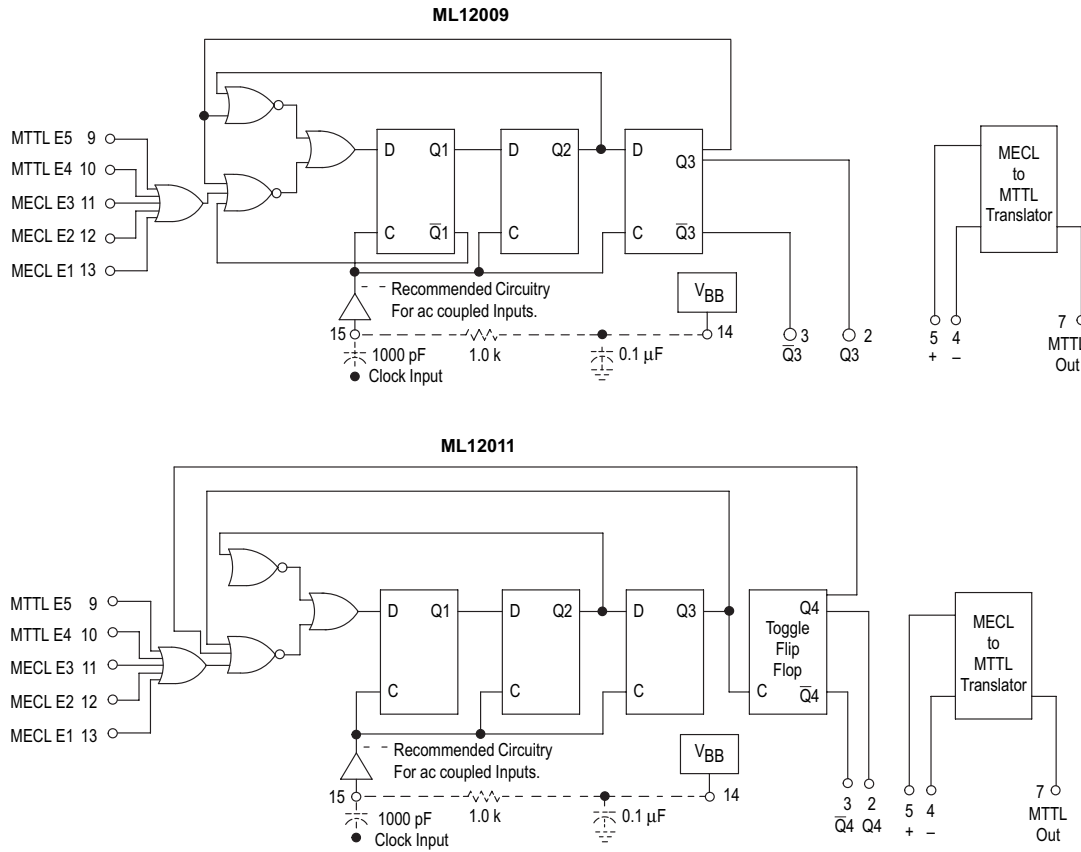


Figure 2. Typical Frequency Synthesizer Application

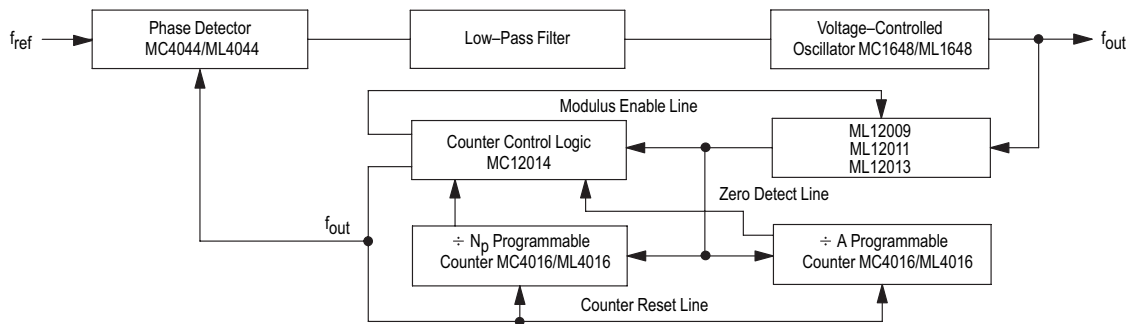


Figure 2b Generic block diagram showing prescaler connection to PLL Device

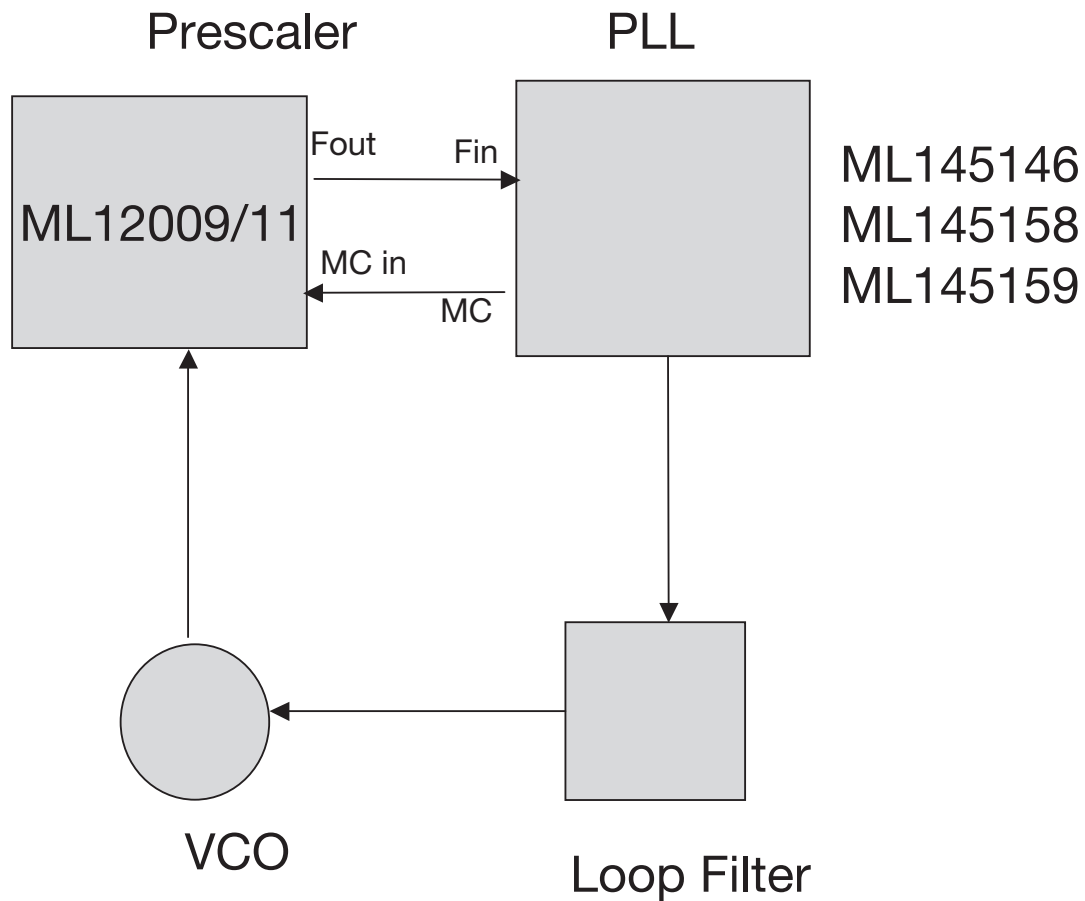
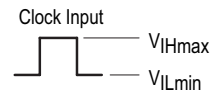


Figure 2b shows a generic block diagram of connecting a prescaler to a PLL device that supports dual modulus controls. Application note AN535 describes using a two-modulus prescaler technique. By using prescaler higher frequencies can be achieved than by a single CMOS PLL device.

ELECTRICAL CHARACTERISTICS (Supply Voltage = -5.2 V, unless otherwise noted.)

Characteristic	Symbol	Pin Under Test	Test Limits						Unit
			-30°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _{CC1}	8	-88		-80		-80		mAdc
	I _{CC2}	6		5.2		5.2		5.2	mAdc
Input Current	I _{inH1}	15		375		250		250	μAdc
		11		375		250		250	
		12		375		250		250	
		13		375		250		250	
	I _{inH2}	4	1.7	6.0	2.0	6.0	2.0	6.4	mAdc
		5	1.7	6.0	2.0	6.0	2.0	6.4	
	I _{inH3}	5	0.7	3.0	1.0	3.0	1.0	3.6	
	I _{inH4}	9		100		100		100	μAdc
10			100		100		100		
Leakage Current	I _{inL1}	15	-10		-10		-10		μAdc
		11	-10		-10		-10		
		12	-10		-10		-10		
		13	-10		-10		-10		
	I _{inL2}	9	-1.6		-1.6		-1.6		mAdc
		10	-1.6		-1.6		-1.6		
Reference Voltage	V _{BB}	14			-1.360	-1.160			Vdc
Logic '1' Output Voltage	V _{OH1} (Note 1)	2	-1.100	-0.890	-1.000	-0.810	-0.930	-0.700	Vdc
		3	-1.100	-0.890	-1.000	-0.810	-0.930	-0.700	
	V _{OH2}	7	-2.8		-2.6		-2.4		
Logic '0' Output Voltage	V _{OL1} (Note 1)	2	-1.990	-1.675	-1.950	-1.650	-1.925	-1.615	Vdc
		3	-1.990	-1.675	-1.950	-1.650	-1.925	-1.615	
	V _{OL2}	7		-4.26		-4.40		-4.48	
Logic '1' Threshold Voltage	V _{OHA} (Note 2)	2	-1.120		-1.020		-0.950		Vdc
		3	-1.120		-1.020		-0.950		
Logic '0' Threshold Voltage	V _{OLA} (Note 3)	2		-1.655		-1.630		-1.595	Vdc
		3		-1.655		-1.630		-1.595	
Short Circuit Current	I _{OS}	7	-65	-20	-65	-20	-65	-20	mAdc

- NOTES:** 1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
 2. In addition to meeting the output levels specified, the device must divide by 5 or 8 during this test. The clock input is the waveform shown.
 3. In addition to meeting the output levels specified, the device must divide by 6 or 9 during this test. The clock input is the waveform shown.

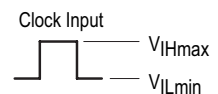


Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V. Test procedures are shown for only one gate. The other gates are tested in the same manner.

ELECTRICAL CHARACTERISTICS (continued) (Supply Voltage = -5.2 V, unless otherwise noted.)

			TEST VOLTAGE/CURRENT VALUES						Gnd	
			Volts							
			V_{IHmax}	V_{ILmin}	V_{IHmin}	V_{ILmax}	V_{IH}	V_{ILH}		
			@ Test Temperature							
			-30°C	-0.890	-1.990	-1.205	-1.500	-2.8	-4.7	
			25°C	-0.810	-1.950	-1.105	-1.475	-2.8	-4.7	
			85°C	-0.700	-1.925	-1.035	-1.440	-2.8	-4.7	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						Gnd	
			V_{IHmax}	V_{ILmin}	V_{IHmin}	V_{ILmax}	V_{IH}	V_{IL}		
Power Supply Drain Current	I_{CC1}	8							1,16	
	I_{CC2}	6	4	5					6	
Input Current	I_{inH1}	15	15						1,16	
		11	11						1,16	
		12	12						1,16	
		13	13						1,16	
	I_{inH2}	4	5	4					6	
		5	5	4					6	
	I_{inH3}	5	4	5					6	
I_{inH4}	9					9		1,16		
	10					10		1,16		
Leakage Current	I_{inL1}	15							1,16	
		11							1,16	
		12							1,16	
		13							1,16	
	I_{inL2}	9						9	1,16	
10							10	1,16		
Reference Voltage	V_{BB}	14							1,16	
Logic '1' Output Voltage	V_{OH1} (Note 1)	2		11,12,13				9,10	1,16	
		3		11,12,13				9,10	1,16	
Logic '0' Output Voltage	V_{OL1} (Note 1)	2		11,12,13				9,10	1,16	
		3		11,12,13				9,10	1,16	
Logic '1' Threshold Voltage	V_{OHA} (Note 2)	2			11,12,13				1,16	
		3			11,12,13				1,16	
Logic '0' Threshold Voltage	V_{OLA} (Note 3)	2				11,12,13			1,16	
		3				11,12,13			1,16	
Short Circuit Current	I_{OS}	7	5	4				7	6	

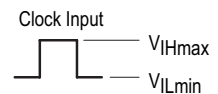
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 2. In addition to meeting the output levels specified, the device must divide by 5 or 8 during this test. The clock input is the waveform shown.
 3. In addition to meeting the output levels specified, the device must divide by 6 or 9 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS (continued) (Supply Voltage = -5.2 V, unless otherwise noted.)

			TEST VOLTAGE/CURRENT VALUES						Gnd	
			Volts			mA				
			V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}		
			@ Test Temperature							
			-30°C	-3.2	-4.4	-5.2	-0.25	16	-0.40	
			25°C	-3.2	-4.4	-5.2	-0.25	16	-0.40	
			85°C	-3.2	-4.4	-5.2	-0.25	16	-0.40	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						Gnd	
			V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}		
Power Supply Drain Current	I_{CC1}	8			8				1,16	
	I_{CC2}	6			8				6	
Input Current	I_{inH1}	15			8				1,16	
		11	9,10		8				1,16	
		12	9,10		8				1,16	
		13	9,10		8				1,16	
	I_{inH2}	4			8				6	
		5			8				6	
	I_{inH3}	5			8				6	
	I_{inH4}	9			8				1,16	
10				8				1,16		
Leakage Current	I_{inL1}	15			8,15				1,16	
		11			8,11				1,16	
		12			8,12				1,16	
		13			8,13				1,16	
	I_{inL2}	9			8				1,16	
		10			8				1,16	
Reference Voltage	V_{BB}	14			8	14			1,16	
Logic '1' Output Voltage	V_{OH1} (Note 1)	2			8				1,16	
		3			8				1,16	
V_{OH2}	7			8			7	6		
Logic '0' Output Voltage	V_{OL1} (Note 1)	2			8				1,16	
		3			8				1,16	
	V_{OL2}	7			8		7		6	
Logic '1' Threshold Voltage	V_{OHA} (Note 2)	2	9,10		8				1,16	
		3	9,10		8				1,16	
Logic '0' Threshold Voltage	V_{OLA} (Note 2)	2		9,10	8				1,16	
		3		9,10	8				1,16	
Short Circuit Current	I_{OS}	7			8				6	

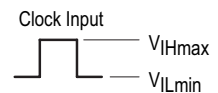
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 3. In addition to meeting the output levels specified, the device must divide by 6 or 9 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS (Supply Voltage = 5.0 V, unless otherwise noted.)

Characteristic	Symbol	Pin Under Test	Test Limits						Unit
			-30°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _{CC1}	8	-88		-80		-80		mAdc
	I _{CC2}	6		5.2		5.2		5.2	mAdc
Input Current	I _{inH1}	15		375		250		250	μAdc
		11		375		250		250	
		12		375		250		250	
		13		375		250		250	
	I _{inH2}	4	1.7	6.0	2.0	6.0	2.0	6.4	mAdc
		5	1.7	6.0	2.0	6.0	2.0	6.4	
	I _{inH3}	5	0.7	3.0	1.0	3.0	1.0	3.6	
	I _{inH4}	9			100	100		100	μAdc
10				100	100		100		
Leakage Current	I _{inL1}	15	-10		-10		-10		μAdc
		11	-10		-10		-10		
		12	-10		-10		-10		
		13	-10		-10		-10		
	I _{inL2}	9	-1.6		-1.6		-1.6		mAdc
		10	-1.6		-1.6		-1.6		
Reference Voltage	V _{BB}	14			3.67	3.87		Vdc	
Logic '1' Output Voltage	V _{OH1} (Note 1)	2	3.900	4.110	4.000	4.190	4.070	4.300	Vdc
		3	3.900	4.110	4.000	4.190	4.070	4.300	
	V _{OH2}	7	2.4		2.6		2.8		
Logic '0' Output Voltage	V _{OL1} (Note 1)	2	3.070	3.385	3.110	3.410	3.135	3.445	Vdc
		3	3.070	3.385	3.110	3.410	3.135	3.445	
	V _{OL2}	7		0.94		0.80		0.72	
Logic '1' Threshold Voltage	V _{OHA} (Note 2)	2	3.880		3.980		4.050		Vdc
		3	3.880		3.980		4.050		
Logic '0' Threshold Voltage	V _{OLA} (Note 3)	2		3.405		3.430		3.465	Vdc
		3		3.405		3.430		3.465	
Short Circuit Current	I _{OS}	7	-65	-20	-65	-20	-65	-20	mAdc

- NOTES:** 1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
 2. In addition to meeting the output levels specified, the device must divide by 5 or 8 during this test. The clock input is the waveform shown.
 3. In addition to meeting the output levels specified, the device must divide by 6 or 9 during this test. The clock input is the waveform shown.

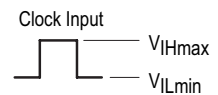


Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V. Test procedures are shown for only one gate. The other gates are tested in the same manner.

ELECTRICAL CHARACTERISTICS (continued) (Supply Voltage = 5.0 V, unless otherwise noted.)

			TEST VOLTAGE/CURRENT VALUES							
			Volts							
			V_{IHmax}	V_{ILmin}	V_{IHmin}	V_{ILmax}	V_{IH}	V_{ILH}		
			@ Test Temperature							
			-30°C	4.110	3.070	3.795	3.500	2.4	0.5	
			25°C	4.190	3.110	3.895	3.525	2.4	0.5	
			85°C	4.300	3.135	3.965	3.560	2.4	0.5	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						(V_{EE}) Gnd	
			V_{IHmax}	V_{ILmin}	V_{IHmin}	V_{ILmax}	V_{IH}	V_{IL}		
Power Supply Drain Current	I_{CC1}	8							8	
	I_{CC2}	6	4	5					8	
Input Current	I_{inH1}	15	15						8	
		11	11						8	
		12	12						8	
		13	13						8	
	I_{inH2}	4	5	4					8	
		5	5	4					8	
	I_{inH3}	5	4	5					8	
	I_{inH4}	9					9		8	
10						10		8		
Leakage Current	I_{inL1}	15							8,15	
		11							8,11	
		12							8,12	
		13							8,13	
I_{inL2}	9						9	8		
	10						10	8		
Reference Voltage	V_{BB}	14						8		
Logic '1' Output Voltage	V_{OH1} (Note 1)	2		11,12,13				9,10	8	
		3		11,12,13				9,10	8	
V_{OH2}	7	5	4					8		
Logic '0' Output Voltage	V_{OL1} (Note 1)	2		11,12,13				9,10	8	
		3		11,12,13				9,10	8	
	V_{OL2}	7	4	5					8	
Logic '1' Threshold Voltage	V_{OHA} (Note 2)	2			11,12,13				8	
		3			11,12,13				8	
Logic '0' Threshold Voltage	V_{OLA} (Note 3)	2				11,12,13		8		
		3				11,12,13		8		
Short Circuit Current	I_{OS}	7	5	4				7	8	

- NOTES:** 1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
 2. In addition to meeting the output levels specified, the device must divide by 5 or 8 during this test. The clock input is the waveform shown.
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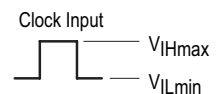
ELECTRICAL CHARACTERISTICS (continued) (Supply Voltage = 5.0 V, unless otherwise noted.)

			TEST VOLTAGE/CURRENT VALUES							
			Volts			mA				
			V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}		I_{OH}	
			@ Test Temperature							
			-30°C	2.0	0.8	5.0	-0.25	16	-0.40	
			25°C	2.0	0.8	5.0	-0.25	16	-0.40	
			85°C	2.0	0.8	5.0	-0.25	16	-0.40	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						(V _{EE}) Gnd	
			V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}		
Power Supply Drain Current	I_{CC1}	8			1,16				8	
	I_{CC2}	6			6				8	
Input Current	I_{inH1}	15			1,16				8	
		11	9,10		1,16				8	
		12	9,10		1,16				8	
		13	9,10		1,16				8	
	I_{inH2}	4			6				8	
		5			6				8	
	I_{inH3}	5			6				8	
I_{inH4}	9			1,16				8		
	10			1,16				8		
Leakage Current	I_{inL1}	15			1,16				8,15	
		11			1,16				8,11	
		12			1,16				8,12	
		13			1,16				8,13	
I_{inL2}	9			1,16				8		
	10			1,16				8		
Reference Voltage	V_{BB}	14			1,16	14			8	
Logic '1' Output Voltage	V_{OH1} (Note 1)	2			1,16				8	
		3			1,16				8	
V_{OH2}	7			6			7	8		
Logic '0' Output Voltage	V_{OL1} (Note 1)	2			1,16				8	
		3			1,16				8	
	V_{OL2}	7			6		7		8	
Logic '1' Threshold Voltage	V_{OHA} (Note 2)	2	9,10		1,16				8	
		3	9,10		1,16				8	
Logic '0' Threshold Voltage	V_{OLA} (Note 3)	2		9,10	1,16				8	
		3		9,10	1,16				8	
Short Circuit Current	I_{OS}	7			6				8	

NOTES: 1. Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.

2. In addition to meeting the output levels specified, the device must divide by 5 or 8 during this test. The clock input is the waveform shown.

3. In addition to meeting the output levels specified, the device must divide by 6 or 9 during this test. The clock input is the waveform shown.



SWITCHING CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	ML12509, ML12511, ML12513									TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW:								
			-30°C			25°C			85°C			Unit	Pulse Gen.1	Pulse Gen.2	Pulse Gen.3	V _{IHmin} †	V _{ILmin} †	V _F -3.0 V	V _{EE} -3.0 V	V _{CC} +2.0
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max									
Propagation Delay (See Figures 3 and 5)	t _{15+ 2+} t _{15+ 2-} t _{5+ 7+} t _{5- 7-}	2 2 7 7	— — — —	— — — —	8.1 7.5 8.4 6.5	— — — —	— — — —	8.1 7.5 8.1 6.5	— — — —	— — — —	8.9 8.2 8.9 7.1	ns ns A A	15 15 — —	— — — —	— — — —	— — — —	11,12,13 11,12,13 — —	9,10 9,10 — —	8 8 8 8	1,6,16 1,6,16 1,6,16 1,6,16
Setup Time (See Figures 4 and 5)	t _{setup1} t _{setup2}	11 9	5.0 5.0	— —	— —	5.0 5.0	— —	— —	5.0 5.0	— —	— —	ns ns	15 15	* *	— —	— —	11,12,13 11,12,13	9,10 *	8 8	1,6,16 1,6,16
Release Time (See Figures 4 and 5)	t _{rel1} t _{rel2}	11 9	5.0 5.0	— —	— —	5.0 5.0	— —	— —	5.0 5.0	— —	— —	ns ns	15 15	* *	— —	— —	11,12,13 *	9,10 *	8 8	1,6,16 1,6,16
Toggle Frequency (See Figure 6) ML12509 : 5/6 ML12511 : 8/9	f _{max}	2	— 440 500	— — —	— 480 550	— — —	— — —	— 440 500	— — —	— — —	— — —	MHz — —	— — —	— — —	— — —	— — —	— — —	— — —	8 8 8	16 16 16

*Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or M TTL).

	-30°C	25°C	85°C	
†V _{IHmin}	1.03	1.115	1.20	V _{dc}
†V _{ILmin}	0.175	0.200	0.235	V _{dc}

Figure 3. AC Voltage Waveforms

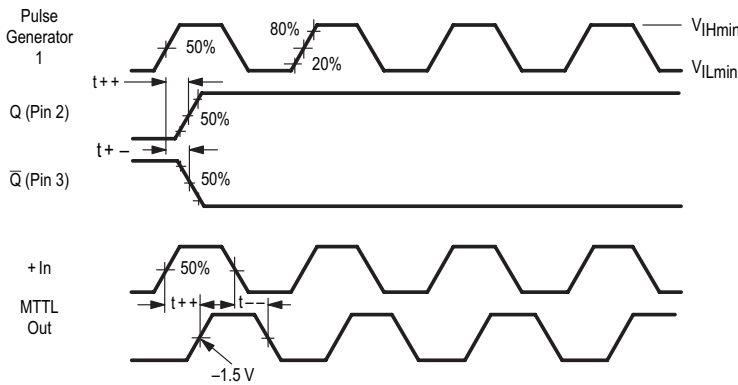


Figure 4. Setup and Release Time Waveforms

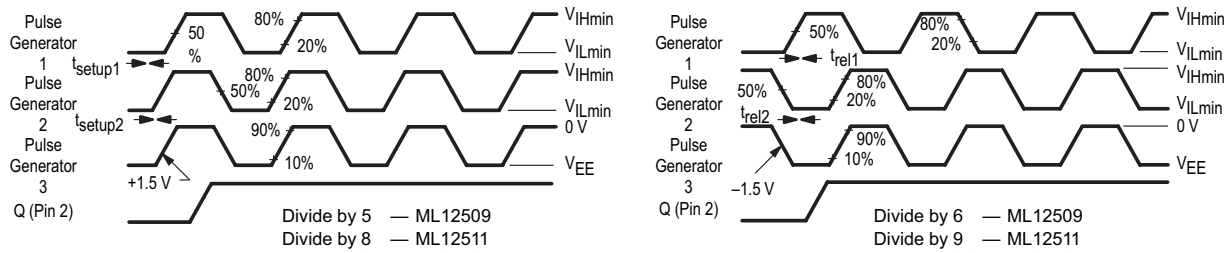


Figure 5. AC Test Circuit

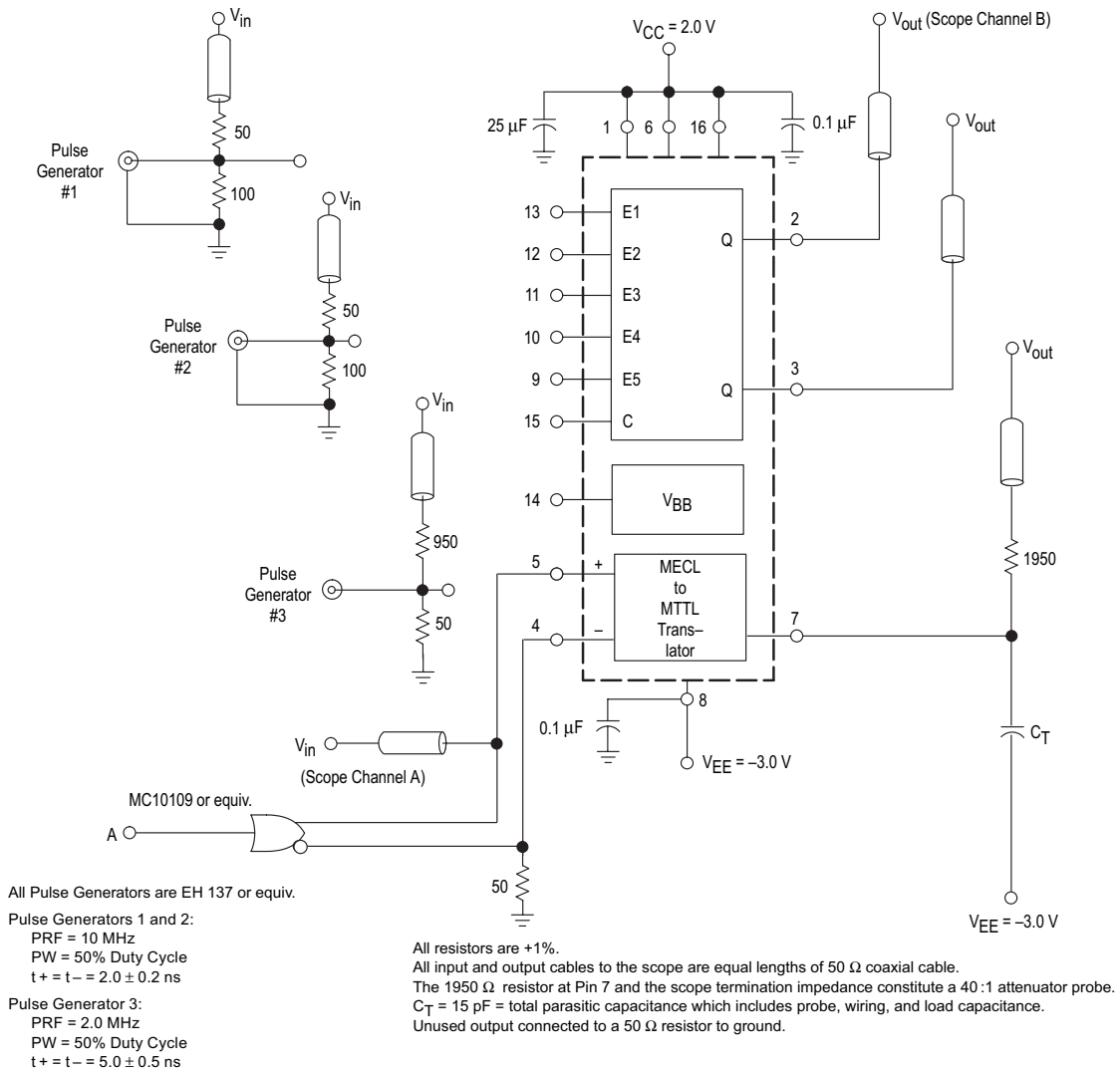
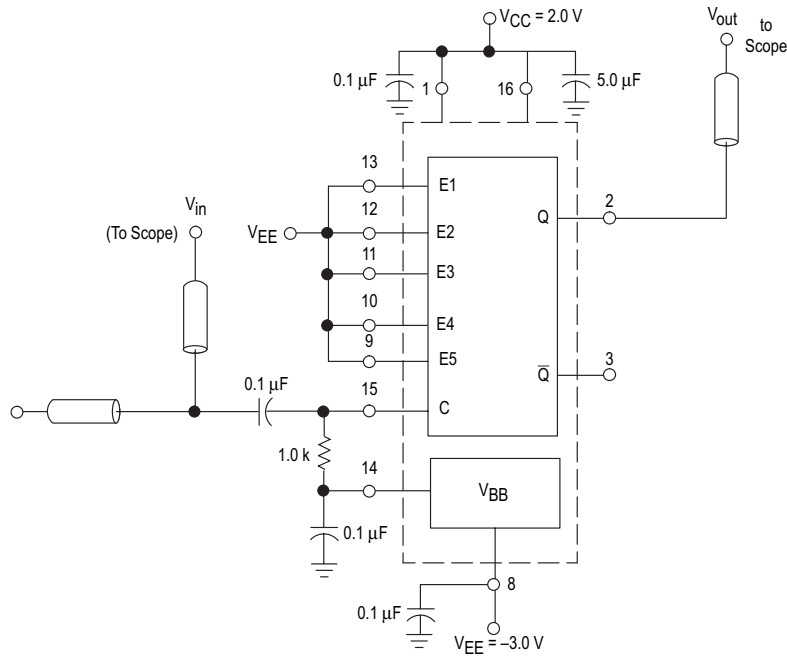


Figure 6. Maximum Frequency Test Circuit



Unused output connected to a 50 Ω resistor to ground

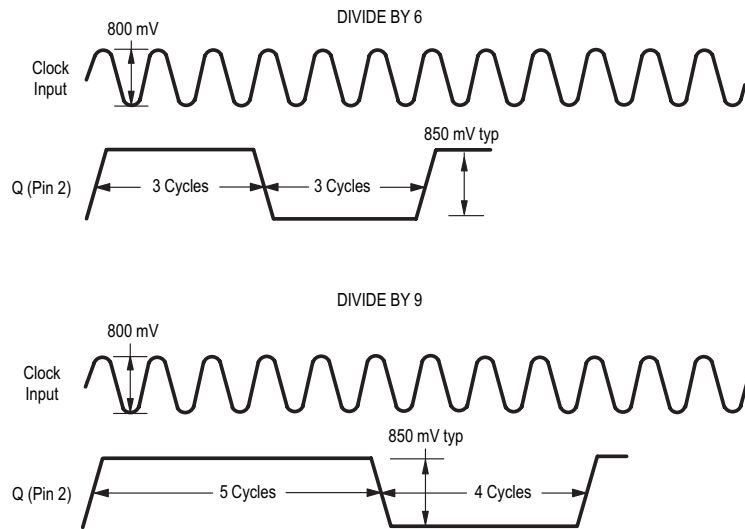
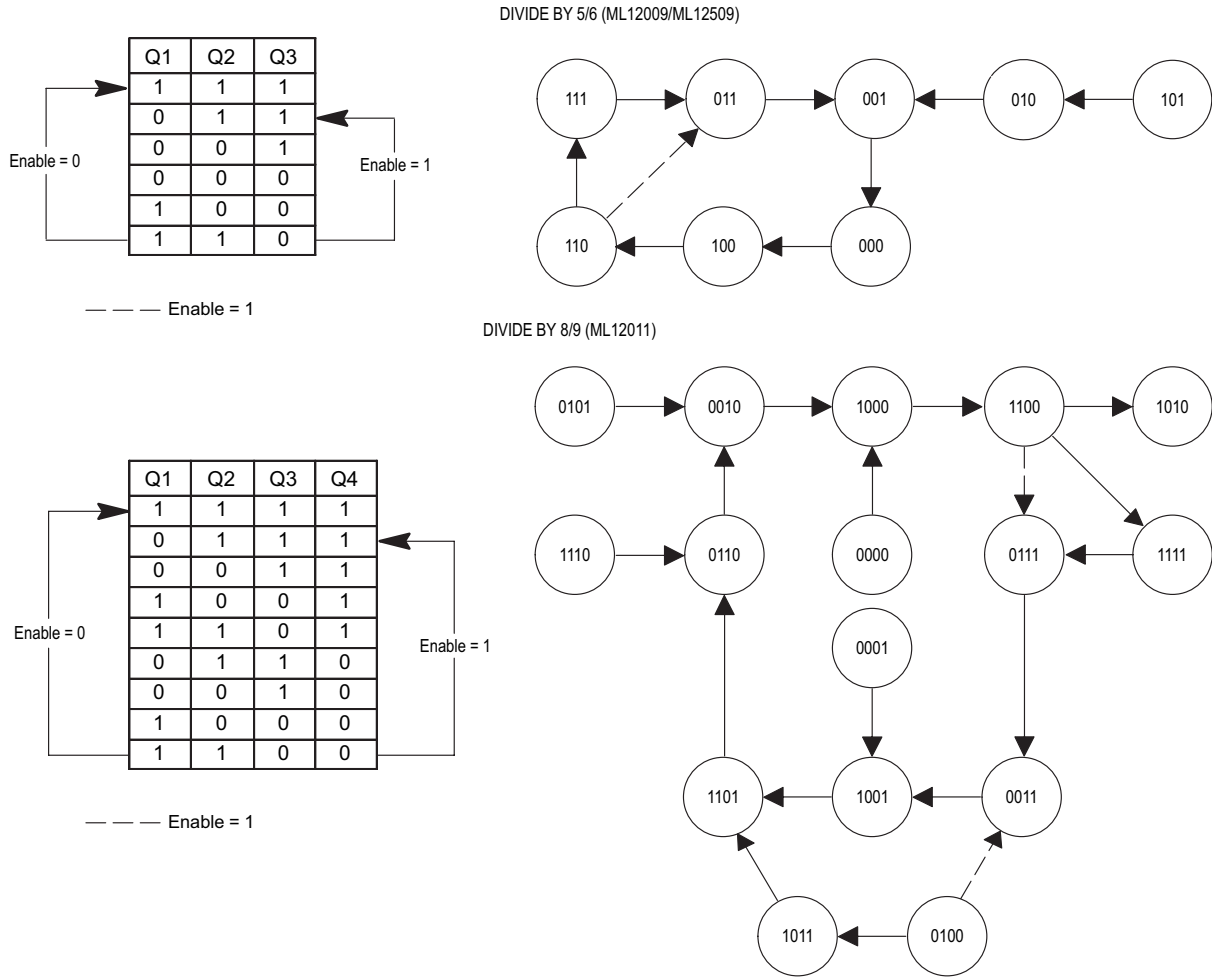


Figure 7. State Diagram



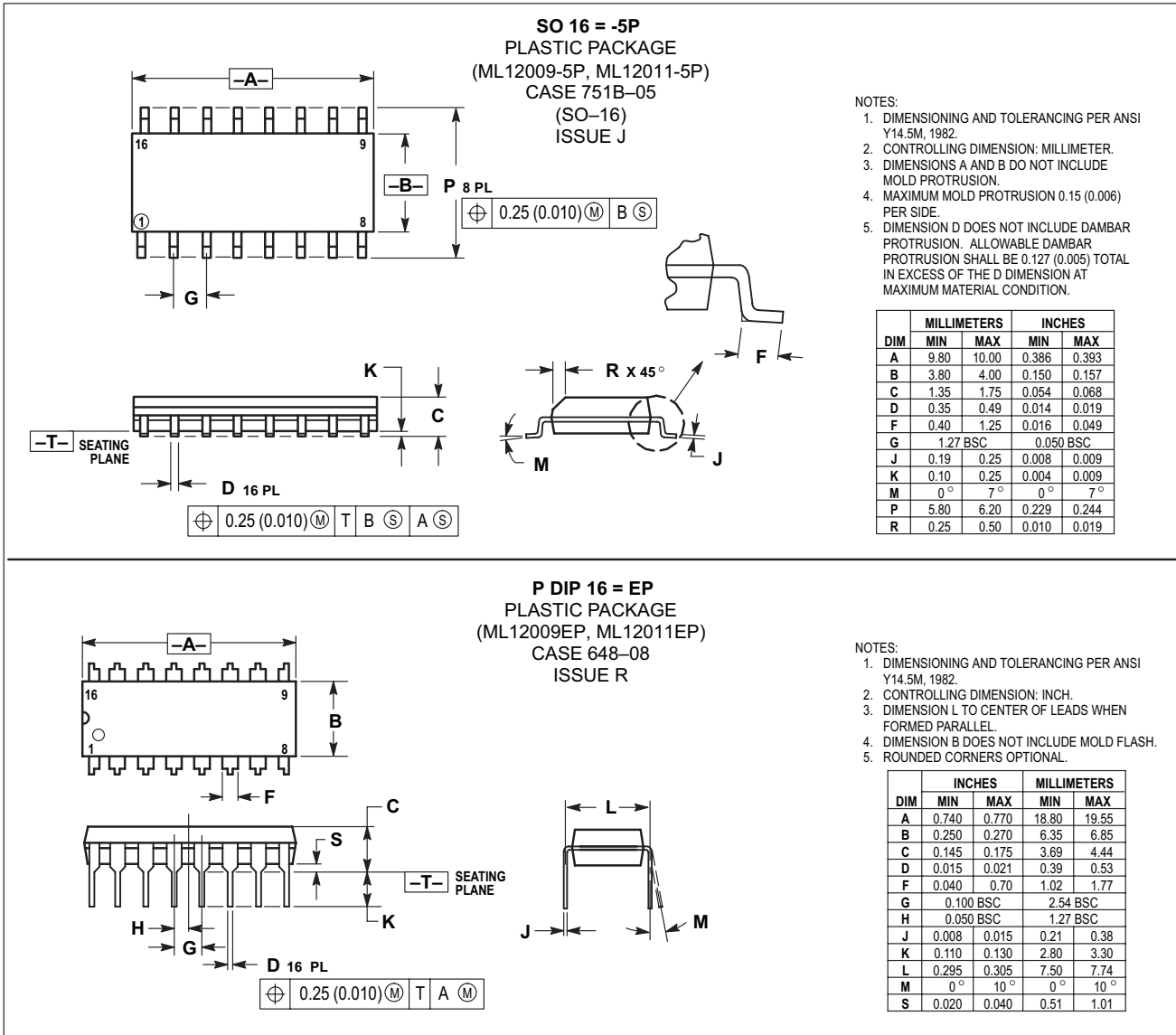
APPLICATIONS INFORMATION

The primary application of these devices is as a high-speed variable modulus prescaler in the divide by N section of a phase-locked loop synthesizer used as the local oscillator of two-way radios.

Proper VHF termination techniques should be followed when the clock is separated from the prescaler by any appreciable distance.

In their basic form, these devices will divide by 5/6 or 8/9. Division by 5, or 8 occurs when any one or all of the five gate inputs E1 through E5 are high. Division by 6, or 9 occurs when all inputs E1 through E5 are low. (Unconnected MTTL inputs are normally high, unconnected MECL inputs are normally low). With the addition of extra parts, many different division configurations may be obtained.

OUTLINE DIMENSIONS



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