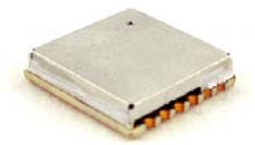
Z-Communications, Inc.
9939 Via Pasar • San Diego, CA 92126
TEL (858) 621-2700 FAX (858) 621-2722

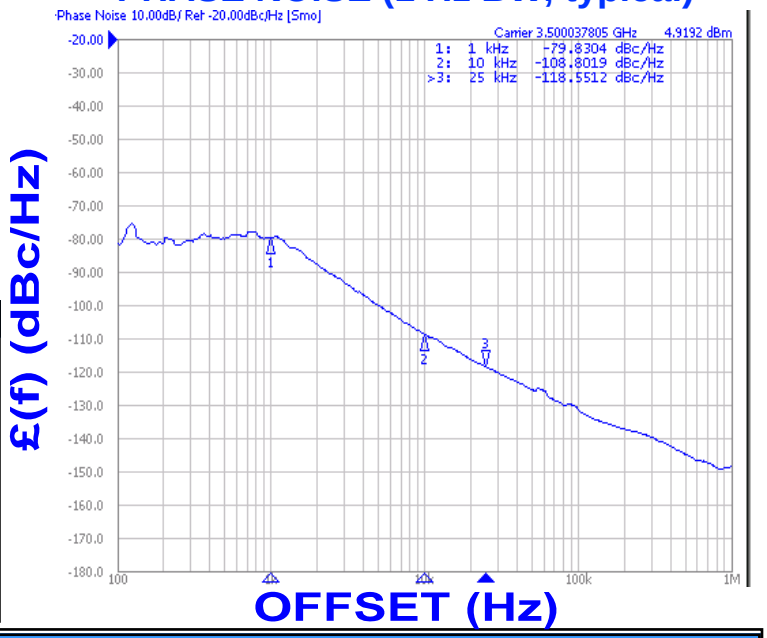
SFS3500C-LF

Fixed Frequency Synthesizer

Rev A1



PHASE NOISE (1 Hz BW, typical)



FEATURES

- Frequency : 3500 MHz
- RMS Phase Error 0.5 deg
- Package Style: PLL-V12N

APPLICATIONS

- WLAN
- Broadband Transmission
-

PERFORMANCE SPECIFICATIONS	VALUE	UNITS
Frequency	3500	MHz
Phase Noise @ 10 KHz offset (1 Hz BW, typ.)	-108	dBc/Hz
RMS Phase Error	0.5	deg
Harmonic Suppression (2nd, typ.)	-15	dBc
Sideband Spurs (typ.)	-65	dBc
Power Output	0±3	dBm
Load Impedance	50	Ω
Startup Lock Time (typ.)	2	mSec
Reference Oscillator	10	MHz
Operating Temperature Range	-40 to 85	°C
Package Style	PLL-V12N	
POWER SUPPLY REQUIREMENTS		
Supply Voltage: P1(Vcc, nom.)	5	Vdc
Supply Current: P1 (Icc, typ.)	30	mA
Supply Voltage: P6 (Vcc, nom.)	3	Vdc
Supply Current: P6 (Icc, typ.)	11	mA

All specifications are typical unless otherwise noted and subject to change without notice.

APPLICATION NOTES

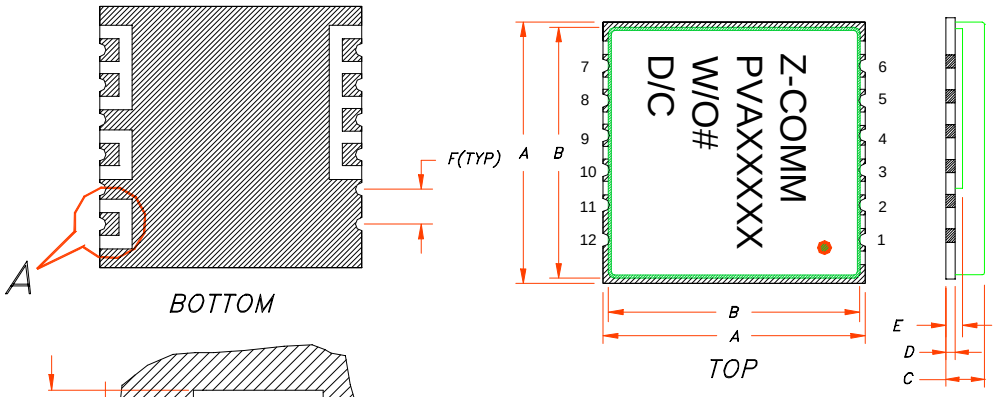
- AN-107 : How to Solder Z-COMM VCOs / PLLs
- AN-200 : Mounting and Grounding of Z-COMM PLLs
- AN-205 : Phase Noise Measurement of Z-COMM SFS Series.

NOTES:

Note1: Phase noise measurement was performed using a 10MHz CMOS reference oscillator with a phase noise of -145dBc/Hz @1KHz.

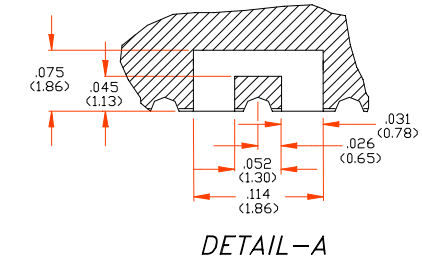
Note2: For Reference oscillator frequency of <20MHz, ensure SR>50V/us. See Analog Devices ADF4106 application note for more details.

PHYSICAL DIMENSIONS



PIN OUT DETAILS
P1 VCC (VCO)
P2 GROUND
P3 RF OUT
P4 GROUND
P5 MUX OUT
P6 VCC (CHIP)
P7 CLOCK
P8 DATA
P9 ENABLE
P10 REFERENCE OSCILLATOR INPUT
P11 GROUND
P12 GROUND

P7, P8 & P9 SHALL BE N/C FOR INTERNALLY PROGRAMMABLE MODELS



	INCH	MM
A	0.600	15.00
B	0.576	14.40
C	0.135 MAX	3.40 MAX
D	0.032	0.78
E	0.025	0.63
F	0.080	2.00