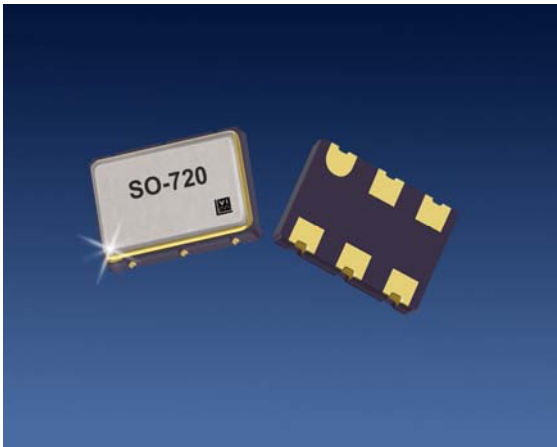


## SO-720 SAW Based Clock Oscillator



### Features

- Industry Standard Package, 5.0 x 7.5 x 2.0 mm
- ASIC Technology For Ultra Low Jitter
  - 0.100 ps-rms typical across 12 kHz to 20 MHz BW
  - 0.120 ps-rms typical across 50 kHz to 80 MHz BW
- Output Frequencies from 150 MHz to 1 GHz
- 3.3 V Operation
- LV-PECL or LVDS Configuration with Fast Transition Times
- Complementary Outputs
- Output Disable Feature
- Improved Temperature Stability over Standard SAW XO



Product is free of lead and compliant to EC RoHS Directive

### Applications

Reference Clock for Wired and Wireless Products

<u>Description</u>	<u>Standard</u>
• 1-2-4 Gigabit Fibre Channel	INCITS 352-2002
• 10 Gigabit Fibre Channel	INCITS 364-2003
• 10GbE LAN / WAN	IEEE 802.3ae
• OC-192	ITU-T G.709
• SONET / SDH	GR-253-CORE Issue3

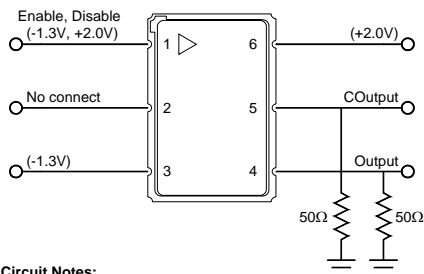
### Description

The SO-720 is a SAW Based Clock Oscillator that achieves low phase noise and very low jitter performance. The SO-720 is housed in an industry standard 6-Pad leadless ceramic package that is hermetically sealed. Packaging options include bulk or tape and reel.

# SO-720 SAW Clock Oscillator

Electrical Performance						
Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
<b>Frequency</b>						
Nominal Frequency	$f_N$	150		1000	MHz	1,2
Frequency Stability (Ordering Option)	$f_{STAB}$		$\pm 50, \pm 100$		ppm	1,2
Aging				10	ppm	6,8
<b>Supply</b>						
Voltage	$V_{CC}$	2.97	3.3	3.63	V	2,3
Current (No Load)	$I_{CC}$		55	70	mA	3
<b>Outputs</b>						
Mid Level - LVPECL		$V_{CC}-1.4$	$V_{CC}-1.25$	$V_{CC}-1.0$	V	2,3
Swing – LVPECL		450	600	750	mV-pp	2,3
Mid Level - LVDS		$V_{CC}-2.4$	$V_{CC}-2.3$	$V_{CC}-2.5$	V	2,3
Swing – LVDS		250	350	450	mV-pp	2,3
Current	$I_{OUT}$			20	mA	6
Rise Time	$t_R$			500	ps	5,6
Fall Time	$t_F$			500	ps	5,6
Symmetry	SYM	45	50	55	%	2,3
Jitter (12 kHz – 20 MHz BW) 622.08 MHz	$\phi_J$		0.100	0.250	ps-rms	6,7
Jitter (50 kHz – 80 MHz BW) 622.08 MHz	$\phi_J$		0.120	0.300	ps-rms	6,7
Period Jitter, RMS (622.08 MHz)	$\phi_J$		2.5	3.0	ps-rms	9
Period Jitter, Peak - Peak (622.08 MHz)	$\phi_J$		16	24	ps pk-pk	9
<b>Operating Temp. (Ordering Option)</b>						
	$T_{OP}$	0/70,-20/70 or -40/85			°C	1
<b>Package Size</b>						
		5.0 x 7.5 x 2.0			mm	

1. See Standard Frequencies and Ordering Information (Pg 7).
2. Parameters are tested with production test circuit below (Fig 1).
3. Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.
4. Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
5. Measured from 20% to 80% of a full output swing (Fig 2).
6. Not tested in production, guaranteed by design, verified at qualification.
7. Integrated across stated bandwidth per GR-253-CORE Issue3.
8. Aging Rate for 10 years (Aging is not part of overall frequency stability budget unless specified at time of order)
9. Broadband Period Jitter measured using Lecroy Wavemaster 8600A 6 GHz Oscilloscope, 250K samples taken.



**Test Circuit Notes:**  
 1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.  
 2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.  
 3) 50Ω Terminations are Within Test Equipment.

Figure 1. Test Circuit

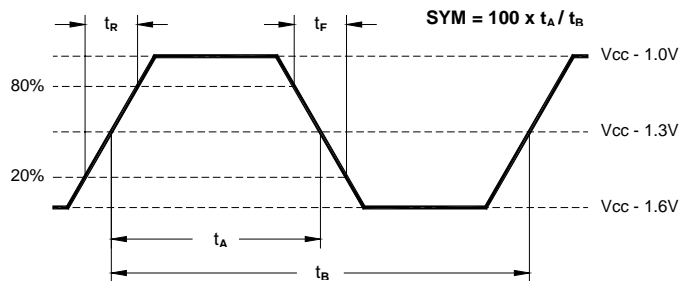
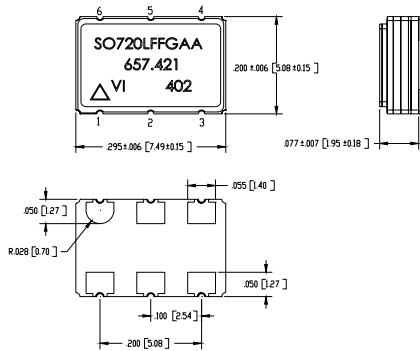


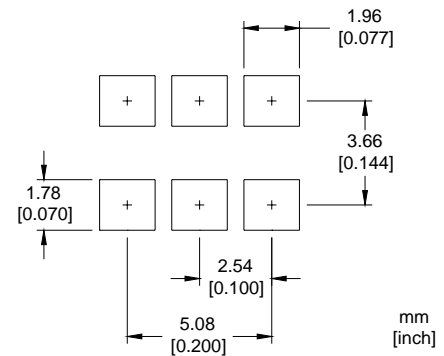
Figure 2. 10K LV-PECL Waveform

# SO-720 SAW Clock Oscillator

## Outline Diagram



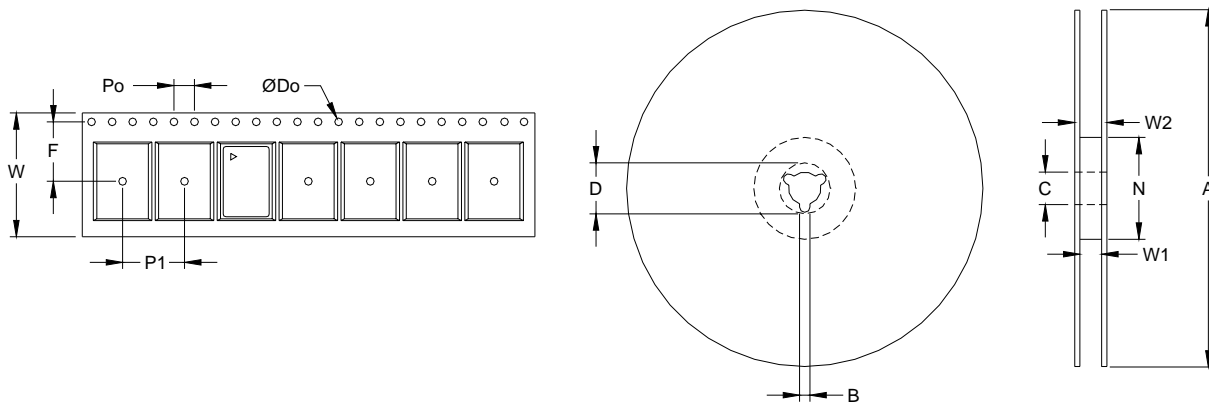
## Suggested Pad Layout



Pin Out		
Pin	Symbol	Function
1	NC or OE <sup>1</sup>	NC or Enable = LV-CMOS Logic 0 or Ground Disabled = LV-CMOS Logic 1
2	OE <sup>1</sup> or NC	NC or Enable = LV-CMOS Logic 0 or Ground Disabled = LV-CMOS Logic 1
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V <sub>CC</sub>	Power Supply Voltage (+3.3V ± 10%)

Note 1: For proper operation, chosen disable pin can not be left floating and a pin 1 or pin 2 enable option must be ordered  
See page 7 for alternative input logic option

## Tape and Reel (EIA-481-2-A)



Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	Reel
SO-720	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

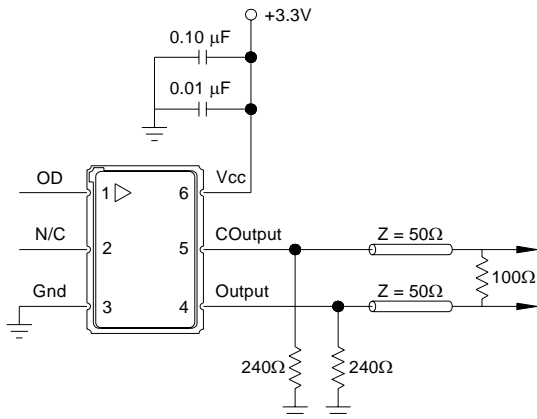
# SO-720 SAW Clock Oscillator

## Absolute Maximum Ratings

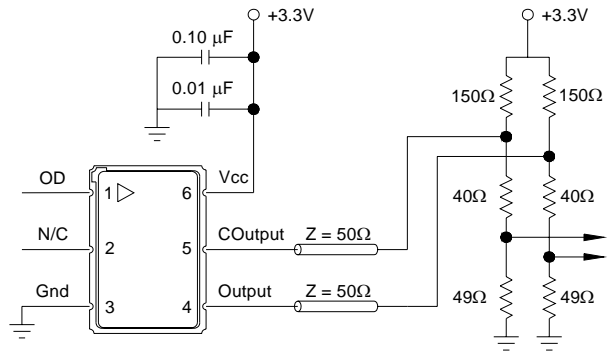
Parameter	Symbol	Ratings	Unit
Power Supply	$V_{CC}$	0 to 4	V
Output Current	$I_{out}$	25	mA
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	$T_{LS}$	260 / 40	°C/sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if OD is applied before  $V_{CC}$ .

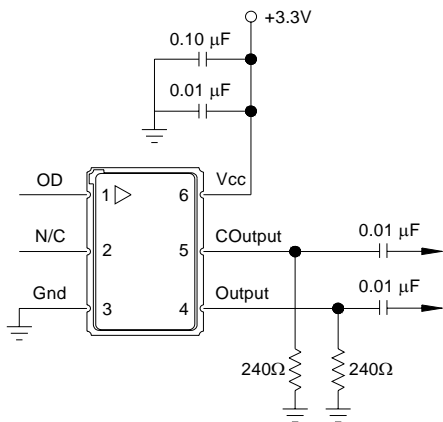
## Suggested Output Load Configurations



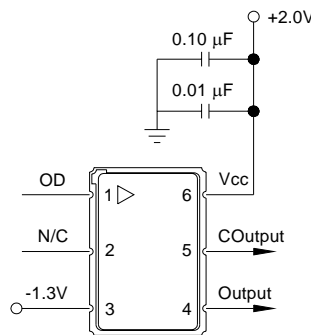
**LV-PECL to LV-PECL:** For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.



**LV-PECL to LVDS:** Restricted for short transmission lengths. Configuration may require modification depending on LVDS receiver.



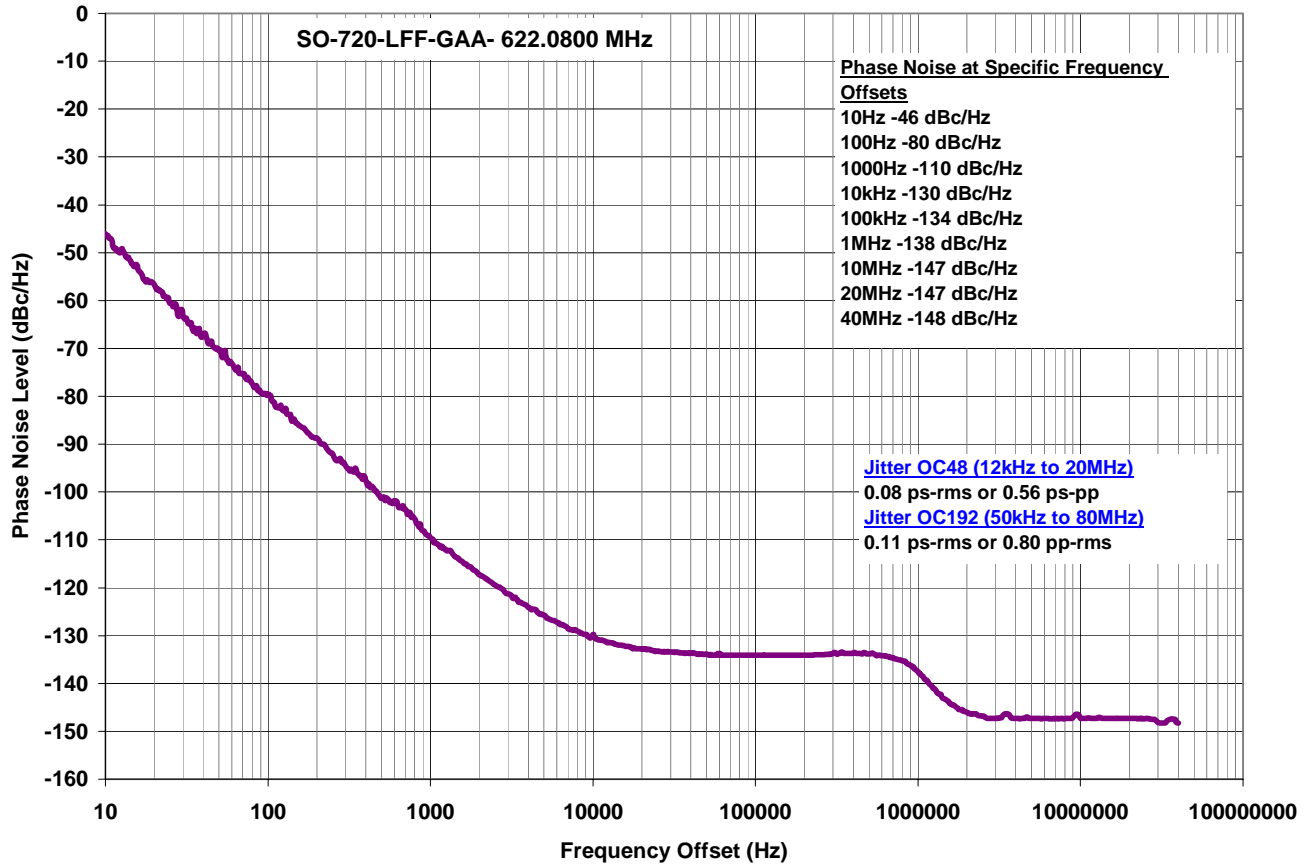
**Functional Test:** Allows standard power supply configuration. Since AC coupled, the LV-PECL levels cannot be measured.



**Production Test:** Allows direct DC coupling into 50Ω measurement equipment. Must bias the power supplies as shown. Similar to Figure 1.

# SO-720 SAW Clock Oscillator

## Typical Phase Noise



# SO-720 SAW Clock Oscillator

## Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The SO-720 family is capable of meeting the following qualification tests:

### Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

### Handling Precautions

Although ESD protection circuitry has been designed into the SO-720 proper precautions should be taken when handling and mounting. VI employs a Human Body model (HBM) and a Man-Man model (MM) for ESD susceptibility testing and design protection evaluation.

### ESD Ratings

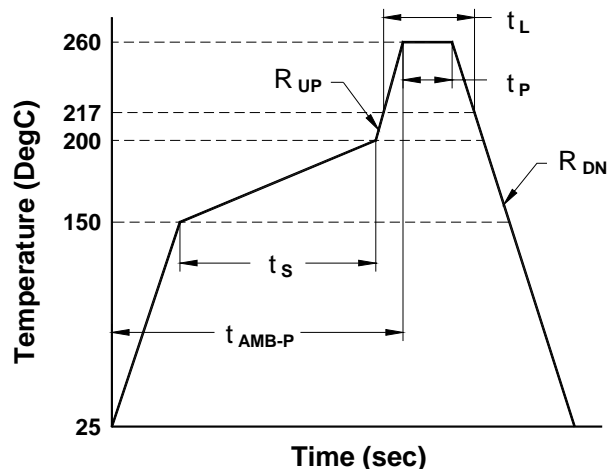
Model	Minimum	Conditions
Human Body Model	1500 V	MIL-STD 883, Method 3015
Man Man Model	200 V	V/JESD22-A115-A,

### Reflow Profile (IPC/JEDEC J-STD-020)

Parameter	Symbol	Value
PreHeat Time	$t_s$	60 sec Min, 180 sec Max
Ramp Up	$R_{UP}$	3 °C/sec Max
Time Above 217 °C	$t_L$	60 sec Min, 150 sec Max
Time To Peak Temperature	$t_{AMB-P}$	480 sec Max
Time At 260 °C	$t_P$	20 sec Min, 40 sec Max
Ramp Down	$R_{DN}$	6 °C/sec Max

The device is designed to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The SO-720 device is hermetically sealed so an aqueous wash is not an issue.

Termination Plating: Electroless Gold Plate over Nickel Plate



# SO-720 SAW Clock Oscillator

## Standard Output Frequencies (MHz)

*155.5200	*156.2500	*160.0000	*175.0000	*187.5000	*194.8000	*200.0000	*240.0000
*250.0000	*268.8000	300.0000	311.0400	312.5000	320.0000	350.0000	375.0000
389.6000	400.0000	480.0000	500.0000	531.2500	532.0000	533.0000	537.6000
600.0000	622.0800	625.0000	640.0000	644.5313	657.4219	666.5143	669.3266
672.1627	690.5692	693.4830	704.3806	707.3527	720.0000	768.0000	796.8750
901.1200	1000.000						

Frequencies not shown are available upon request. \*VCC6 is preferred XO for frequencies < 300 MHz

## Revision Control

<b>A</b>	<b>6/21/06</b>	<b>Vectron Prod. Mgt.</b>	<b>Release of SO-720 Datasheet</b>
<b>B</b>	<b>11/28/07</b>	<b>Tim Glass</b>	<b>Increased Frequency Range to 1 GHz</b>

## Ordering Information

### SO - 720 - L F F - G A A - xxx.xxx

**Product Family**

SO = SO Based XO

**Package**

720 = 5.0 x 7.5 x 2.0 mm  
6 Pad Ceramic SMD

**Input**

L = 3.3 Vdc ± 10%

**Output**

F = LVPECL (45/55% Symmetry)  
P = LVDS (45/55% Symmetry)

**Frequency**

150 - 1000 MHz

**Overall Stability Condition**

A = Includes 10 years of aging at 40°C  
N = Excludes aging

**Enable/Disable Pin & Input Logic**

A = Pin 2: Enable Low (or Gnd) / Disable High  
B = Pin 2: Enable High (or Vcc) / Disable Low  
C = Pin 1: Enable Low (or Gnd) / Disable High  
D = Pin 1: Enable High (or Vcc) / Disable Low

**Stability**

G = ± 50 ppm maximum  
H = ± 100 ppm maximum

**Operating Temperature**

C = 0°C to 70°C  
D = -20°C to 70°C  
F = -40°C to 85°C

Not All Combinations Possible

## For Additional Information, Please Contact:



USA: Vectron International, 267 Lowell Rd, Hudson, NH 03051 . . . . . Tel: 1-88-VECTRON-1  
EUROPE: . . . . . Tel: +49 (0) 3328-4784-17  
ASIA: . . . . . Tel: +86-21-28909740

Fax: 1-888-FAX-VECTRON  
Fax: +49 (0) 3328-4784-30  
Fax: +86-21-28909240

Vectron International reserves the right to make changes to the product(s) and or information contained herein without notice. No liability is assumed as a result of their use or application. No rights under any patent accompany the sale of any such product(s) or information.