HIGH-VOLTAGE MIXED-SIGNAL IC

UC1697v

128 x 128RGB C-STN LCD Controller-Driver
w/ 16-bit per RGB On-Chip SRAM

ES Specifications
Revision 0.6

February 7, 2007

ULTRACHIP

The Coolest LCD Drive, Ever!!

Specifications and information herein are subject to change without notice.

TABLE OF CONTENT

UC1697v

Single-Chip, Ultra-Low Power
128COM x 128RGB Matrix
Passive Color LCD Controller-Driver

INTRODUCTION

UC1697v is an advanced high-voltage mixed-signal CMOS IC, specially designed for the display needs of low power hand-held devices.

In addition to low power COM and SEG drivers, UC1697v contains all necessary circuits for high-V LCD power supply, bias voltage generation, temperature compensation, timing generation, and graphics data memory.

UC1697v employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture and LRM (Line Rate Modulation) gray-shade modulation scheme to achieve well balanced shading, vivid colors, and natural-looking images.

With UC1697v, LCD makers can now achieve TFT-like image quality, while maintaining the same STN advantages in power consumption, unit cost, ease of customization and production flexibility.

MAIN APPLICATIONS

- Cellular Phones and other battery operated hand held devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 128x128 matrix C-STN LCD with comprehensive support for input format and color depth:
  8-bit RGB: 256-color
  12-bit RGB: 4K-color
  16-bit RGB: 64K-color
- A software-readable ID bit (ID0) to support configurable vender identification.
- ID pin (ID1)-switched input data sets (D[7:0] or D[14,12,10,8,6,4,2,0]) for 8-bit mode.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both row-ordered and column-ordered display buffer RAM access.
- Support industry standard 4-wire, 3/4-wire, and 3-wire serial bus (S8, S8uc, S9) and 16-bit/8-bit parallel bus (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Four software programmable temperature compensation coefficients.
- Software programmable, self-configuring 10x charge pump.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Pad layouts support COG applications.
- V_{DD} (digital) range: 1.8V(Typ.) ~ 3.3V
  V_{DD} (analog) range: 2.6V(Typ.) ~ 3.3V
  LCD V_{OP} range: 6.4V ~ 16.5V
- Available MTP trimming supports precise LCD contrast matching.
- Available in gold bump dies.

  COM/SEG bump information
  Bump pitch: 26.5 μM
  Bump gap: 12.0 μM
  Bump surface: 2001 μM^2

ORDERING INFORMATION

GOLD BUMPED DIE

Part Number	MTP	I^2C	Description
UC1697vGAA	Yes	No	Gold bumped die, with MTP function.

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

MTP LIGHT & ESD SENSITIVITY

The MTP memory cell is sensitive to photon excitation and ESD. Under extended exposure to strong ambient light, or when TST4 pin is exposed to ESD strikes, the MTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light & ESD shields to realize full MTP content retention performance.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

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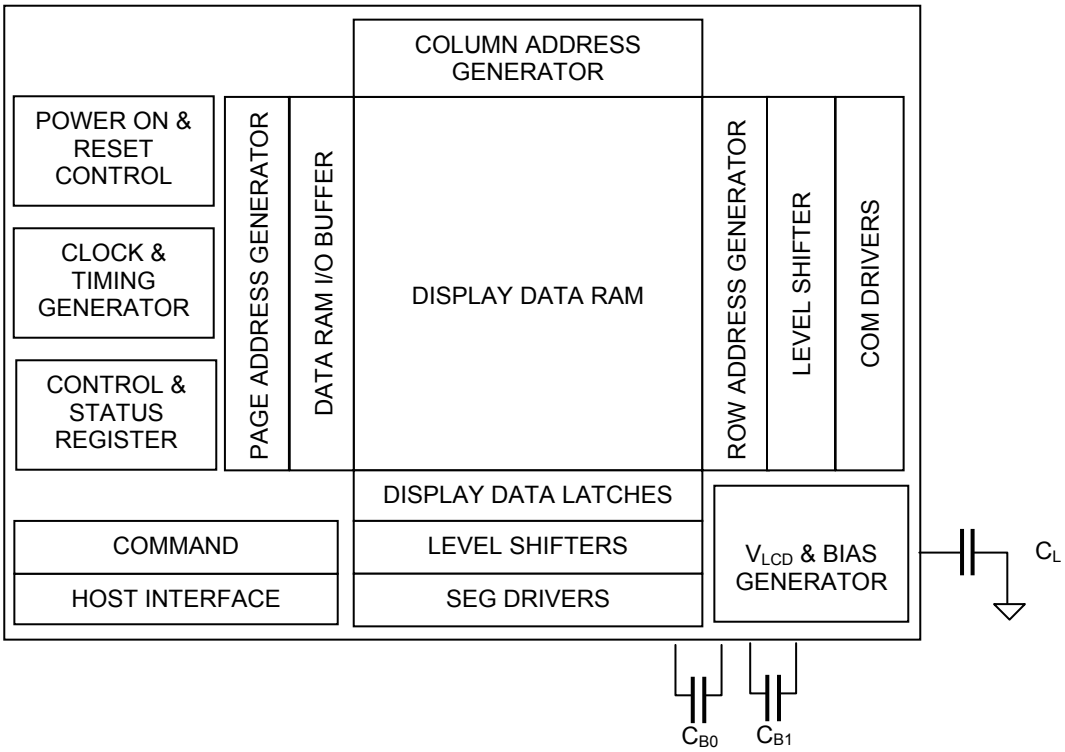
BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	# of Pads	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	9 9 2	V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. Please maintain the following relationship: $V_{DD}+1.3V \geqslant V_{DD2/3} \geqslant V_{DD}$ Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	12 12	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for this node.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{B1+} , V_{B1-} V_{B0+} , V_{B0-}	PWR	6, 6 6, 6	LCD SEG driving voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect a capacitor, C_{BX}, between V_{BX+} and V_{BX-} . The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V_{LCD-IN} $V_{LCD-OUT}$	PWR	2 2	High voltage LCD Power Supply. When internal V_{LCD} is used, connect these pins together. When external V_{LCD} is used, connect external V_{LCD} source to V_{LCDIN} pins and leave V_{LCDOUT} open. Capacitor C_L should be connected between V_{LCD} and V_{SS}. In COG applications, keep the ITO trace resistance under 30 Ω.

NOTE

- Recommended capacitor values:
  C_{Bx} : 2.2μF/5V or 300x LCD load capacitance, whichever is higher.
  C_L : 330nF (25V) is appropriate for most applications.

<table>
<tr><th>Name</th><th>Type</th><th># of Pads</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1</td><td>I</td><td>1
1</td><td>Bus mode: The interface bus mode is determined by BM[1:0] and {DB15, DB13} by the following relationship:
<table>
<tr><th>BM[1:0]</th><th>{DB15, DB13}</th><th>Mode</th></tr>
<tr><td>11</td><td>Data</td><td>6800/16-bit</td></tr>
<tr><td>10</td><td>Data</td><td>8080/16-bit</td></tr>
<tr><td>01</td><td>0x</td><td>6800/8-bit</td></tr>
<tr><td>00</td><td>0x</td><td>8080/8-bit</td></tr>
<tr><td>01</td><td>10</td><td>3-wire SPI w/ 9-bit token
(S9: conventional)</td></tr>
<tr><td>00</td><td>10</td><td>4-wire SPI w/ 8-bit token
(S8: conventional)</td></tr>
<tr><td>00</td><td>11</td><td>3/4-wire SPI w/ 8-bit token
(S8uc: Ultra-Compact)</td></tr>
</table></td></tr>
<tr><td>CS0
CS1</td><td>I</td><td>1
1</td><td>Chip Select. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, D[15:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states.
An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Select Control data or Display data for read/write operation. In S9, CD pin is not used. Connect CD to V_{SS} when not used.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>ID0</td><td>I</td><td>1</td><td>Used for production control.
Connect ID0 to V_{DD} for “H” or V_{SS} for “L”.
The wiring status of ID0 is available with PID[1:0] of the <code>Get Status</code> command.</td></tr>
<tr><td>ID1</td><td>I</td><td>1</td><td>Select input data set for 8-bit mode.
ID1=0 : 8-bit input data are D[0, 2, 4, 6, 8, 10, 12, 14]
ID1=1 : 8-bit input data are D[0:7]
The wiring status of ID1 is available with PID[1:0] of the <code>Get Status</code> command. Other than 8-bit mode, connect ID1 to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR[1:0] controls the read/write operation of the host interface. See section Host Interface for more detail.
In parallel mode, the meaning of WR[1:0] depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
</table>

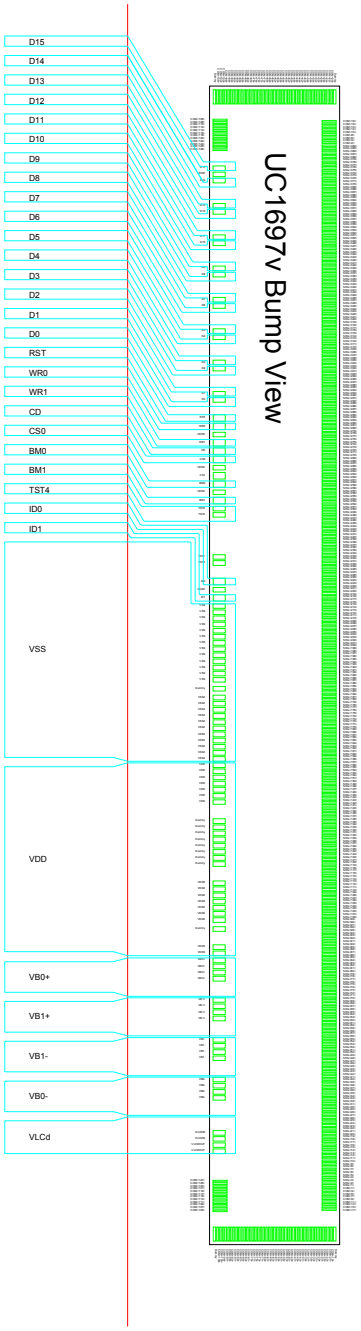
<table>
<tr><th>Name</th><th>Type</th><th># of Pads</th><th>Description</th></tr>
<tr><td colspan="4">DATA BUS</td></tr>
<tr><td>D0~D15</td><td>I/O</td><td>16</td><td>Bi-directional bus for parallel host interfaces.
In serial modes, connect DB[0] to SCK, DB[8] to SDA.
<table>
<tr><th></th><th>BM=1x
(16-bit)</th><th>BM=0x
(8-bit)
ID1=0</th><th>BM=0x
(8-bit)
ID1=1</th><th>BM=01
(S9)</th><th>BM=00
(S8/S8uc)</th></tr>
<tr><td>DB0</td><td>D0</td><td>D0/D8</td><td>D0/D8</td><td>SCK</td><td>SCK</td></tr>
<tr><td>DB1</td><td>D1</td><td>–</td><td>D1/D9</td><td>–</td><td>–</td></tr>
<tr><td>DB2</td><td>D2</td><td>D1/D9</td><td>D2/D10</td><td>–</td><td>–</td></tr>
<tr><td>DB3</td><td>D3</td><td>–</td><td>D3/D11</td><td>–</td><td>–</td></tr>
<tr><td>DB4</td><td>D4</td><td>D2/D10</td><td>D4/D12</td><td>–</td><td>–</td></tr>
<tr><td>DB5</td><td>D5</td><td>–</td><td>D5/D13</td><td>–</td><td>–</td></tr>
<tr><td>DB6</td><td>D6</td><td>D3/D11</td><td>D6/D14</td><td>–</td><td>–</td></tr>
<tr><td>DB7</td><td>D7</td><td>–</td><td>D7/D15</td><td>–</td><td>–</td></tr>
<tr><td>DB8</td><td>D8</td><td>D4/D12</td><td>–</td><td>SDA</td><td>SDA</td></tr>
<tr><td>DB9</td><td>D9</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB10</td><td>D10</td><td>D5/D13</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB11</td><td>D11</td><td>–</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB12</td><td>D12</td><td>D6/D14</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB13</td><td>D13</td><td>–</td><td>–</td><td>0</td><td>0:S8 / 1:S8uc</td></tr>
<tr><td>DB14</td><td>D14</td><td>D7/D15</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB15</td><td>D15</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
</table>
Always connect unused pins to either V_{SS} or V_{DD}.</td></tr>
</table>

Name	Type	# of Pads	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG384	HV	384	SEG (column) driver outputs. Support up to 128xRGB pixels. Leave unused SEG drivers open-circuit.
COM1 ~ COM128	HV	128	COM (row) driver outputs. Support up to 128 rows. When designing LCM, always start from COM1. If the LCM has *N* pixel rows and *N* is less than 128, set CEN to be *N-1*, and leave COM drivers [N+1 ~ 128] open-circuit.
MISC. PINS			
V_{DDX}	O	5	Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus within the IC. These pads are provided to facilitate chip configurations in COG application. These pins should *NOT* be used to provide V_{DD} power to the chip. It is not necessary to connect V_{DDX} to main V_{DD} externally.
TST4	I/HV	2	Test control. This pin has on-chip pull-up resistor. Leave it open during normal operation. TST4 is also used as one of the high voltage power supply for MTP programming operation. For COG designs, please wire out TST4 with trace resistance between 30~50 Ω.
TST1 TST2	O	1 1	Test I/O pins. Leave these pins open during normal use.

NOTE:

Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM*X* or SEG*X* will correspond to index *X*-1, and the value ranges for those index registers will be 0~127 for COM and 0~383 for SEG.

RECOMMENDED COG LAYOUT



Note for V_{DD} and V_{SS} with COG:

The operation condition V_{DD}=1.8V (typical) must be satisfied under all operating conditions. With its high speed data-write condition, UC1697v's peak current (I_{DD}) can be up to ~15mA range during high speed data write to UC1697v's on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD}, V_{SS} ITO trances in COG glass modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop below 1.65V and cause the IC to malfunction.

CONTROL REGISTERS

UC1697v contains registers which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, starting with a summary table, followed by a detailed instruction-by-instruction description.

Name: The Symbolic reference of the register.
Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	7	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (no scrolling) and (127 – 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The top FLTx2 and bottom FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections: 2xFLT on one side non-scrollable, 2xFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CA	7	0H	Display Data RAM Column Address (counted in RGB triplet) (Used in Host to Display Data RAM access)
RA	7	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	3	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 000b : 6 001b : 10 010b : 11 **011b : 12** 100b : 9
TC	2	0H	Temperature Compensation (per ^{o}C) **00b : -0.00%** 01b : -0.10% 10b : -0.15% 11b : -0.05%
PM	8	5CH	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	6	00H	PM offset. PMO[5]=1: The effective PM value, PMV = PM - PMO[4:0] PMO[5]=0: The effective PM value, PMV = PM + PMO[4:0]
PC	4	EH	Power Control. PC[1:0] : 0xb: LCD: ⩽ 13nF **1xb: 13 < LCD < 22nF** PC[3:2] : 00b: External V_{LCD} **11b: Internal V_{LCD} (10x charge pump)**
AC	4	1H	Address Control: AC[0] : WA: Automatic column/row Wrap Around (**1 : ON**) AC[1] : Auto-Increment order **0 : Column (CA) first** 1 : Row (RA) first AC[2] : RID: RA (row address) auto increment direction (**0 : +1** 1 : -1) AC[3] : Window Program Mode **0 : Inside Mode:** Write to SRAM within the window defined by (WPC0, WPP0), (WPC1, WPP1) 1 : Outside Mode: Write to SRAM but skip the window defined by (WPC0, WPP0), (WPC1, WPP1)

Name	Bits	Default	Description
DC	5	18H	Display Control: DC[0] : PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1] : APO: All Pixels ON (Default **0: OFF**) DC[2] : Display ON/OFF (Default **0: OFF**) When DC[2] is set to 0, the IC will enter Sleep mode. DC[3] : Gray-shade Modulation mode. 0 : On/Off mode **1 : 32-shade Mode** DC[4] : Green Enhance Mode. *Only valid in 4K-color mode.* 0 : Enable. Allows an extra display bit for green color. **1 : Disable**
LC	10	090H	LCD Control: LC[0] : Enable the top FLTx2 and bottom FLBx2 lines in partial display mode (Default **OFF**). LC[1] : MX, Mirror X. SEG/Column sequence inversion (Default: **OFF**) LC[2] : MY, Mirror Y. COM/Row sequence inversion (Default: **OFF**) LC[4:3] : Line Rate (Klps: Kilo-Line-per-second) 00b : 20.1 Klps 01b : 24.4 Klps **10b : 29.6 Klps** 11b : 35.8 Klps Line Rate (for 8-color On/Off mode) 00b : 5.5 Klps 01b : 6.6 Klps **10b : 8.0 Klps** 11b : 9.7 Klps (Line-Rate = Frame-Rate x Mux-Rate) LC[5] : RGB filter order (as mapped to SEG1, SEG2, SEG3) **0 : BGR-BGR** 1 : RGB-RGB LC[7:6] : Color and input mode when DC[4]=1: 00b : 256 color mode 3R-3G-2B (8-bit/RGB) 01b : 4K color mode 4R-4G-4B (12-bit/RGB) **10b : 64K color mode** 5R-6G-5B (16-bit/RGB) when DC[4]=0: 00b : 256 color mode 3R-3G-2B (8-bit/RGB) 01b : 4K color mode 4R-5G-3B (12-bit/RGB) 10b : 64K color mode 5R-6G-5B (16-bit/RGB) LC[9:8] : Partial Display Control **0xb: Disable** Mux-Rate = CEN+1 (DST, DEN not used) 10b: Enabled Mux-Rate = CEN+1 11b: Enabled Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2
NIV	7	51H	N-Line Inversion: NIV[5:0] : 00000b: Disable 00001b ~ 111111b: 1~ 63 lines (Default: **17lines**) NIV[6] : 0b: no-XOR **1b: XOR**
CSF	3	0H	COM Scan Function CSF[0] : **0b : LRM sequence: AEBCD-AEBCD** 1b : LRM sequence: AEBCD-EBCDA CSF[1] : **0b :FRC Disable** 1b : FRC Enable CSF[2] : Shade-1 / Shade-30 option **0 : Dither directly on input data (SRAM Change)** 1 : PWM on SEG output stage

Name	Bits	Default	Description
CEN DST DEN	7 7 7	7FH 00H 7FH	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ⩾ DEN ⩾ DST+ 9
WPC0	7	00H	Window program starting column address. Value range: 0 ~127.
WPP0	7	00H	Window program starting row address. Value range: 0~127.
WPC1	7	7FH	Window program ending column address. Value range: 0~127.
WPP1	7	7FH	Window program ending row address. Value range: 0~127.
MTPC	5	10H	MTP Programming Control: MTPC[2:0] : MTP command **000** : **Idle** 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip's debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. 0: Ignore **1: Use**
MTP	6	--	Multiple-Time Programming. For V_{LCD} fine tune.
MTPM	6	00H	MTP Write Mask. Bit =1: program, Bit=0: no action.
APC	2	N/A	Advanced Program Control. For UltraChip only. Please do not use.
Status Registers			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	–	MTP option flag: 1 for MTP version, 0 for non-MTP version.
MS	1	–	MTP programming in-progress
WS	1	–	MTP Operation Succeeded
ID	2	PIN	Access the connected status of ID pins.

COMMAND TABLE

The following is a list of host commands supported by UC1697v

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
#: Useful Data bits –: Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	N/A Product Code (5h)
				Ver	PMO[6:0]								
				Product Code				PID[2:0]		0	0		
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	1xb
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0], R = 0, 1, or 2	N/A
		0	0	#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	0	#	#	#	Set SL[6:4]	0
10	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	0	#	#	#	Set RA[6:4]	0
11	Set V_{BIAS} Potentiometer (double-byte command)	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set PM[7:0]	5CH
12	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	0xH
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0 0	0 0	1 #	0 #	0 #	1 #	0 #	0 #	0 #	0 #	Set {FLT, FLB}	0
15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
18	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
19	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
20	Set N-Line Inversion	0	0	1 -	1 #	0 #	0 #	1 #	0 #	0 #	0 #	Set NIV[6:0]	51H
21	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
22	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
23	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b
24	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
25	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
26	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
27	Set LCD Bias Ratio	0	0	1	1	1	0	1	#	#	#	Set BR[2:0]	011b: 12
28	Set COM End	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	0 #	1 #	Set CEN[6:0]	127
29	Set Partial Display Start	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	0 #	Set DST[6:0]	0
30	Set Partial Display End	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	1 #	Set DEN[6:0]	127
31	Set Window Program Starting Column Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with MTP Commands	Set WPC0 — 0
32	Set Window Program Starting Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set WPP0 — 0
33	Set Window Program Ending Column Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set WPC1 — 127
34	Set Window Program Ending Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set WPP1 — 127
35	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Inside
36	Set MTP Operation control	0 0	0 0	1 -	0 -	1 -	1 #	1 #	0 #	0 #	0 #	Set MTPC[4:0]	10H
37	Set MTP Write Mask	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	1 #	Set MTPM[5:0]	0

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
38	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Program commands	Set MTP1	N/A
39	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	N/A
40	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	N/A
41	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	N/A

NOTE:

- All bit patterns other than commands listed above, may result in undefined behavior.
- The interpretation of commands (37)~(41) depends on the setting of register MTPC[3].
  - Commands (38)~(41) are shared with commands (31)~(34). These two sets of commands share exactly the same code and control registers. When MTPC[3]=0, they are interpreted as Window Program commands and registers. When MTPC[3]=1, they function as MTP Control commands and registers.
- After MTP ERASE or PROGRAM operation, before resuming normal operation, please always
  a) Remove TST4 power source,
  b) Do a full V_{DD} ON-OFF-ON cycle.
- Under 16-bit bus mode and CD=0, D[15:8] is ignored and only D[7:0] is used. As a result, the bus cycles for commands under 16-bit bus and 8-bit bus are the same, and double-byte commands still need two bus cycles under 16-bit bus mode.

  Example:

  8-bit bus mode:

  Set PL[1:0] = 2'b11 : D[7:0] = 0010 1011

  Set PM[7:0] = 8'h8b : 1st D[7:0] = 1000 0001

  2nd D[7:0] = 1000 1011

  16-bit bus mode:

  Set PL[1:0] = 2'b11: D[15:0] = 0000 0000 0010 1011

  Set PM[7:0] = 8'h8b: 1st D[15:0] = 0000 0000 1000 0001

  2nd D[15:0] = 0000 0000 1000 1011

COMMAND DESCRIPTION

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit data write to SRAM							

UC1697v will convert input RAM data to 16-bit of RGB data. Please refer to command *Set Color Mode* for detail of data-write sequence.

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit data from SRAM							

Each RGB triplet is stored as 16-bit in the display RAM. Each 16-bit of RGB data takes 1 / 2 RAM read cycles for 16 / 8 – bit bus mode, respectively. The read out RGB data is *after-extension* for 64K color mode.

R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
1st 8-bit Read								2nd 8-bit Read							

Write/Read Data Byte (command (1) / (2)) operation uses internal Row Address register (RA) and Column Address register (CA). RA and CA can be programmed by issuing commands `Set Row Address` and `Set Column Address`. If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the CA boundary, and system programmers need to set the values of RA and CA explicitly. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and RA will be increased or decreased, depending on the setting of Row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 127), RA will be wrapped around to the other end of RAM and continue.

(3) GET STATUS & PM

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS
	0	1	Ver		PMO[5:0]					
	0	1	Product Code				PID[2:0]		0	0

Status1 definitions:
- *GE*: Green Enhancing enable flag. Green Enhance Mode is disabled when GE = 1.
- *MX*: Status of register LC[1], mirror X.
- *MY*: Status of register LC[2], mirror Y.
- *WA:* Status of register AC[0]. Automatic column/row wrap around.
- *DE*: Display enable flag. DE=1 when display is enabled
- *WS*: MTP Operation succeeded
- *MD*: MTP Option (1 for MTP version, 0 for non-MTP version)
- *MS*: MTP action status

Status2 definitions:
- *Ver:* Version Code. 00 ~ 11.
- *PMO[5:0]:* PM offset value.

Status3 definitions:
- *Product Code*: 1110b (Eh)
- *PID[1:0]:* Provide access to ID pins connection status.

If multiple `Get Status` commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[6:4]	0	0	**0**	**0**	**0**	**1**	**0**	CA6	CA5	CA4

Set SRAM column address for read/write access. CA is counted in RGB triplets, not individual SEG electrode.

CA value range: **0~127**

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:
00b = -0.00%/°C 01b = -0.10%/°C 10b = -0.15%/°C 11b = -0.05%/°C

(6) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition:
0xb: LCD: ≤ 13nF **1xb: LCD: 13~22nF**

(7) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages. Always make sure the IC is in a RESET state before changing PC[3:2] value. Avoid changing PC[3:2] setting when the display is enabled.

Pump control definition:
00b = External V_{LCD} **11b = Internal V_{LCD} (x10)**

(8) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R][7:0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	R	R
(Double-byte command)	0	0	APC register parameter							

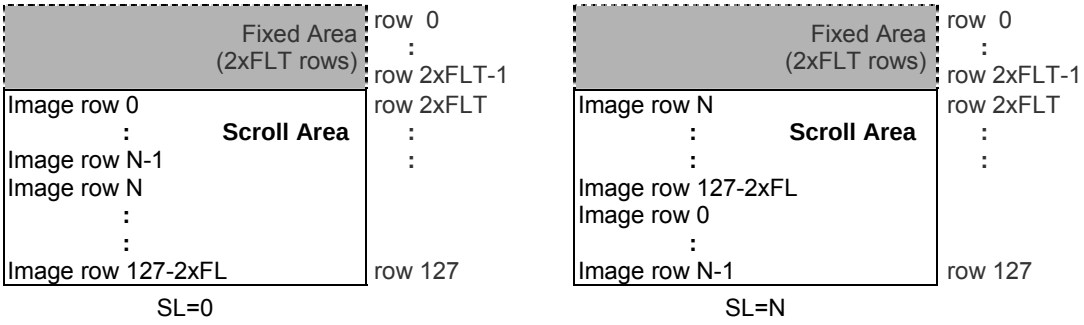
For UltraChip only. Please do NOT use.

(9) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	**0**	**1**	**0**	**1**	**0**	SL6	SL5	SL4

Set the number of lines for scroll area.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 127-2x(FLT+FLB) (full scrolling). FLT and FLB are the register values programmed by the `Set Fixed Lines` command.



(10) SET ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address LSB RA [3:0]	0	0	**0**	**1**	**1**	**0**	RA3	RA2	RA1	RA0
Set Row Address MSB RA [6:4]	0	0	**0**	**1**	**1**	**1**	**0**	RA6	RA5	RA4

Set SRAM row address for read/write access.

Possible value = **0~127**

(11) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0] (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section *LCD Voltage Setting* for more detail.

Effective range: **0 ~ 255**

(12) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [9:8]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	LC9	LC8

This command is used to enable partial display function.

LC[9:8] : **0x**b: Disable Partial Display, Mux-Rate = CEN+1 (DST, DEN not used.)
10b: Enable Partial Display, Mux-Rate = CEN+1
11b: Enable Partial Display, Mux-Rate = DEN-DST+1+ LC[0]x(FLT+FLB)x2

(13) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/row wrap around.
0: CA or RA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increment by one step.

AC[1]: Auto-Increment order
0 : column (CA) increment (+1) first until CA reaches CA boundary, then RA will increment by (+/-1).
1 : row (RA) increment (+/-1) first until RA reach RA boundary, then CA will increment by (+1).

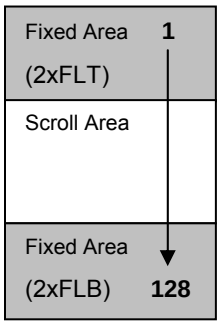
AC[2]: RID, row address (RA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, RID controls whether row address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. For Window Program enabling (AC[3]=ON), see section *Command Description* (34) ~ (37) for more details. If WPC[1:0] and WPP[1:0] values are the default values, the behavior of CA, RA auto-increment will be the same, no matter what the setting of AC[3] is.

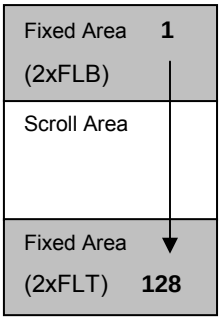
(14) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT, FLB}	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
(Double-byte command)	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. The `Set Fixed Lines` command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT and bottom 2xFLB rows for mirror Y (MY) is 0, or covers the top 2xFLB and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0



MY = 1

When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], please make sure

MY=0 DST ⩾ FLTx2
DEN ⩽ (CEN-FLBx2).

MY=1 DST ⩾ FLBx2
DEN ⩽ (CEN-FLTx2)

(15) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 87, 65, 44 and 33.

The following are line rates at Mux Rate = 88 ~ 128.

00b: 20.1 Klps 01b: 24.4 Klps **10b: 29.6 Klps** 11b: 35.8 Klps

In On/Off Mode

00b: 5.5 Klps 01b: 6.6 Klps **10b: 8.0 Klps** 11b: 9.7 Klps

(Klps: Kilo-Line-per-second)

(16) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(17) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

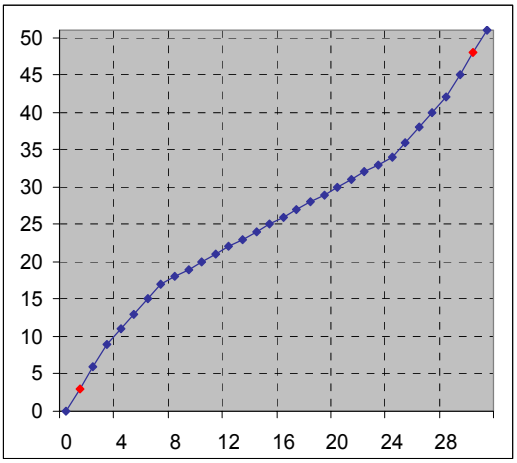
(18) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [4:2]	0	0	**1**	**0**	**1**	**0**	**1**	DC4	DC3	DC2

This command is for programming register DC[4:2].

When DC[2] is set to **0**, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1697v will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3] controls the gray shade modulation modes. UC1697v has two gray shade modulation modes: an On/Off mode and a 32-shade mode. The modulation curves are shown below. Horizontal axes are the gray shade data. The vertical axes are the ON-OFF ratio.



DC[4] Green Enhance Mode. Refer to command `Set Color Mode` for more information.

0b: Green Enhancing Mode enabled **1b: Green Enhancing Mode disabled**

NOTE:

1. For red and blue colors, shades mapped to data 1 and 30 (shown as red points above) are achieved by special dithering. This will be solved when the PWM function is enabled.
2. Green shades are created by combining FRC and special dithering. Six of the shades (1, 2, 3, 59, 60, and 61) are created by special dithering. This will be solved when the PWM function is enabled. Data 62 and 63 are mapped to the same shade.
3. When the internal DC-DC converter starts to operate and pump out current to V_{LCD}, there will be an in-rush pulse current between V_{DD2} and V_{SS2} initially. To avoid this current pulse from causing potential harmful noise, do *NOT* issue any command or write any data to UC1697v for 5~10mS after setting DC[2] to 1.

(19) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	LC0

This command is used for programming LC[2:0] to control COM (row) mirror (MY), SEG (column) mirror (MX).

LC[2] controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by the MY action. MY will have immediate effect on the display image.

LC[1] controls Mirror X (MX): MX is implemented by selecting the CA or 127-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

LC[0] controls whether soft icon sections (2xFLT, 2xFLB) are displayed during partial display mode.

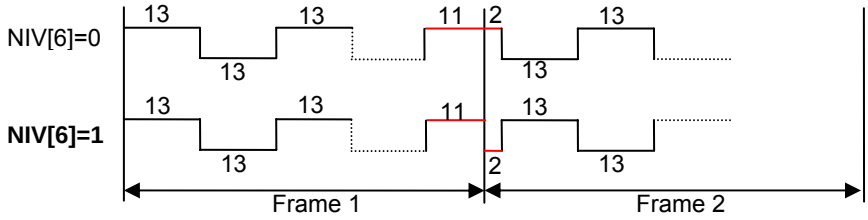
(20) SET N-LINE INVERSION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-line Inversion, NIV[4:0]	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
(Double-byte command)	0	0	**-**	NIV6	NIV5	NIV4	NIV3	NIV2	NIV1	NIV0

N-Line Inversion:

NIV[5:0]: 000000b: Disable
000001b ~ 111111b: 1~63 lines (**Default : 17 lines**)

NIV[6]: 0b: non-XOR **1b: XOR**



(21) SET COLOR PATTERN

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Pattern LC [5]	0	0	**1**	**1**	**0**	**1**	**0**	**0**	**0**	LC5

UC1697v supports on-chip swapping of R⇔B data mapping to the SEG drivers.

LC[5]	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	…	SEG388	SEG389	SEG390
0	B	G	R	B	G	R	…	B	G	R
1	R	G	B	R	G	B	…	R	G	B

The definition of R/G/B input data is determined by LC[7:6], as described in *`Set Color Mode`* below.

(22) SET COLOR MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mode LC [7:6]	0	0	**1**	**1**	**0**	**1**	**0**	**1**	LC7	LC6

Program color mode and RGB input pattern. Color mode (LC[7:6]) definition:

Note: *For serial bus modes, please refer to 8-bit tables below.*

Green Enhance Mode disabled (**DC[4] = 1**):

LC[7:6] = 00b (RRR-GGG-BB, 256-color)
8 bits of input RGB data are stored to 16 RAM bits. No dither is performed.

Data Write Sequence (8-bit)	***D[7:0]***
1st Write Data Cycle	R2 R1 R0 G2 G1 G0 B1 B0

Data Write Sequence (16-bit)	***D[15:0]***
1st Write Data Cycle	0 0 0 0 0 0 0 0 R2 R1 R0 G2 G1 G0 B1 B0

LC[7:6] = 01b (RRRR-GGGG-BBBB, 4K-color)
12 bits of input RGB data are stored to 16 RAM bits. No dither is performed. Every 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence (8-bit)	***D[7:0]***
1st Write Data Cycle	R3 R2 R1 R0 G3 G2 G1 G0
2nd Write Data Cycle	B3 B2 B1 B0 R3 R2 R1 R0
3rd Write Data Cycle	G3 G2 G1 G0 B3 B2 B1 B0

Data Write Sequence (16-bit)	***D[15:0]***
1st Write Data Cycle	0 0 0 0 R3 R2 R1 R0 G3 G2 G1 G0 B3 B2 B1 B0
2nd Write Data Cycle	0 0 0 0 R3 R2 R1 R0 G3 G2 G1 G0 B3 B2 B1 B0

LC[7:6] = **10b** (RRRRR-GGGGGG-BBBBB, 64K-color)
16 bits of input data are stored to 16 RAM bits directly.

Data Write Sequence (8-bit)	***D[7:0]***
1st Write Data Cycle	R4 R3 R2 R1 R0 G5 G4 G3
2nd Write Data Cycle	G2 G1 G0 B4 B3 B2 B1 B0

Data Write Sequence (16-bit)	***D[15:0]***
1st Write Data Cycle	R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0 B4 B3 B2 B1 B0

Green Enhance Mode enabled (DC[4]=0):

LC[7:6] = 00b (RRR-GGG-BB, 256-color)

8 bits of input RGB data are stored to 16 RAM bits. No dither is performed.

Data Write Sequence (8-bit)	***D[7:0]***
1st Write Data Cycle	R2 R1 R0 G2 G1 G0 B1 B0

Data Write Sequence (16-bit)	***D[15:0]***
1st Write Data Cycle	0 0 0 0 0 0 0 0 R2 R1 R0 G2 G1 G0 B1 B0

LC[7:6] = 01b (RRRR-GGGGG-BBB, 4K-color)

12 bits of input data are extended and stored to 16 RAM bits. Every 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence (8-bit)	***D[7:0]***
1st Write Data Cycle	R3 R2 R1 R0 G4 G3 G2 G1
2nd Write Data Cycle	G0 B2 B1 B0 R3 R2 R1 R0
3rd Write Data Cycle	G4 G3 G2 G1 G0 B2 B1 B0

Data Write Sequence (16-bit)	***D[15:0]***
1st Write Data Cycle	0 0 0 0 R3 R2 R1 R0 G4 G3 G2 G1 G0 B2 B1 B0
2nd Write Data Cycle	0 0 0 0 R3 R2 R1 R0 G4 G3 G2 G1 G0 B2 B1 B0

LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color)

The behaviors of 8-bit input mode and 16-bit input mode do not change with DC[4] setting. Refer to previous section for more information on these two input modes.

(23) SET COM SCAN FUNCTION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set COM Scan Function CSF[2:0]	0	0	**1**	**1**	**0**	**1**	**1**	CSF2	CSF1	CSF0

COM scan function

CSF[0]: LRM sequence option

0b: LRM sequence: AEBCD-AEBCD

1b : LRM sequence: AEBC-EBCDA

CSF[1]: FRC option

0b: FRC Disable

1b: FRC Enable

CSF[2]: Shade-1, Shade-30 option

0 : Dither directly on input data(SRAM Change)

1 : PWM on SEG output stage

(24) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(25) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

(26) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	TT	
(Double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Do *NOT* use.

(27) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [2:0]	0	0	**1**	**1**	**1**	**0**	**1**	BR2	BR1	BR0

Bias ratio definition:

000b = 6 001b = 10 010b = 11 **011b = 12**
100b = 9

(28) SET COM END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN [6:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(Double-byte command)	0	0	**-**	*CEN* register parameter						

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 128 pixel rows, the LCM designer should set CEN to *N-1* (where *N* is the number of pixel rows) and use COM1 through COM-*N* as COM driver electrodes.

(29) SET PARTIAL DISPLAY START

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST [6:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(Double-byte command)	0	0	**-**	*DST* register parameter						

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

(30) SET PARTIAL DISPLAY END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN [6:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(Double-byte command)	0	0	**-**	*DEN* register parameter						

This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based indexes of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

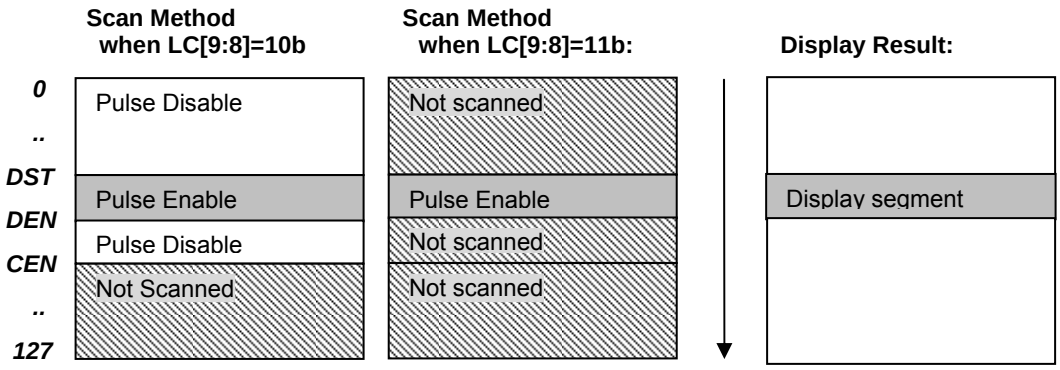
When LC[9]=1, two partial display modes are possible with UC1697v:
LC[8]=1: ON-OFF only, ultra-low-power mode (if Mux-Rate ⩽ 33, set BR=6).
LC[8]=0: Full gray shade low power mode (BR and PM stays the same)

When LC[9:8]=10b, the Mux-Rate is still CEN+1. This is achieved by suppressing only the scanning pulses, but not the scanning time slots, for COM electrodes that is outside of DST~DEN. Under this mode, the gray-scale quality of the display is preserved, while the power can be reduced significantly.

When LC[9:8]=11b, the Mux-Rate is narrowed down DEN-DST +1 + 2x(FLT+FLB)xLC[0]. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also require BR and V_{LCD} to be readjusted. When Mux-Rate is under 33, it is recommend to set BR=6.

For minimum power consumption, set LC[9:8]=11b, set (DST, DEN, FL, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use On-Off mode, set PC[1:0]=00b, and use lowest BR, lowest V_{LCD} which satisfies the contrast requirement.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(31) SET WINDOW PROGRAM STARTING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 [6:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	**-**	*WPC0* register parameter						

This command is to program the starting column address of RAM program window.

(32) SET WINDOW PROGRAM STARTING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 [6:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	**-**	*WPP0* register parameter						

This command is to program the starting row address of RAM program window.

(33) SET WINDOW PROGRAM ENDING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 [6:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	**-**	*WPC1* register parameter						

This command is to program the ending column address of RAM program window.

(34) SET WINDOW PROGRAM ENDING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 [6:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	**-**	*WPP1* register parameter						

This command is to program the ending row address of RAM program window.

(35) SET WINDOW PROGRAM MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	AC3

This command controls the Window Program function.

AC[3]=0: Inside Mode

When Window Programming is under “Inside” mode , the CA and RA increment and wrap-around will be performed automatically around the boundaries as defined by registers WPC0, WPC1, WPP0, and WPP1, so that the CA/RA address will stay ***within*** the defined window of SRAM address, and therefore allow effective data update within the window.

AC[3]=1: Outside Mode

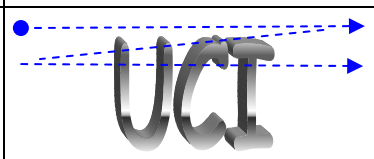
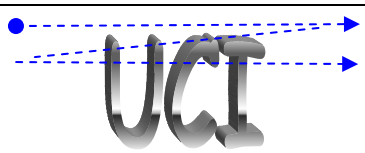
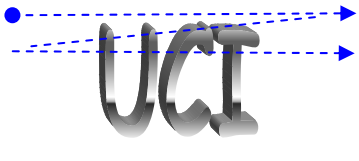
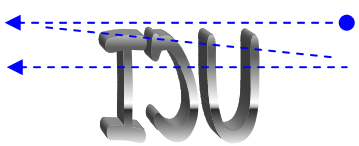
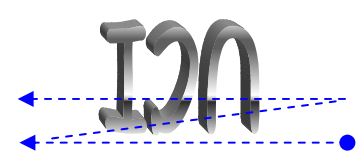
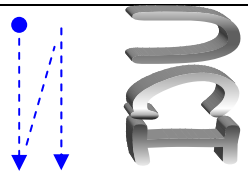
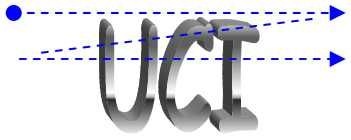
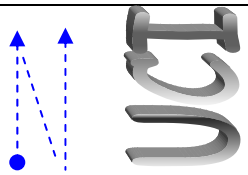
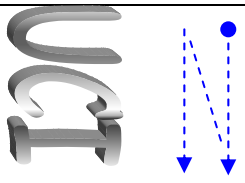
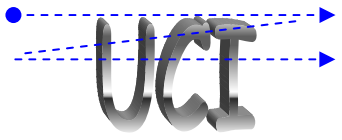
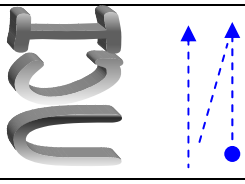
When Window Programming is under “Outside” mode, the CA and RA increment and wrap-around boundary will cover the entire UC1697v SRAM map (CA: 0~127, RA:0~127). However, when CA/RA points to a memory location within the window defined by registers WPC0, WPC1, WPP0, and WPP1, the SRAM data update operation will be suspended, the existing data will be retained and the input data will be ignored.

The direction of Window Program will depend on the WA (AC[0]), RID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting.

- WA decides whether the program RAM address advances to next row/column after reaching the specified window column / row boundary.
- RID controls the RAM address incrementing from WPP0 toward WPP1 (RID=0) or reverse the direction (RID=1).
- Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0).
- MX results the RAM column address incrementing from 127-WPC0 to 127-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

By different combination of RID, AC[1], MX, and by setting CA, RA at proper corners of the “window”, effects such as mirrors and rotations can be easily achieved.

Setting or resetting AC[3] does not affect the values of CA and RA. So, always remember to reposition CA and RA properly after changing the setting of AC[3].

Display Data Direction	Function Setting			Image in the Host (MPU) (Start :	Image in Display Data Ram (Physical origin: upper left corner)
	AIO AC[1]	MX LC[1]	RID AC[2]		
Normal	0	0	0		
Y-mirror	0	0	1		
X-mirror	0	1	0		
X-mirror Y-mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-mirror	1	0	1		
X-Y Exchange X-mirror	1	1	0		
X-Y Exchange X-mirror Y-mirror	1	1	1		

(36) SET MTP OPERATION CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC [4:0] (Double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**
	0	0	**-**	**-**	**-**	*MTPC* register parameter				

This command is for MTP operation control:

MTPC[2:0] : MTP command

000 : Sleep
001 : MTP Read
010 : MTP Erase
011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (ignore MTP value when L)

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

The following commands, (37) ~ (41), are used as MTP commands only when MTPC[3]=1.

(37) SET MTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM [6:0] (Triple-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**
	0	0	**-**	MTPM register parameter						

This command enables Write to each of the 7 individual MTP bits.

When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to "1". MTPM[x]=0 means no Write action for x-th bit. And the content of this bit will not change.

The amount of "programming current" increases with the number of 1's in MTPM. If the "programming current" appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1's evenly into these cycles.

MTPM[6:0] : Set PMO value
MTPM1[1:0]: Set MID value

This command is only valid when MTPC[3]=1.

(38) SET V_{MTP1} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP1 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	Shared register parameter							

This command is for fine tuning V_{OPT1} setting (use with BR=000) and is only valid when MTPC[3]=1.

(39) SET V_{MTP2} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP2 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	Shared register parameter							

This command is for fine tuning V_{MTP2} PM setting (use with BR=001) and is only valid when MTPC[3]=1.

(40) SET MTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP3 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

(41) SET MTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP4 (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1697v via registers CEN, DST, DEN, FLT, FLB, and partial display control flags LC[9:8] and LC[0].

Combined with low power partial display mode and a low bias ratio of 6, UC1697v can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD}/V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=128), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally can not maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1697v supports five *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3	4
Bias Ratio	6	10	11	12	9

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per ^{o}C	-0.00	-0.10	-0.15	-0.05

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\,\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} AND CONTRAST FINE TUNING

Color STN LCD is sensitive to even a 0.5% mismatch between IC driving voltage and the V_{OP} of LCD. It is very difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to precisely match the actual V_{OP} of each LCD.

For the best results, software or MTP based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH FOR COG

The power supply circuit of UC1697v is designed to handle LCD panels with loading up to ~16nF using 7-Ω/Sq ITO glass with $V_{DD2/3} \geqslant 2.8V$. For larger LCD panels, use lower resistance ITO glass.

Due to crosstalk consideration, ~16nF is also the recommended maximum LCD panel loading for COG applications. Using 4.5-Ω/Sq low resistance ITO glass for the IC bonding substrate can help improve image quality and operation tolerance.

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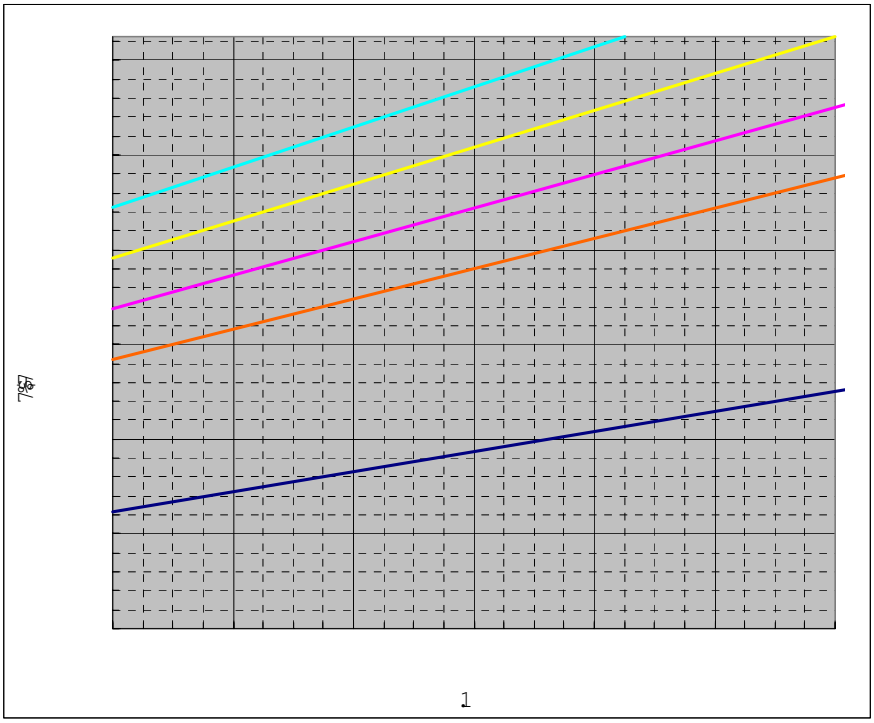
V_{LCD} QUICK REFERENCE



BR	C_{V0} (V)	C_{PM} (mV)	PM_reg	V_{LCD} (V)
6	6.402	13.14	0	6.40
			255	9.75
10	10.670	21.90	0	10.67
			255	16.25
11	11.737	24.09	0	11.74
			198	16.51
12	12.804	26.28	0	12.80
			141	16.51
9	9.603	19.71	0	9.60
			255	14.63

V_{LCD}-PM-BR relationship at 25°C

NOTE:

1. For good product reliability, please keep V_{LCD} under **16.5V** over all temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR REFERENCE CIRCUIT

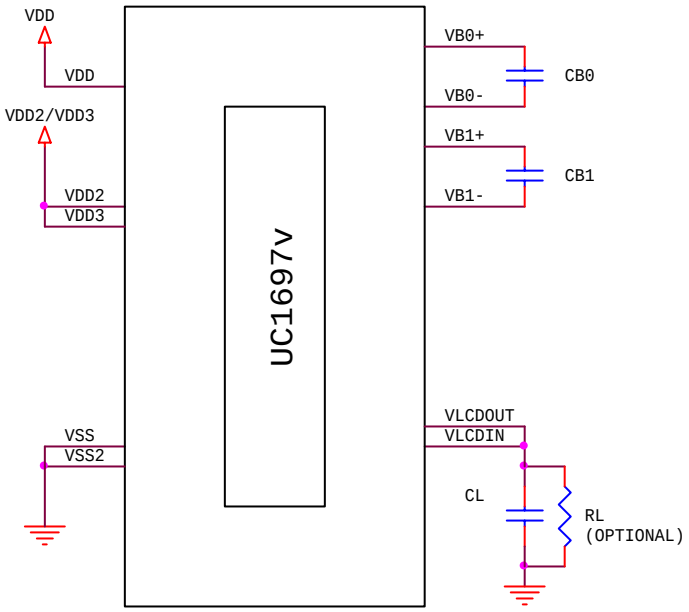


FIGURE 1: Sample circuit using internal Hi-V generator circuit

NOTE:
Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

$C_{B0\sim1}$: 2.2 μF/5V or 300 x LCD load capacitance, whichever is higher.

C_L : 330 nF (25V) is appropriate for most applications.

R_L : 3.3~10 MΩ to act as a draining circuit when V_{DD} is shut down abruptly

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1697v contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 88, frame rate is calculated as:

Line-Rate = Frame Rate x Mux-Rate.

When Mux-Rate is lowered to 87, 65, 44 and 33, line rate will be scaled down automatically by 1.5, 2, 3 and 4 times to reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Line rate 30 Klps or higher is recommended for 32-shade mode. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When switching from 32-shade modulation to On/Off mode, line rate will be scaled down automatically by ~30% to reduce power.

Under most situations, flicker behavior is similar between these two modulation schemes. However, it is recommended to test each mode to make sure the result is as expected.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG drivers are in Idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming convention is COM(*X*), where *X* =1~128, referring to the COM driver for the *X*-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via the `Set Display Enable` command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1697v will put itself into Sleep mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1697v will first exit from Sleep mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FLT and FLB specify two regions of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. FLT and FLB registers can be used to implement fixed regions when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1697v provides flexible control of Mux Rate and active display area. Please refer to commands `Set COM End`, `Set Partial Display Start`, and `Set Partial Display End` for more detail.

GRAY-SHADE MODULATION MODE

UC1697v has two gray-shade modulation modes: 32-shade and On/Off mode.

The On/Off mode will consume roughly 40~45% less power than the 32-shade mode, and can be used for situations where power consumption is more critical than color fidelity.

Changing gray-shade modulation mode does not affect the content of SRAM display buffer, and the image data will remain the same after switching back and forth between On/Off mode and 32-shade mode.

INPUT COLOR FORMATS

UC1697v supports the following two different input color formats.

256C (8-bit/RGB): In this color mode, R/G/B will be extended and the input data will be converted into 3R-3G-2B format before they are stored to display RAM.

4KC (12-bit/RGB): In this color mode, R/G/B will be extended and the input data will be converted into 5R-6G-5B format before they are stored to display RAM.

64KC (16-bit/RGB): This is the native color mode. Data will be stored directly to on-chip SRAM in 5R-6G-5B (16-bit) format (except shade1 and shade30, which are achieved by special dithering. See command `Set Display Enable` for more details). This is the default input format mode.

Changing color mode does not affect the content already stored in the display buffer RAM. Users can mix several color modes together and switch among them in real time.

For example, the menu portion can be painted in 4K-color mode for fast update speed, and then switch to 64K-color mode, together with window programming function to effectively produce smooth graphics images.

ITO LAYOUT AND LC SELECTION

Since COM scanning pulses of UC1697v can be as short as 15μS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

COM TRACES

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase COM direction crosstalk.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 0.9\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} – RC_{MIN} | < 0.22\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

(Use worst case values for all calculations)

SEG TRACES

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase of SEG direction crosstalk.

For good image quality, please minimize SEG ITO trace resistance and limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.25\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / #_column, where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too high, image contrast and color saturation will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, visibility of shades will suffer, and crosstalk may increase sharply for medium shades.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics, and V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/128	1/12	8.95%	7.2%	6.4%
1/128	1/11	8.85%	7.1%	6.4%

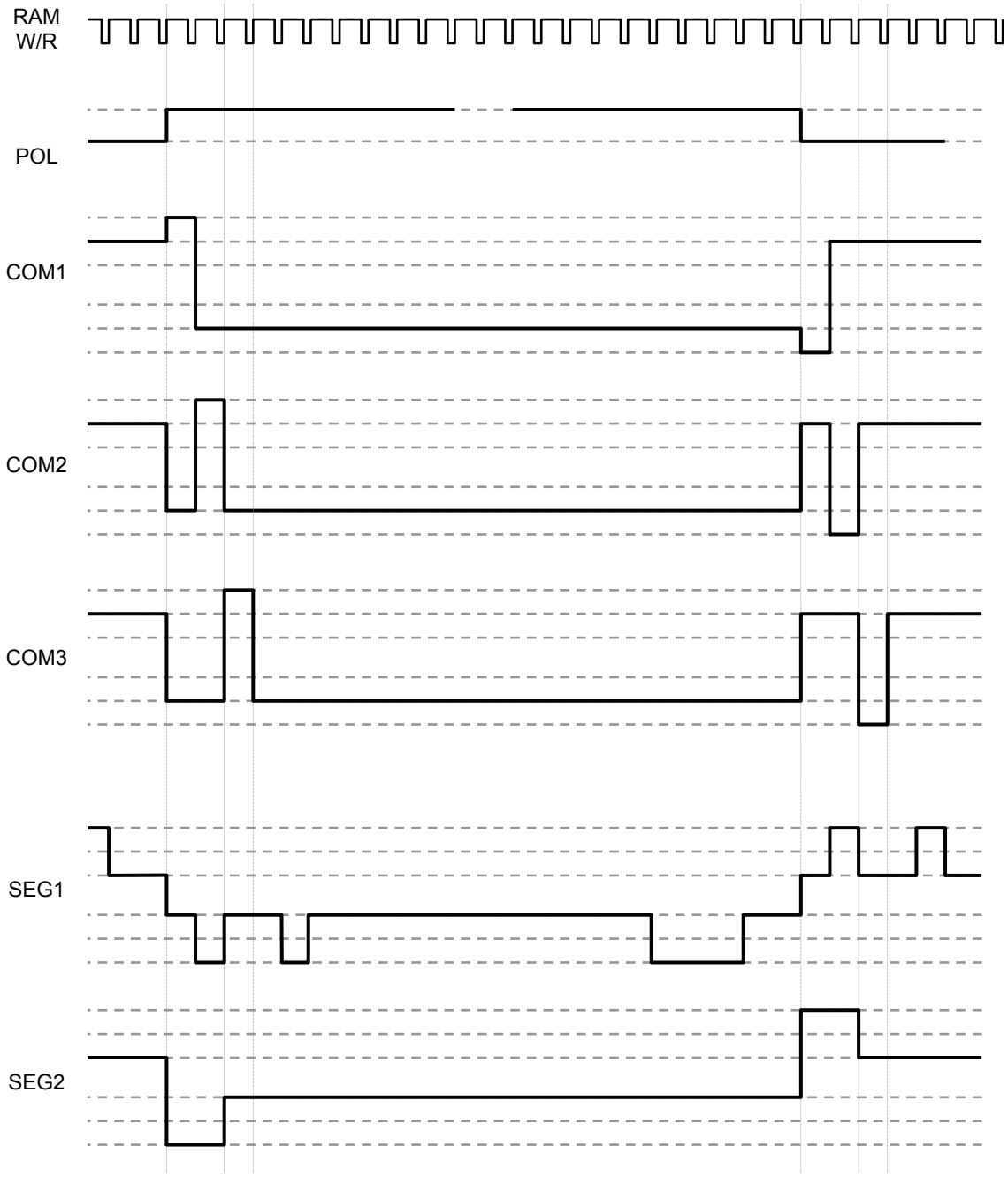


FIGURE 2: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1697v supports two parallel bus protocols, in either 8-bit or 16-bit bus width, and three serial bus protocols.

Designers can either use parallel buses to achieve high data transfer rate, or use serial buses to create compact LCD modules.

		Bus Type						
		8080		6800		S8 (4wr)	S8uc (3/4wr)	S9 (3 wr)
Width		16-bit	8-bit	16-bit	8-bit	Serial		
Access		Read/Write				Write Only		
Control & Data Pins	BM[1:0]	10	00	11	01	00	00	01
	{DB[15], DB[13]}	Data	0x	Data	0x	10	11	10
	CS[1:0]	Chip Select						
	CD	Control / Data						0
	WR0	$\overline{WR}$		R/$\overline{W}$		0		
	WR1	$\overline{RD}$		EN		0		
	DB[1,3,5,7,9,11]	Data	–	Data	–	–		
	DB[0,2,4,6,8,10,12,14]	Data	Data	Data	Data	DB[8]=SDA, DB[0]=SCK		

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

	CS Disable Interface	CS Init bus state	CD 1⇔0 Init bus state	CD 1⇨0 Init color mapping	RESET Init bus state	RESET Init color mapping
16-bit	✓	–	–	✓	✓	✓
8-bit	✓	–	–	✓	✓	✓
S8 or S9	✓	✓	–	✓	✓	✓
S8uc	✓	–	✓	✓	✓	✓

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- CD refers to CD transitions within valid CS window. CD = 0 means write command or read status.
- CS Sync / RESET can be used to initialize bus state machine (like 8-bit / S8 / S9).
- RESET can be pin reset / soft reset / power on reset.
- CD can be used to initialize the multi-byte input RGB format to/from on-chip SRAM mapping.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1697v internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in 8-bit mode or 16-bit mode, by either *Set CA,* or *Set RA* command, a dummy read cycle needs to be performed before the actual data can propagate through the pipe-line and be read from data port D.

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

16-BIT & 8-BIT BUS OPERATION

UC1697v supports both 8-bit and 16-bit bus width. The bus width is determined by pin BM[1].

8-bit bus operation exactly doubles the clock cycles of 16-bit bus operation, MSB followed by LSB, including the dummy read, which also requires two clock cycles. The bus cycle of 8-bit mode is reset each time CD pin changes state (when CS is active).

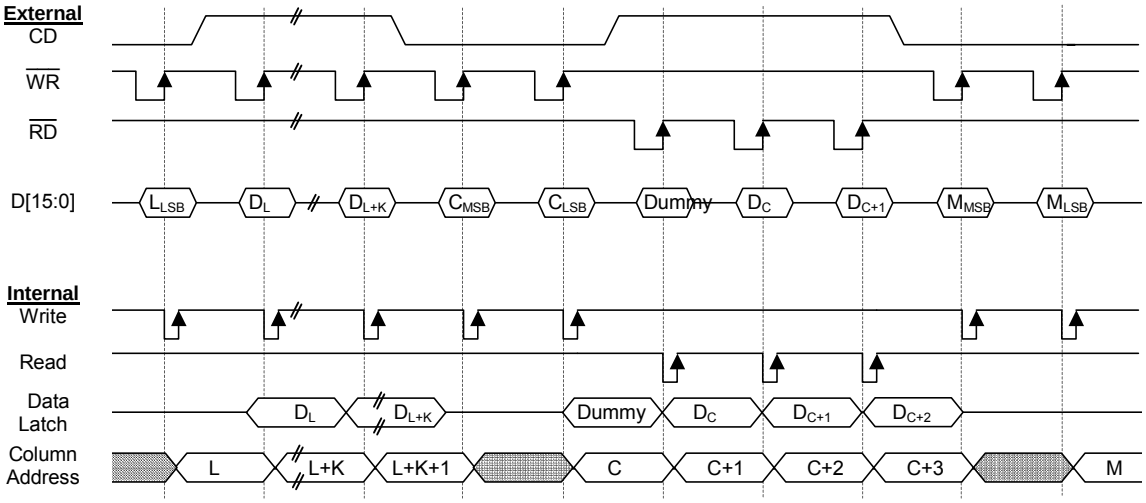


FIGURE 3: 16-bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1697v supports three serial modes, a 4-wire SPI mode (S8), a compact 3/4-wire mode (S8uc), and a 3-wire mode (S9). Bus interface mode is determined by the wiring of the BM[1:0], DB[15] and DB[13]. See table on last page for more detail.

S8 (4-WIRE) INTERFACE

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

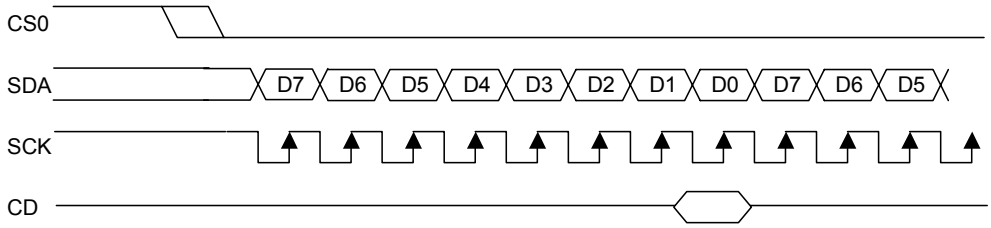


FIGURE 4.a: 4-wire Serial Interface (S8)

S8UC (3/4-WIRE) INTERFACE

Only write operations are supported in this 3/4-wire serial mode. The data format is identical to S8. The CD pin transitions will reset the bus cycle in this mode. So, if CS pins are hardwired to enable chip-select, the bus can work properly with only three signal pins.

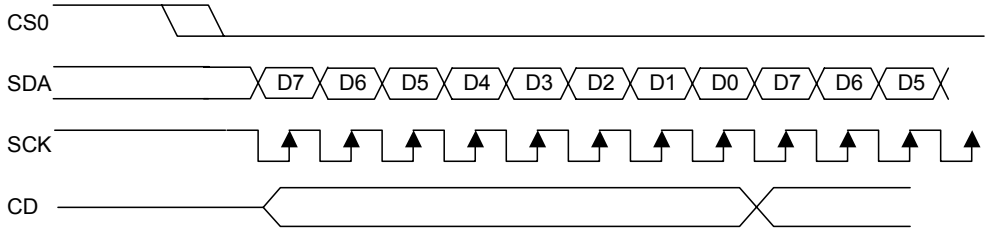


FIGURE 4.b: 3/4-wire Serial Interface (S8uc)

S9 (3-WIRE) INTERFACE

Only write operations are supported in this 3-wire serial mode. Pin CS[1-0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command/data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

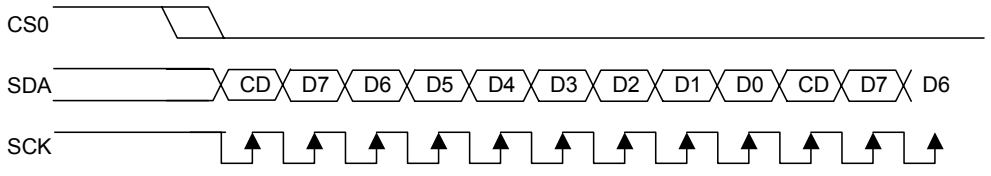


FIGURE 4.c: 3-wire Serial Interface (S9)

HOST INTERFACE REFERENCE CIRCUIT

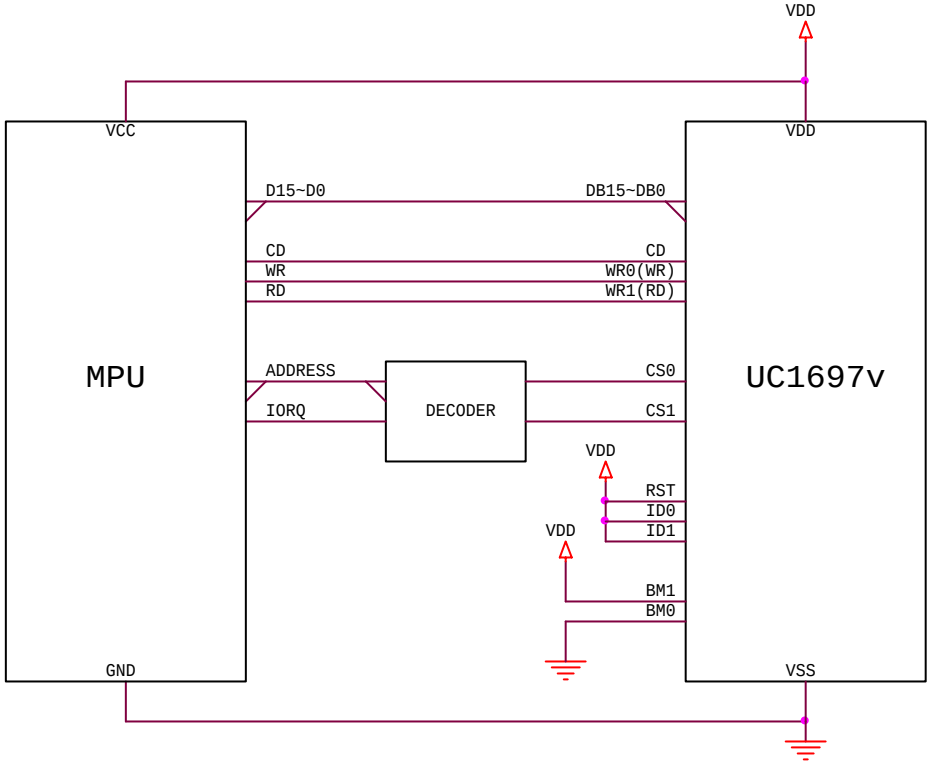


FIGURE 5: 8080/16-bit parallel mode example

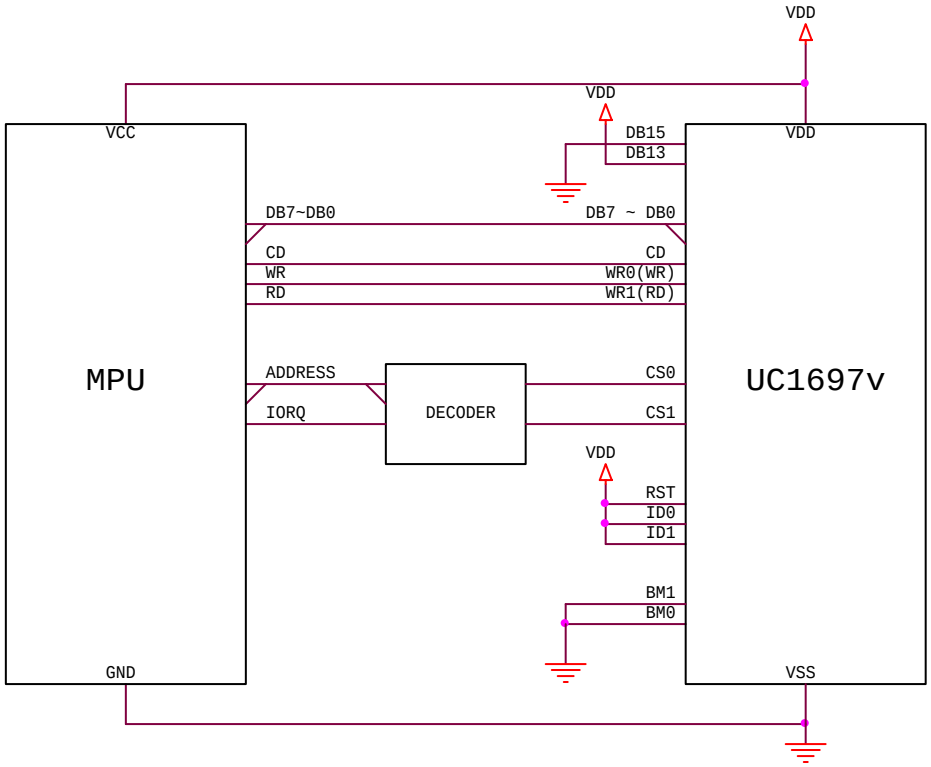


FIGURE 6: 8080/8-bit parallel mode example

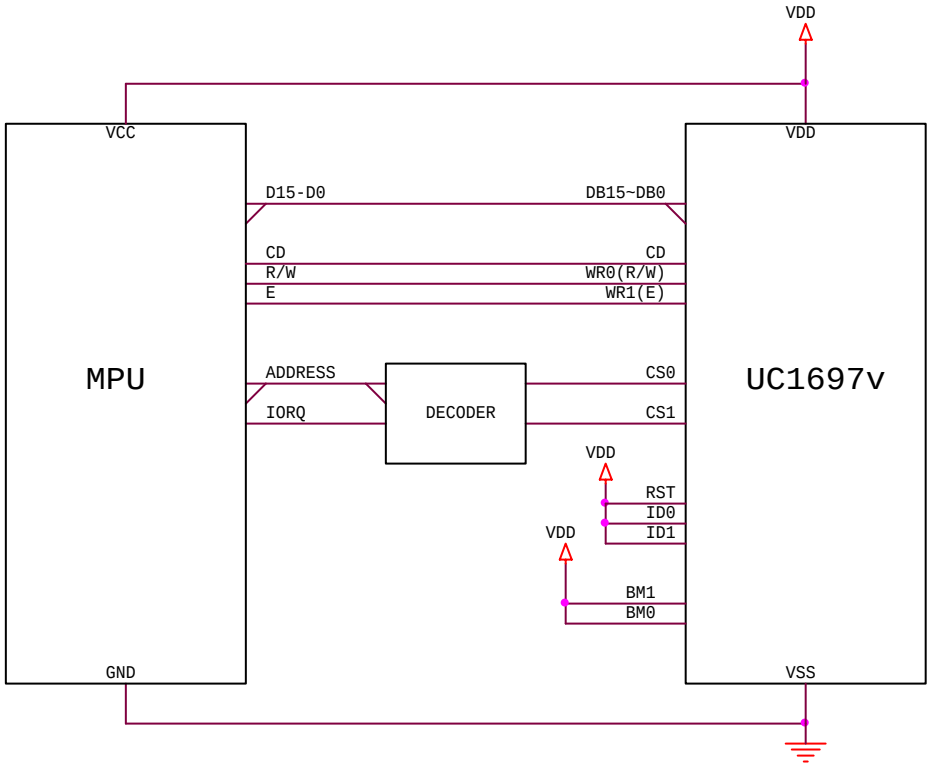


FIGURE 7: 6800/16-bit parallel mode example

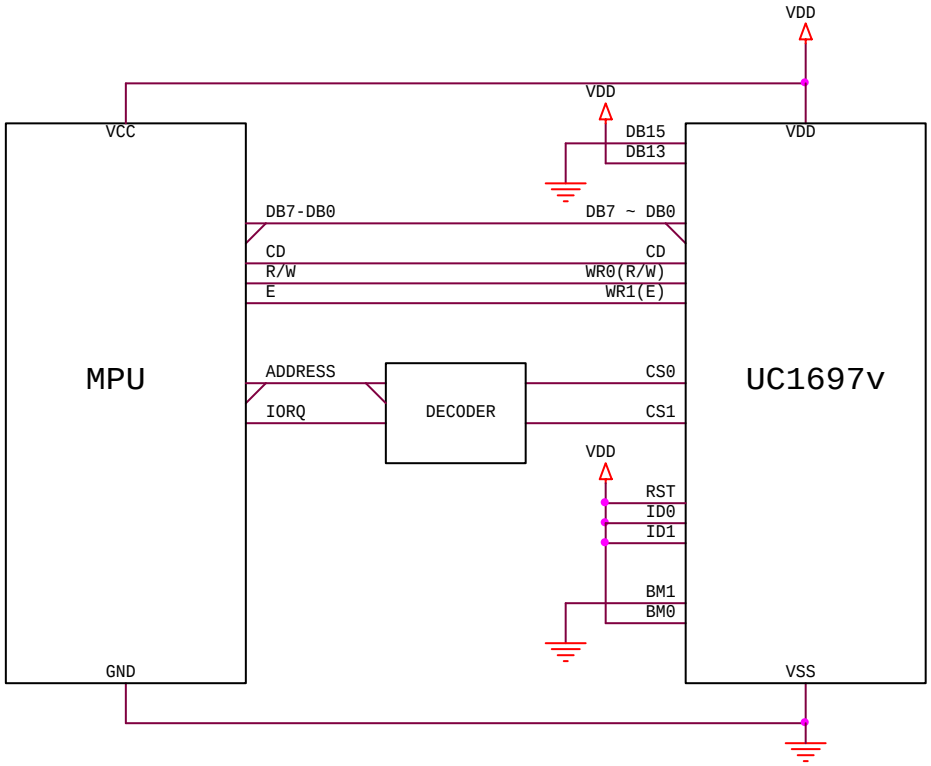


FIGURE 8: 6800/8-bit parallel mode example

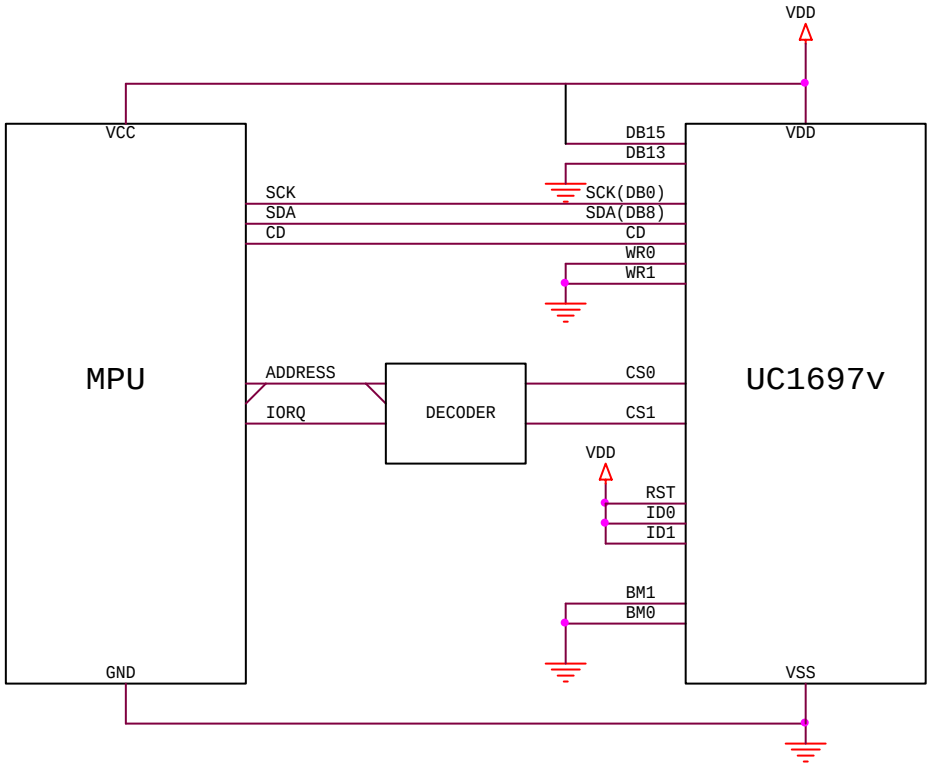


FIGURE 9: 4-Wires SPI (S8) serial mode example

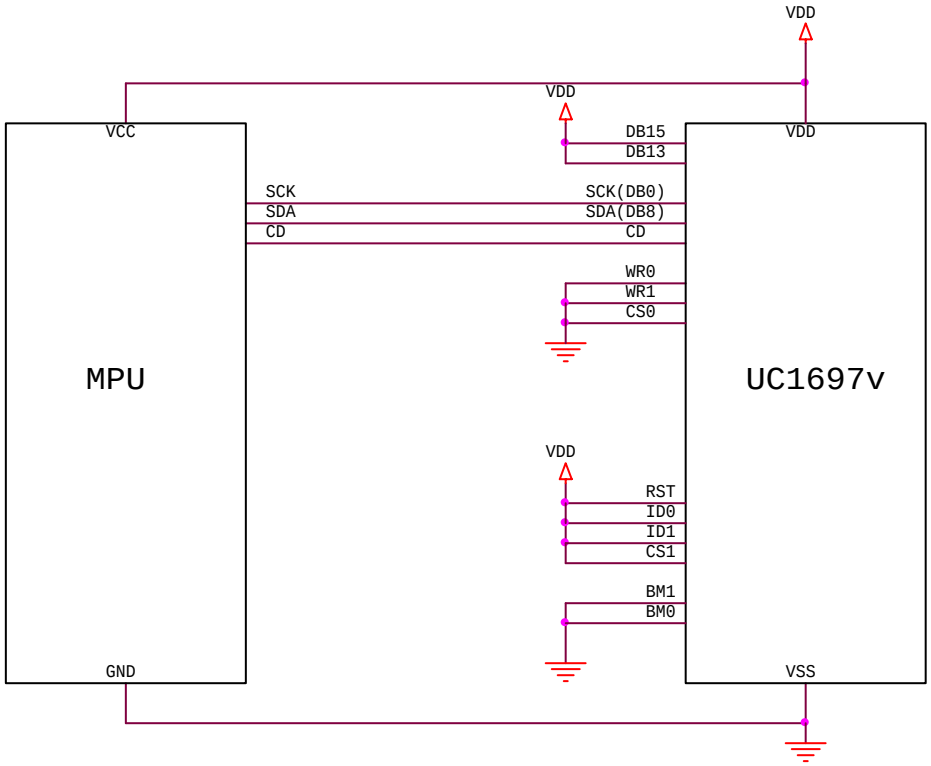


FIGURE 10: 3/4-Wires SPI (S8uc) serial mode example

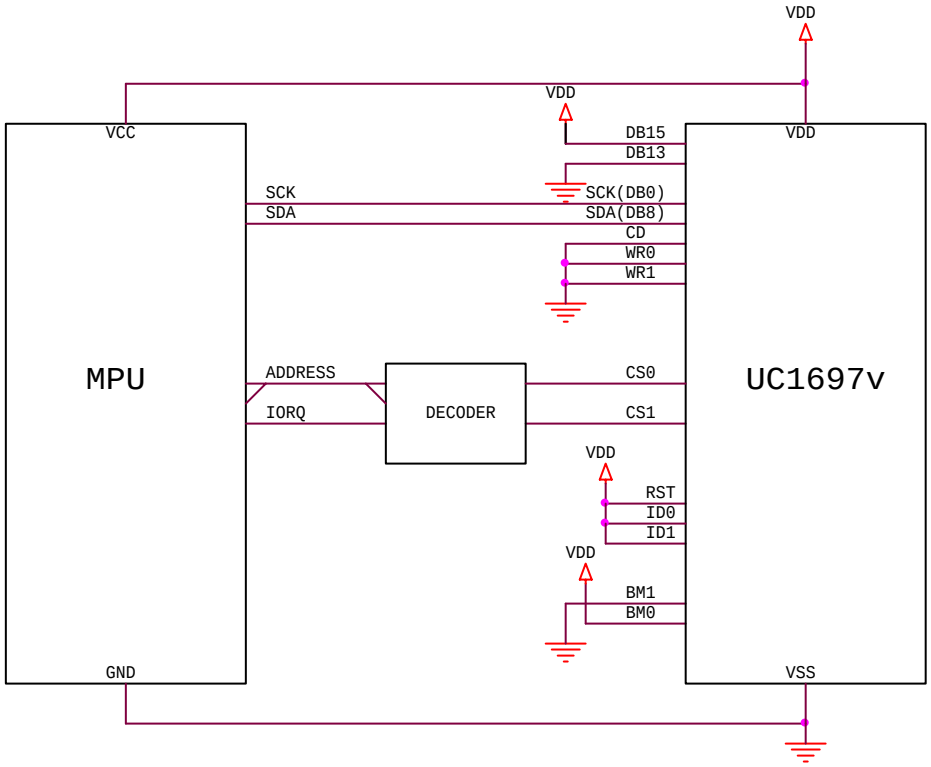


FIGURE 11: 3/4-Wires SPI (S9) serial mode example

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data (depend on color mode) are stored to a dual port static RAM (RAM, for Display Data RAM) organized as 128x128x16.

After setting CA and RA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *`Set Row Address`* and `Set Column Address` commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (127), and system programmers need to set the values of RA and CA explicitly.

If WA is ON (1), when CA reaches the end of a row, CA will be reset to 0 and RA will increment or decrement, depending on the setting of row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 127), RA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (127–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Scroll Line (SL), Fixed Line (FLT & FLB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FLT & FLB=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field

Line = *SL*

Otherwise

Line = Mod(*Line*+1, 128)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches 128. Effects such as scrolling can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field

Line = Mod(*SL* + *MUX-1*, 128)
where MUX = CEN + 1

Otherwise

Line = Mod(*Line-1*, 128)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM are not affected by MY.

WINDOW PROGRAM

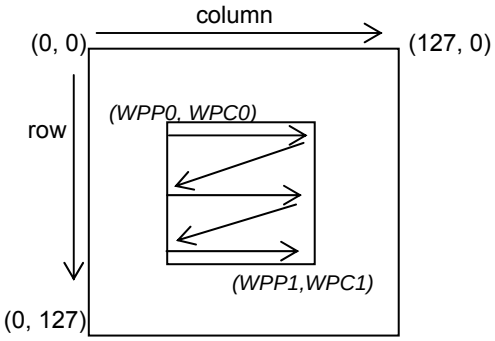
Window program is designed for data-write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and AC[3] setting for inside/outside window mode. When AC[3] is set to '0' (default value), data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). When AC[3] is set to '1', data will be written to whole SRAM excluding the specified window area.

The data-write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data-write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or row direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial column address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

Specify the starting point of data-write by issuing commands `Set Window Program Starting Column Address`, and `Set Window Program Starting Row Address`.

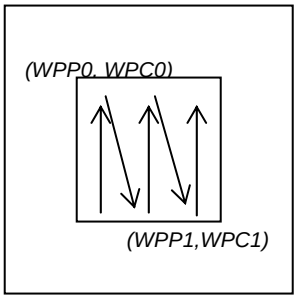
Example1 (AC[2:0] = 001) **:**

AC[3]=0 MX=0



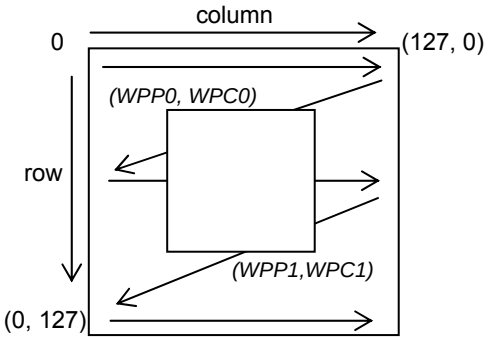
Example 2 (AC[2:0] = 111) **:**

AC[3] = 0 MX = 0



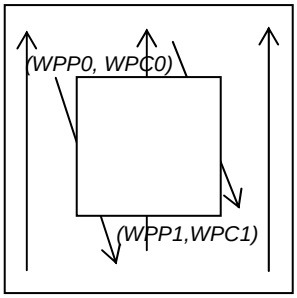
Example1-1 :

AC[3]=1 MX=0



Example 2-1 :

AC[3] = 1 MX = 0



Row Adderss	RAM	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
00H		COM1	COM17	COM128	COM16
01H		COM2	COM18	COM127	COM15
02H		COM3	COM19	COM126	COM14
03H		COM4	COM20	COM125	COM13
04H		COM5	COM21	COM124	COM12
05H		COM6	COM22	COM123	COM11
06H		COM7	COM23	COM122	COM10
07H		COM8	COM24	COM121	COM9
08H		COM9	COM25	COM120	COM8
09H		COM10	COM26	COM119	COM7
0AH		COM11	COM27	COM118	COM6
0BH		COM12	COM28	COM117	COM5
0CH		COM13	COM29	COM116	COM4
0DH		COM14	COM30	COM115	COM3
0EH		COM15	COM31	COM114	COM2
0FH		COM16	COM32	COM113	COM1
10H		COM17	COM33	COM112	COM128
11H		COM18	COM34	COM111	COM127
12H		COM19	COM35	COM110	COM126
13H		COM20	COM36	COM109	COM125
14H		COM21	COM37	COM108	COM124
15H		COM22	COM38	COM107	COM123
16H		COM23	COM39	COM106	COM122
17H		COM24	COM40	COM105	COM121
18H		COM25	COM41	COM104	COM120
19H		COM26	COM42	COM103	COM119
1AH		COM27	COM43	COM102	COM118
1BH		COM28	COM44	COM101	COM117
1CH		COM29	COM45	COM100	COM116
68H		COM105	COM121	COM24	COM40
69H		COM106	COM122	COM23	COM39
6AH		COM107	COM123	COM22	COM38
6BH		COM108	COM124	COM21	COM37
6CH		COM109	COM125	COM20	COM36
6DH		COM110	COM126	COM19	COM35
6EH		COM111	COM127	COM18	COM34
6FH		COM112	COM128	COM17	COM33
70H		COM113	COM1	COM16	COM32
71H		COM114	COM2	COM15	COM31
72H		COM115	COM3	COM14	COM30
73H		COM116	COM4	COM13	COM29
74H		COM117	COM5	COM12	COM28
75H		COM118	COM6	COM11	COM27
76H		COM119	COM7	COM10	COM26
77H		COM120	COM8	COM9	COM25
78H		COM121	COM9	COM8	COM24
79H		COM122	COM10	COM7	COM23
7AH		COM123	COM11	COM6	COM22
7BH		COM124	COM12	COM5	COM21
7CH		COM125	COM13	COM4	COM20
7DH		COM126	COM14	COM3	COM19
7EH		COM127	COM15	COM2	COM18
7FH		COM128	COM16	COM1	COM17

MX	SEG1	SEG2	SEG3	SEG4	SEG5			SEG380	SEG381	SEG382	SEG383	SEG384
0	SEG1	SEG2	SEG3	SEG4	SEG5			SEG380	SEG381	SEG382	SEG383	SEG384
1	SEG382	SEG383	SEG384	SEG379	SEG380			SEG5	SEG6	SEG1	SEG2	SEG3

Example for memory mapping: let MX = 0, MY = 0, SL = 0, LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color), according to the data shown in the above table (R: 11111b, G: 111111b, B: 11111b):

⇒ 1st byte of Write data: 11111111b

⇒ 2nd byte of Write data: 11111111b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1697v has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about 150mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1697v enters RESET sequence:

- Operation mode will be "Reset".
- All control registers are reset to default values. Refer to section *Control Registers* for details of their default values.

OPERATION MODES

UC1697v has three operating modes (OM): Reset, Sleep, Normal.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by `Set Display Enable`, OM will be updated automatically. There is no other action required to enter Sleep mode.

OM changes are synchronized with the edges of UC1697v internal clock. To ensure consistent system states, wait at least 10μS after `Set Display Enable` or `System Reset` command.

Action	Mode	OM
Reset command RST_ pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1697v consumes very little energy in Sleep mode (typically under 2μA).

EXITING SLEEP MODE

UC1697v contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1697v internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1697v power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 150 mS before the CPU starting to issue commands to UC1697v. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands.

There's no delay needed while turning on V_{DD} and $V_{DD2/3}$, and either one can be turned on first.

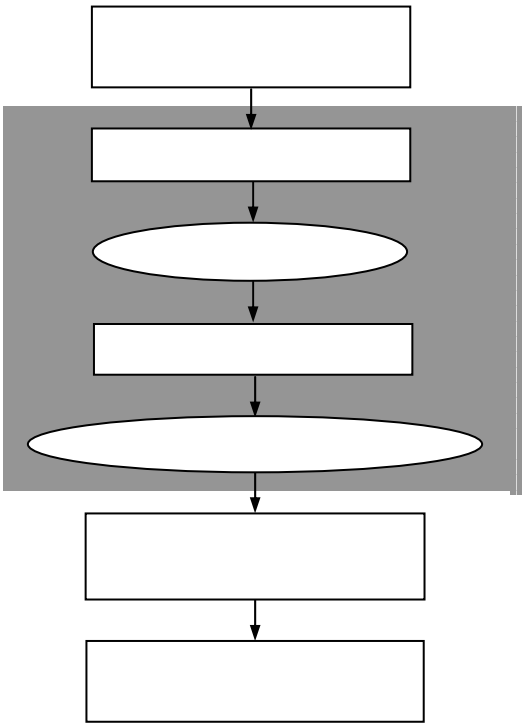


Figure 12: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX} and C_L from damaging the LCD, when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 10 KΩ for both V_{LCD} and V_{B+}. It is recommended to wait *3* x *RC* for V_{LCD} and *1.5 x RC* for V_B. For example, if C_L is 0.1uF, then the draining time required for V_{LCD} is ~3 mS.

When internal V_{LCD} is not used, UC1697v will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

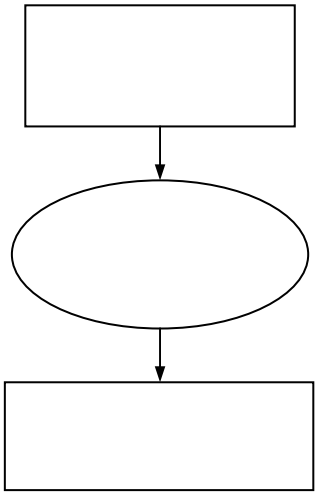


Figure 13: Reference Power-Down Sequence

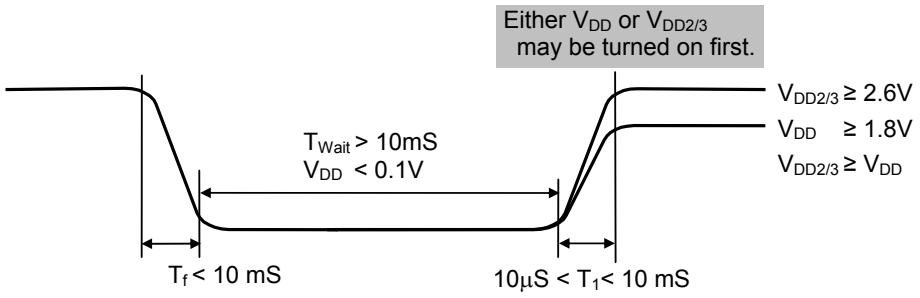


Figure 14: Power Off-On Sequence

MULTI-TIME PROGRAM NV MEMORY

OVERVIEW

MTP feature is available for UC1697v such that LCM makers can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1697v:

MTP-Erase, MTP-Program, MTP-Read.

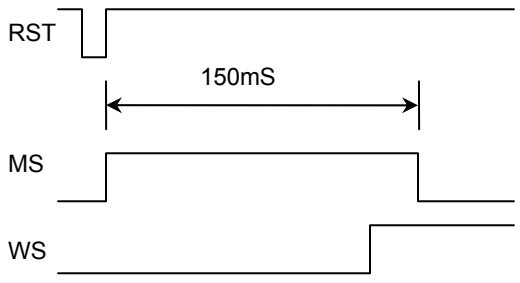
MTP-Program requires an external power source supplied to TST4 pin. MTP allows to program at least 10 times and should be performed only by the LCM makers.

MTP-Read is facilitated by the internal DC-DC converter built-in on UC1697v, no external power source is required, and it is performed automatically after hardware RESET (power-ON or pin RESET).

OPERATION FOR THE SYSTEM USERS

For the MTP version of UC1697v, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the *Read Status* commands will exhibit the following waveforms.



As illustrated above, the {MS, WS} will go through a {0,0}⇨{1,0}⇨{1,1}⇨{0,1} transition. When the {MS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

Although user can use *Read Status* command in a polling loop to make sure {MS, WS}={0, 1} before proceeding with the normal operations, however, it may be simpler to just issue `Set Display Enable` command every 0.5~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above “Periodical re-initializing” approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS. SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software *RESET* command. This enables the ICs to turn on display faster without the delay caused by MTP-READ.

It is recommended to use software *RESET* for normal operation control purpose and hardware RESET only during the event of power up and power down.

OPERATION FOR THE LCM MAKERS

Always ERASE the MTP NV memory cells, before starting the Write process.

MTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register MTP3 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 10V at TST4 can be maintained with proper consistency.

No external power source is required for MTP Erase and Read operation. For these MTP operations, TST4 should be open, or connected to V_{DD3}.

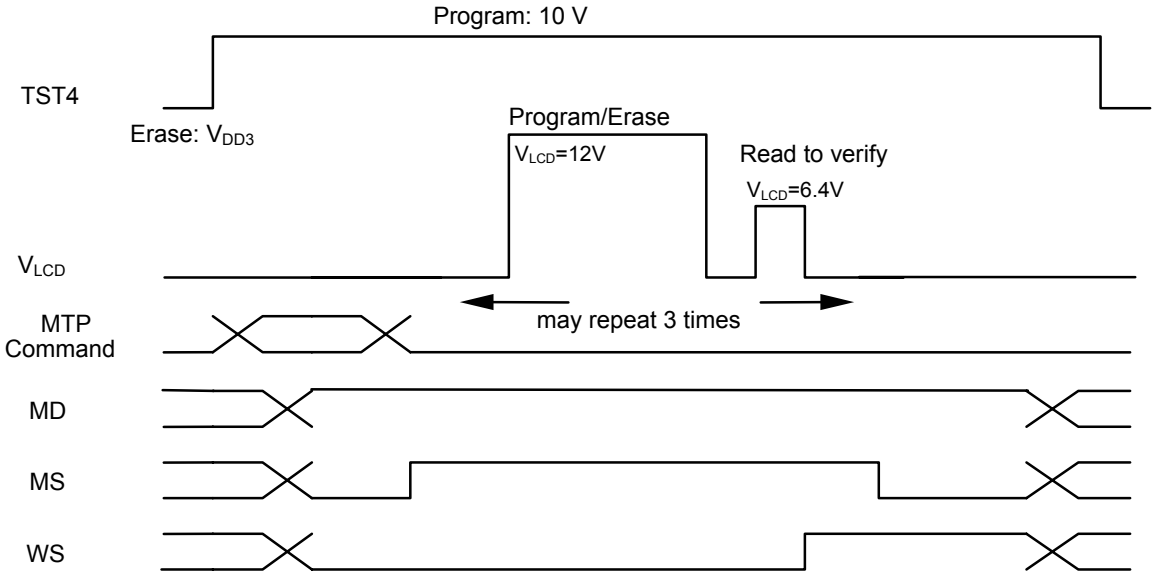
	V_{LCD}	**TST4 (external input)**
Program	MTP3 : 3Dh (12V)	10V (1mA per bit)
Erase	MTP3 : 3Dh (12V)	Floating or V_{DD3}
Read	MTP2 : 00h (6.4V)	Floating or V_{DD3}

Note:

1. Do Erase before Program and program one bit at a time.
2. When doing MTP Program or Erase, it's required to use $V_{DD2/3} \geqslant 3.0V$.

3. Read MTP status bits

With normal Get Status method (CD=0, W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not. If the operation succeeded, and current operation will be ended with WS=1. If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted. MD is MTP ID, which is either 1 for MTP IC. No transition.



MTP status bits, TST4 & V_{LCD} Waveform

MTP CELL VALUE USAGE

There are 6 MTP cell bits. They are divided into two groups for different purpose.

MTP[5:0] : V_{LCD} Trim
When PMO[5]=1: PM with trim = PM - PMO[4:0]
When PMO[5]=0: PM with trim = PM + PMO[4:0]

MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

(1) MTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP2: 00h(6.4V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	1	1	1	0	0	1		MTP3: 3Dh(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	1	0	1	0	0	0	0		MTP4: 50h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	1	0	0	0		MTP5: 08h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0	0	0	0	0	0	0	1	MTPM	Ex: To program MTPM[0] to be 1, set the value to 00000001b *
R	-	-	-	-	-	-	-	-	-	-		Apply TST4 voltage Program: 10V
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	1		Set MTPC[2:0]=011
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0, WS=1
R												Remove TST4 voltage
R											V_{DD}=0V	Power OFF

* It is recommended that users program one bit at a time.

(2) MTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP2: 00h(6.4V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	0	0	1	1	1	0	0	1		MTP3: 3Dh(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	1	0	1	0	0	0	0		MTP4: 50h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	1	0	0	0		MTP5: 08h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0	0	0	0	1	1	1	1	MTPM1	Ex: To erase MTPM[3:0], set the value to 00001111b
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	0		Set MTPC[2:0]=010
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0 WS=1
R											V_{DD}=0V	Power OFF

Note: It is recommended that users clear first all the bits to be programmed.

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)
W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).
Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 1mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset	Wait 150mS
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	Set Color Mode	
C	0	0	1	1	1	0	1	0	#	#	Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	LCD specific operating voltage setting
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~3mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

The following pins in UC1697v require special "ESD Sensitivity" consideration in particular:

Test Mode		Machine Mode		Human Body Mode	
		V_{DD}	V_{SS}	V_{DD}	V_{SS}
LCD Driver		200V	200V	2.0KV	2.0KV
LCM Interface		300V	300V	3.0KV	3.0KV
LCM HV pin/ Test pin	TST1/2/4	300V	300V	3.0KV	3.0KV
	CB pins	300V	300V	3.0KV	3.0KV
	V_{LCDIN}	300V	300V	3.0KV	3.0KV
	V_{LCDOUT}	300V	300V	3.0KV	3.0KV
PWR / GND		--	300V	--	3.0KV

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, Note 1 and 2

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Driving voltage	-0.3	+19.8	V
V_{IN}	Digital input signal	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

NOTE:

1. V_{DD} is based on V_{SS} = 0V
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65		3.3	V
$V_{DD2/3}$	Supply for bias & pump		2.5		3.3	V
V_{LCD}	Charge pump output	$V_{DD2/3}$ = 2.8V, 25^{O}C		15.2	16.5	V
V_D	LCD data voltage	$V_{DD2/3}$ = 2.8V, 25^{O}C	0.93		1.76	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
I_{SB}	Standby current	V_{DD} = $V_{DD2/3}$ = 3.3V, Temp = 85^{o}C			50	μA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 16.5V		1000	1200	Ω
$R_{ON(COM)}$	Upward COM output impedance	V_{LCD} = 16.5V		1000	1200	Ω
$R_{ONs(COM)}$	Downward COM output impedance	V_{LCD} = 16.5V		1900	2500	Ω
f_{LINE}	Average line rate	LC[4:3] = 10b, 25^{O}C	-10%	29.6	+10%	Klps

Note : Voltages exceeding the Max. value may still keep the IC operating properly, yet might shorten its lifetime.

POWER CONSUMPTION

V_{DD} = 2.7 V,
V_{LCD} = 15.22 V,
Mux Rate = 128,
C_B = 2.2 μF,
N-line inversion = 17 lines

Bias Ratio = 12,
Line Rate = 10 b,
Bus mode = 6800,
Temperature = 25 ^{o}C,
Color Mode = 64 K mode,

PM = 92,
Panel Loading (PC[1:0]) = 11 b,
C_L = 330 nF,
MTP= 00 H,
All HV outputs are open circuit.

Display Pattern	Conditions	Typ. (μA)	Max. (μA)
All-Pixel-OFF	Bus = idle	1233	(TBD)
2-pixel checker	Bus = idle	1692	(TBD)
None	Reset (stand-by current)	< 1	5

AC CHARACTERISTICS

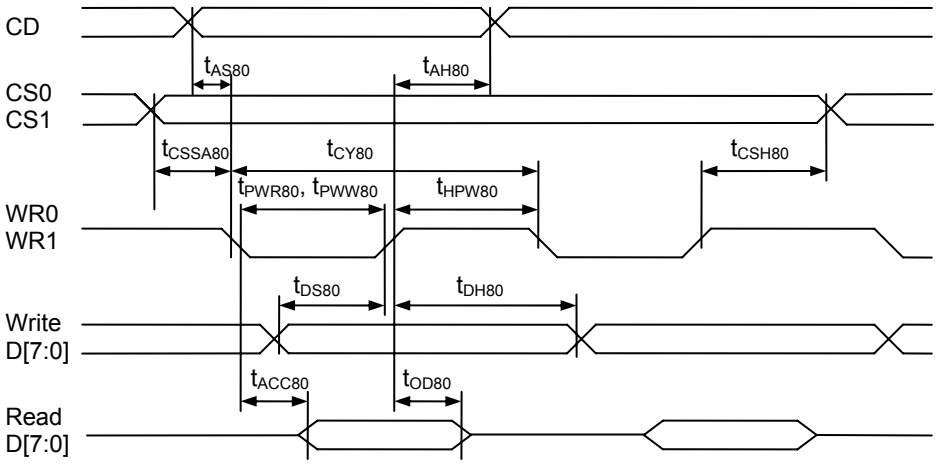


FIGURE 15: Parallel Bus Timing Characteristics (for 8080 MCU)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)		 170 130 100 80	–	nS
t_{PWR80}	WR1	Pulse width 16-bit (read) 8-bit		85 50	–	nS
t_{PWW80}	WR0	Pulse width 16-bit (write) 8-bit		65 40	–	nS
t_{HPW80}	WR0, WR1	High pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)		 85 65 50 40	–	nS
t_{DS80} t_{DH80}	D0~D15	Data setup time Data hold time		30 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		0 0		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)		 320 270 180 145	–	nS
t_{PWR80}	WR1	Pulse width 16-bit (read) 8-bit (read)		160 90	–	nS
t_{PWW80}	WR0	Pulse width 16-bit (write) 8-bit (write)		135 72	–	nS
t_{HPW80}	WR0, WR1	High pulse width 16-bit bus (read) (write) 8-bits bus (read) (write)		 160 135 90 72	–	nS
t_{DS80} t_{DH80}	D0~D15	Data setup time Data hold time		60 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	- 30	120 60	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		0 0		nS

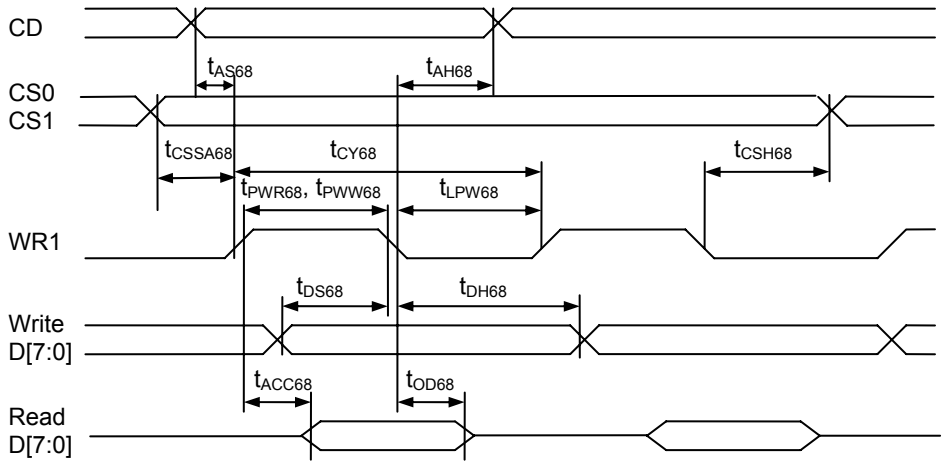


FIGURE 16: Parallel Bus Timing Characteristics (for 6800 MCU)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)		 170 130 100 80	–	nS
t_{PWR68}	WR1	Pulse width 16-bit (read) 8-bit		85 50	–	nS
t_{PWW68}		Pulse width 16-bit (write) 8-bit		65 40	–	nS
t_{LPW68}		Low pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)		 85 65 50 40	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		0 0		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)		 320 270 180 145	–	nS
t_{PWR68}	WR1	Pulse width 16-bit (read) 8-bit (read)		160 90	–	nS
t_{PWW68}		Pulse width 16-bit (write) 8-bit (write)		135 72	–	nS
t_{LPW68}		Low pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)		 160 135 90 72	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		60 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	- 30	120 60	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		0 0		nS

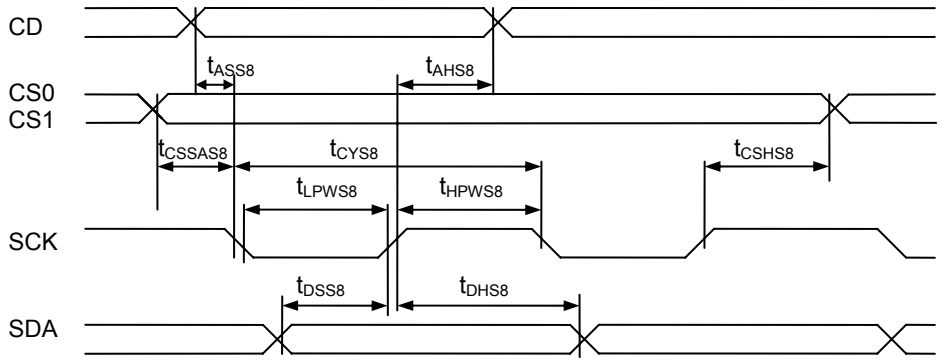


FIGURE 17: Serial Bus Timing Characteristics (for S8/S8uc)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		40	–	nS
t_{LPWS8}		Low pulse width		20	–	nS
t_{HPWS8}		High pulse width		20	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		15 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		75	–	nS
t_{LPWS8}		Low pulse width		37	–	nS
t_{HPWS8}		High pulse width		37	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 10	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		15 15		nS

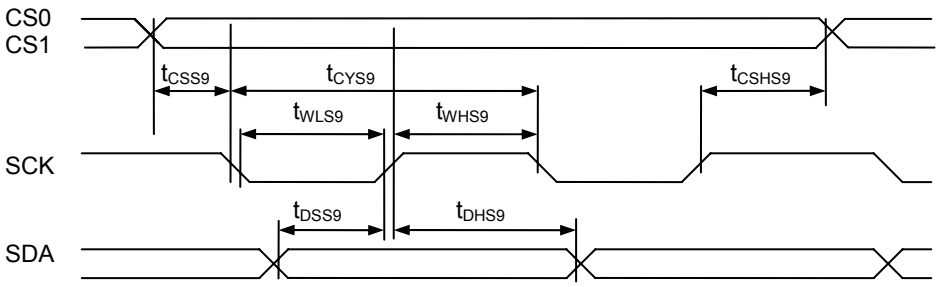


FIGURE 18: Serial Bus Timing Characteristics (for S9)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		40	–	nS
t_{LPWS9}		Low pulse width		20	–	nS
t_{HPWS9}		High pulse width		15	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		15 0	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		75	–	nS
t_{LPWS9}		Low pulse width		40	–	nS
t_{HPWS9}		High pulse width		30	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 0	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10		nS

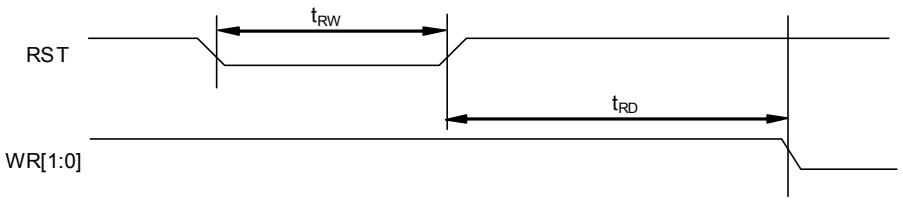


FIGURE 19: Reset Characteristics

(1.65V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	µS
t_{RD}	RST, WR	Reset to WR pulse delay		10	–	mS

PHYSICAL DIMENSIONS

PAD COORDINATES

DIE SIZE:
11309.6 μM x 1273 μM ± 40 μM

DIE THICKNESS:
400 μM ± 20 μM

AU BUMP HEIGHT:
15 μM
(H_{MAX}-H_{MIN}) within die ⩽ 2 μM

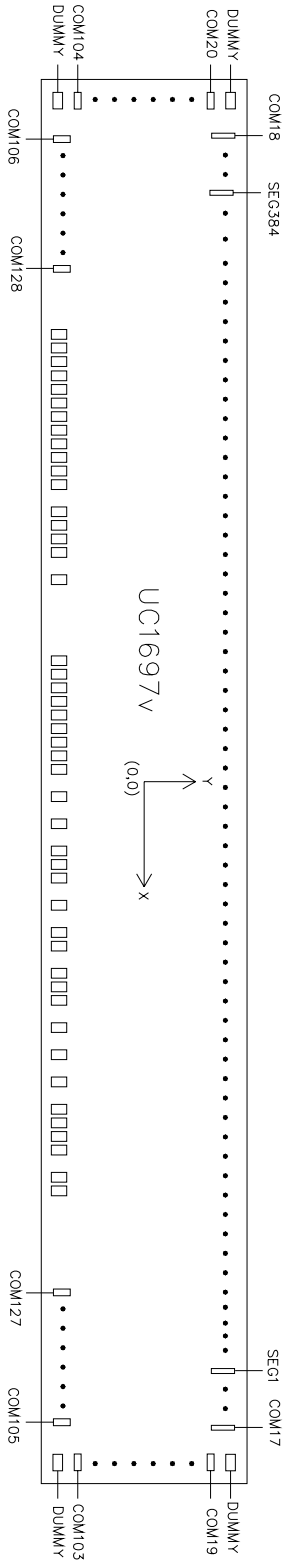
BUMP SIZE:
SEG /COM: 14.5x138 μM^2

BUMP PITCH:
26.5 μM

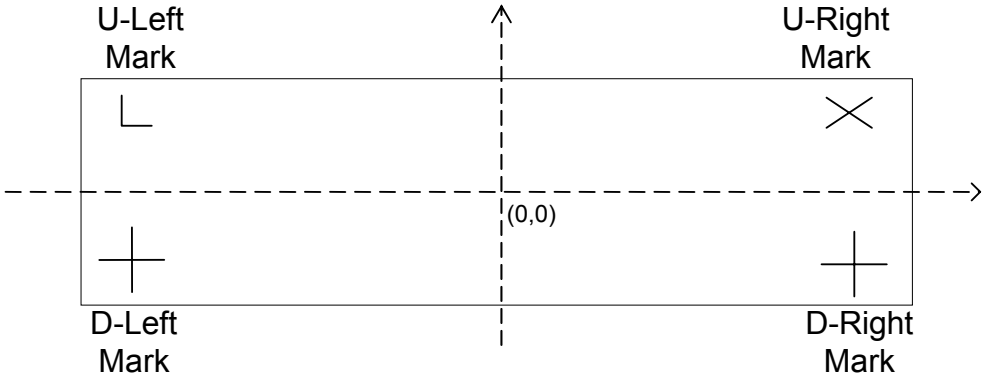
BUMP GAP:
12.0 μM

PAD COORDINATE ORIGIN:
Chip center

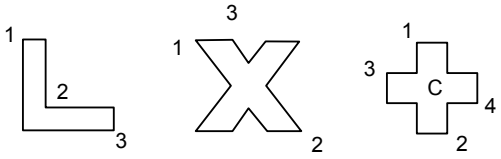
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment marks are on Metal3 under Passivation.

The “x” and “+” marks are symmetric both horizontally and vertically.

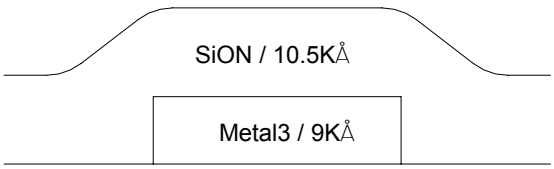
COORDINATES:

	U-Left Mark (L)		U-Right Mark (X)	
	X	Y	X	Y
1	-5374.5	586	5346.5	586
2	-5363.3	569.2	5374.5	558
3	-5346.5	558	5353.5	586

	D-Left Mark (+)		D-Right Mark (+)	
	X	Y	X	Y
1	-5419.8	-495	5399.8	-495
2	-5399.8	-580	5419.8	-580
3	-5452.3	-527.5	5367.3	-527.5
4	-5367.3	-547.5	5452.3	-547.5
C	-5409.8	-537.5	5409.8	-537.5

Note: The values of x-coordinate and y-coordinate in the tables are after-rounded.

TOP METAL AND PASSIVATION:



FOR MTP PROCESS CROSS-SECTION

PAD COORDINATES

#	Pad	X	Y	W	H
1	DUMMY	-5551.3	587.375	138	23.25
2	COM20	-5551.3	556.5	138	14.5
3	COM22	-5551.3	530	138	14.5
4	COM24	-5551.3	503.5	138	14.5
5	COM26	-5551.3	477	138	14.5
6	COM28	-5551.3	450.5	138	14.5
7	COM30	-5551.3	424	138	14.5
8	COM32	-5551.3	397.5	138	14.5
9	COM34	-5551.3	371	138	14.5
10	COM36	-5551.3	344.5	138	14.5
11	COM38	-5551.3	318	138	14.5
12	COM40	-5551.3	291.5	138	14.5
13	COM42	-5551.3	265	138	14.5
14	COM44	-5551.3	238.5	138	14.5
15	COM46	-5551.3	212	138	14.5
16	COM48	-5551.3	185.5	138	14.5
17	COM50	-5551.3	159	138	14.5
18	COM52	-5551.3	132.5	138	14.5
19	COM54	-5551.3	106	138	14.5
20	COM56	-5551.3	79.5	138	14.5
21	COM58	-5551.3	53	138	14.5
22	COM60	-5551.3	26.5	138	14.5
23	COM62	-5551.3	0	138	14.5
24	COM64	-5551.3	-26.5	138	14.5
25	COM66	-5551.3	-53	138	14.5
26	COM68	-5551.3	-79.5	138	14.5
27	COM70	-5551.3	-106	138	14.5
28	COM72	-5551.3	-132.5	138	14.5
29	COM74	-5551.3	-159	138	14.5
30	COM76	-5551.3	-185.5	138	14.5
31	COM78	-5551.3	-212	138	14.5
32	COM80	-5551.3	-238.5	138	14.5
33	COM82	-5551.3	-265	138	14.5
34	COM84	-5551.3	-291.5	138	14.5
35	COM86	-5551.3	-318	138	14.5
36	COM88	-5551.3	-344.5	138	14.5
37	COM90	-5551.3	-371	138	14.5
38	COM92	-5551.3	-397.5	138	14.5
39	COM94	-5551.3	-424	138	14.5
40	COM96	-5551.3	-450.5	138	14.5
41	COM98	-5551.3	-477	138	14.5
42	COM100	-5551.3	-503.5	138	14.5
43	COM102	-5551.3	-530	138	14.5
44	COM104	-5551.3	-556.5	138	14.5
45	DUMMY	-5551.3	-587.375	138	23.25
46	COM106	-5325.05	-533	14.5	138
47	COM108	-5298.55	-533	14.5	138
48	COM110	-5272.05	-533	14.5	138
49	COM112	-5245.55	-533	14.5	138
50	COM114	-5219.05	-533	14.5	138
51	COM116	-5192.55	-533	14.5	138
52	COM118	-5166.05	-533	14.5	138
53	COM120	-5139.55	-533	14.5	138
54	COM122	-5113.05	-533	14.5	138
55	COM124	-5086.55	-533	14.5	138
56	COM126	-5060.05	-533	14.5	138
57	COM128	-5033.55	-533	14.5	138
58	D15	-4853.9	-541.5	45	119
59	VDDX	-4793.9	-541.5	45	119
60	D14	-4733.9	-541.5	45	119
61	D13	-4487.9	-541.5	45	119
62	D12	-4427.9	-541.5	45	119
63	D11	-4181.9	-541.5	45	119

#	Pad	X	Y	W	H
64	D10	-4121.9	-541.5	45	119
65	D9	-3875.9	-541.5	45	119
66	D8	-3815.9	-541.5	45	119
67	D7	-3569.9	-541.5	45	119
68	D6	-3509.9	-541.5	45	119
69	D5	-3263.9	-541.5	45	119
70	D4	-3203.9	-541.5	45	119
71	D3	-2957.9	-541.5	45	119
72	D2	-2897.9	-541.5	45	119
73	D1	-2651.9	-541.5	45	119
74	D0	-2591.9	-541.5	45	119
75	RST_	-2415.1	-541	65	118
76	WR0	-2333.5	-541	65	118
77	VDDX	-2253.7	-541.5	45	119
78	WR1	-2173.9	-541	65	118
79	CD	-2092.3	-541	65	118
80	CS0	-2010.7	-541	65	118
81	VDDX	-1930.9	-541.5	45	119
82	CS1	-1851.1	-541	65	118
83	BM0	-1769.5	-541	65	118
84	VDDX	-1689.7	-541.5	45	119
85	BM1	-1609.9	-541	65	118
86	TST4	-1530.1	-541.5	45	119
87	TST4	-1470.1	-541.5	45	119
88	TST1	-1059.225	-541.5	45	119
89	TST2	-999.225	-541.5	45	119
90	ID0	-818.8	-541	65	118
91	VDDX	-739	-541.5	45	119
92	ID1	-659.2	-541	65	118
93	VSS	-579.4	-541.5	45	119
94	VSS	-519.4	-541.5	45	119
95	VSS	-459.4	-541.5	45	119
96	VSS	-399.4	-541.5	45	119
97	VSS	-339.4	-541.5	45	119
98	VSS	-279.4	-541.5	45	119
99	VSS	-219.4	-541.5	45	119
100	VSS	-159.4	-541.5	45	119
101	VSS	-99.4	-541.5	45	119
102	VSS	-39.4	-541.5	45	119
103	VSS	20.6	-541.5	45	119
104	VSS	80.6	-541.5	45	119
105	VSS	140.6	-541.5	45	119
106	DUMMY	228.775	-541.5	45	119
107	VSS2	313.6	-541.5	45	119
108	VSS2	373.6	-541.5	45	119
109	VSS2	433.6	-541.5	45	119
110	VSS2	493.6	-541.5	45	119
111	VSS2	553.6	-541.5	45	119
112	VSS2	613.6	-541.5	45	119
113	VSS2	673.6	-541.5	45	119
114	VSS2	733.6	-541.5	45	119
115	VSS2	793.6	-541.5	45	119
116	VSS2	853.6	-541.5	45	119
117	VSS2	913.6	-541.5	45	119
118	VDD	973.6	-541.5	45	119
119	VDD	1033.6	-541.5	45	119
120	VDD	1093.6	-541.5	45	119
121	VDD	1153.6	-541.5	45	119
122	VDD	1213.6	-541.5	45	119
123	VDD	1273.6	-541.5	45	119
124	VDD	1333.6	-541.5	45	119
125	DUMMY	1519.525	-541.5	45	119
126	DUMMY	1579.525	-541.5	45	119

#	Pad	X	Y	W	H
127	DUMMY	1639.525	-541.5	45	119
128	DUMMY	1699.525	-541.5	45	119
129	DUMMY	1759.525	-541.5	45	119
130	DUMMY	1819.525	-541.5	45	119
131	DUMMY	1879.525	-541.5	45	119
132	DUMMY	1939.525	-541.5	45	119
133	VDD2	2125.45	-541.5	45	119
134	VDD2	2185.45	-541.5	45	119
135	VDD2	2245.45	-541.5	45	119
136	VDD2	2305.45	-541.5	45	119
137	VDD2	2365.45	-541.5	45	119
138	VDD2	2425.45	-541.5	45	119
139	VDD2	2485.45	-541.5	45	119
140	DUMMY	2573.625	-541.5	45	119
141	VDD3	2750.3	-541.5	45	119
142	VDD3	2810.3	-541.5	45	119
143	VB0+	2878.45	-541.5	45	119
144	VB0+	2938.45	-541.5	45	119
145	VB0+	2998.45	-541.5	45	119
146	VB0+	3058.45	-541.5	45	119
147	VB1+	3266.6	-541.5	45	119
148	VB1+	3326.6	-541.5	45	119
149	VB1+	3386.6	-541.5	45	119
150	VB1+	3446.6	-541.5	45	119
151	VB1-	3654.75	-541.5	45	119
152	VB1-	3714.75	-541.5	45	119
153	VB1-	3774.75	-541.5	45	119
154	VB1-	3834.75	-541.5	45	119
155	VB0-	4042.9	-541.5	45	119
156	VB0-	4102.9	-541.5	45	119
157	VB0-	4162.9	-541.5	45	119
158	VB0-	4222.9	-541.5	45	119
159	VLCDIN	4562.9	-541.5	45	119
160	VLCDIN	4622.9	-541.5	45	119
161	VLCDOUT	4682.9	-541.5	45	119
162	VLCDOUT	4742.9	-541.5	45	119
163	COM127	5033.55	-533	14.5	138
164	COM125	5060.05	-533	14.5	138
165	COM123	5086.55	-533	14.5	138
166	COM121	5113.05	-533	14.5	138
167	COM119	5139.55	-533	14.5	138
168	COM117	5166.05	-533	14.5	138
169	COM115	5192.55	-533	14.5	138
170	COM113	5219.05	-533	14.5	138
171	COM111	5245.55	-533	14.5	138
172	COM109	5272.05	-533	14.5	138
173	COM107	5298.55	-533	14.5	138
174	COM105	5325.05	-533	14.5	138
175	DUMMY	5551.3	-587.375	138	23.25
176	COM103	5551.3	-556.5	138	14.5
177	COM101	5551.3	-530	138	14.5
178	COM99	5551.3	-503.5	138	14.5
179	COM97	5551.3	-477	138	14.5
180	COM95	5551.3	-450.5	138	14.5
181	COM93	5551.3	-424	138	14.5
182	COM91	5551.3	-397.5	138	14.5
183	COM89	5551.3	-371	138	14.5
184	COM87	5551.3	-344.5	138	14.5
185	COM85	5551.3	-318	138	14.5
186	COM83	5551.3	-291.5	138	14.5
187	COM81	5551.3	-265	138	14.5
188	COM79	5551.3	-238.5	138	14.5
189	COM77	5551.3	-212	138	14.5
190	COM75	5551.3	-185.5	138	14.5
191	COM73	5551.3	-159	138	14.5

#	Pad	X	Y	W	H
192	COM71	5551.3	-132.5	138	14.5
193	COM69	5551.3	-106	138	14.5
194	COM67	5551.3	-79.5	138	14.5
195	COM65	5551.3	-53	138	14.5
196	COM63	5551.3	-26.5	138	14.5
197	COM61	5551.3	0	138	14.5
198	COM59	5551.3	26.5	138	14.5
199	COM57	5551.3	53	138	14.5
200	COM55	5551.3	79.5	138	14.5
201	COM53	5551.3	106	138	14.5
202	COM51	5551.3	132.5	138	14.5
203	COM49	5551.3	159	138	14.5
204	COM47	5551.3	185.5	138	14.5
205	COM45	5551.3	212	138	14.5
206	COM43	5551.3	238.5	138	14.5
207	COM41	5551.3	265	138	14.5
208	COM39	5551.3	291.5	138	14.5
209	COM37	5551.3	318	138	14.5
210	COM35	5551.3	344.5	138	14.5
211	COM33	5551.3	371	138	14.5
212	COM31	5551.3	397.5	138	14.5
213	COM29	5551.3	424	138	14.5
214	COM27	5551.3	450.5	138	14.5
215	COM25	5551.3	477	138	14.5
216	COM23	5551.3	503.5	138	14.5
217	COM21	5551.3	530	138	14.5
218	COM19	5551.3	556.5	138	14.5
219	DUMMY	5551.3	587.375	138	23.25
220	COM17	5313.25	533	14.5	138
221	COM15	5286.75	533	14.5	138
222	COM13	5260.25	533	14.5	138
223	COM11	5233.75	533	14.5	138
224	COM9	5207.25	533	14.5	138
225	COM7	5180.75	533	14.5	138
226	COM5	5154.25	533	14.5	138
227	COM3	5127.75	533	14.5	138
228	COM1	5101.25	533	14.5	138
229	SEG1	5074.75	533	14.5	138
230	SEG2	5048.25	533	14.5	138
231	SEG3	5021.75	533	14.5	138
232	SEG4	4995.25	533	14.5	138
233	SEG5	4968.75	533	14.5	138
234	SEG6	4942.25	533	14.5	138
235	SEG7	4915.75	533	14.5	138
236	SEG8	4889.25	533	14.5	138
237	SEG9	4862.75	533	14.5	138
238	SEG10	4836.25	533	14.5	138
239	SEG11	4809.75	533	14.5	138
240	SEG12	4783.25	533	14.5	138
241	SEG13	4756.75	533	14.5	138
242	SEG14	4730.25	533	14.5	138
243	SEG15	4703.75	533	14.5	138
244	SEG16	4677.25	533	14.5	138
245	SEG17	4650.75	533	14.5	138
246	SEG18	4624.25	533	14.5	138
247	SEG19	4597.75	533	14.5	138
248	SEG20	4571.25	533	14.5	138
249	SEG21	4544.75	533	14.5	138
250	SEG22	4518.25	533	14.5	138
251	SEG23	4491.75	533	14.5	138
252	SEG24	4465.25	533	14.5	138
253	SEG25	4438.75	533	14.5	138
254	SEG26	4412.25	533	14.5	138
255	SEG27	4385.75	533	14.5	138
256	SEG28	4359.25	533	14.5	138

#	Pad	X	Y	W	H
257	SEG29	4332.75	533	14.5	138
258	SEG30	4306.25	533	14.5	138
259	SEG31	4279.75	533	14.5	138
260	SEG32	4253.25	533	14.5	138
261	SEG33	4226.75	533	14.5	138
262	SEG34	4200.25	533	14.5	138
263	SEG35	4173.75	533	14.5	138
264	SEG36	4147.25	533	14.5	138
265	SEG37	4120.75	533	14.5	138
266	SEG38	4094.25	533	14.5	138
267	SEG39	4067.75	533	14.5	138
268	SEG40	4041.25	533	14.5	138
269	SEG41	4014.75	533	14.5	138
270	SEG42	3988.25	533	14.5	138
271	SEG43	3961.75	533	14.5	138
272	SEG44	3935.25	533	14.5	138
273	SEG45	3908.75	533	14.5	138
274	SEG46	3882.25	533	14.5	138
275	SEG47	3855.75	533	14.5	138
276	SEG48	3829.25	533	14.5	138
277	SEG49	3802.75	533	14.5	138
278	SEG50	3776.25	533	14.5	138
279	SEG51	3749.75	533	14.5	138
280	SEG52	3723.25	533	14.5	138
281	SEG53	3696.75	533	14.5	138
282	SEG54	3670.25	533	14.5	138
283	SEG55	3643.75	533	14.5	138
284	SEG56	3617.25	533	14.5	138
285	SEG57	3590.75	533	14.5	138
286	SEG58	3564.25	533	14.5	138
287	SEG59	3537.75	533	14.5	138
288	SEG60	3511.25	533	14.5	138
289	SEG61	3484.75	533	14.5	138
290	SEG62	3458.25	533	14.5	138
291	SEG63	3431.75	533	14.5	138
292	SEG64	3405.25	533	14.5	138
293	SEG65	3378.75	533	14.5	138
294	SEG66	3352.25	533	14.5	138
295	SEG67	3325.75	533	14.5	138
296	SEG68	3299.25	533	14.5	138
297	SEG69	3272.75	533	14.5	138
298	SEG70	3246.25	533	14.5	138
299	SEG71	3219.75	533	14.5	138
300	SEG72	3193.25	533	14.5	138
301	SEG73	3166.75	533	14.5	138
302	SEG74	3140.25	533	14.5	138
303	SEG75	3113.75	533	14.5	138
304	SEG76	3087.25	533	14.5	138
305	SEG77	3060.75	533	14.5	138
306	SEG78	3034.25	533	14.5	138
307	SEG79	3007.75	533	14.5	138
308	SEG80	2981.25	533	14.5	138
309	SEG81	2954.75	533	14.5	138
310	SEG82	2928.25	533	14.5	138
311	SEG83	2901.75	533	14.5	138
312	SEG84	2875.25	533	14.5	138
313	SEG85	2848.75	533	14.5	138
314	SEG86	2822.25	533	14.5	138
315	SEG87	2795.75	533	14.5	138
316	SEG88	2769.25	533	14.5	138
317	SEG89	2742.75	533	14.5	138
318	SEG90	2716.25	533	14.5	138
319	SEG91	2689.75	533	14.5	138
320	SEG92	2663.25	533	14.5	138
321	SEG93	2636.75	533	14.5	138

#	Pad	X	Y	W	H
322	SEG94	2610.25	533	14.5	138
323	SEG95	2583.75	533	14.5	138
324	SEG96	2557.25	533	14.5	138
325	SEG97	2530.75	533	14.5	138
326	SEG98	2504.25	533	14.5	138
327	SEG99	2477.75	533	14.5	138
328	SEG100	2451.25	533	14.5	138
329	SEG101	2424.75	533	14.5	138
330	SEG102	2398.25	533	14.5	138
331	SEG103	2371.75	533	14.5	138
332	SEG104	2345.25	533	14.5	138
333	SEG105	2318.75	533	14.5	138
334	SEG106	2292.25	533	14.5	138
335	SEG107	2265.75	533	14.5	138
336	SEG108	2239.25	533	14.5	138
337	SEG109	2212.75	533	14.5	138
338	SEG110	2186.25	533	14.5	138
339	SEG111	2159.75	533	14.5	138
340	SEG112	2133.25	533	14.5	138
341	SEG113	2106.75	533	14.5	138
342	SEG114	2080.25	533	14.5	138
343	SEG115	2053.75	533	14.5	138
344	SEG116	2027.25	533	14.5	138
345	SEG117	2000.75	533	14.5	138
346	SEG118	1974.25	533	14.5	138
347	SEG119	1947.75	533	14.5	138
348	SEG120	1921.25	533	14.5	138
349	SEG121	1894.75	533	14.5	138
350	SEG122	1868.25	533	14.5	138
351	SEG123	1841.75	533	14.5	138
352	SEG124	1815.25	533	14.5	138
353	SEG125	1788.75	533	14.5	138
354	SEG126	1762.25	533	14.5	138
355	SEG127	1735.75	533	14.5	138
356	SEG128	1709.25	533	14.5	138
357	SEG129	1682.75	533	14.5	138
358	SEG130	1656.25	533	14.5	138
359	SEG131	1629.75	533	14.5	138
360	SEG132	1603.25	533	14.5	138
361	SEG133	1576.75	533	14.5	138
362	SEG134	1550.25	533	14.5	138
363	SEG135	1523.75	533	14.5	138
364	SEG136	1497.25	533	14.5	138
365	SEG137	1470.75	533	14.5	138
366	SEG138	1444.25	533	14.5	138
367	SEG139	1417.75	533	14.5	138
368	SEG140	1391.25	533	14.5	138
369	SEG141	1364.75	533	14.5	138
370	SEG142	1338.25	533	14.5	138
371	SEG143	1311.75	533	14.5	138
372	SEG144	1285.25	533	14.5	138
373	SEG145	1258.75	533	14.5	138
374	SEG146	1232.25	533	14.5	138
375	SEG147	1205.75	533	14.5	138
376	SEG148	1179.25	533	14.5	138
377	SEG149	1152.75	533	14.5	138
378	SEG150	1126.25	533	14.5	138
379	SEG151	1099.75	533	14.5	138
380	SEG152	1073.25	533	14.5	138
381	SEG153	1046.75	533	14.5	138
382	SEG154	1020.25	533	14.5	138
383	SEG155	993.75	533	14.5	138
384	SEG156	967.25	533	14.5	138
385	SEG157	940.75	533	14.5	138
386	SEG158	914.25	533	14.5	138

#	Pad	X	Y	W	H
387	SEG159	887.75	533	14.5	138
388	SEG160	861.25	533	14.5	138
389	SEG161	834.75	533	14.5	138
390	SEG162	808.25	533	14.5	138
391	SEG163	781.75	533	14.5	138
392	SEG164	755.25	533	14.5	138
393	SEG165	728.75	533	14.5	138
394	SEG166	702.25	533	14.5	138
395	SEG167	675.75	533	14.5	138
396	SEG168	649.25	533	14.5	138
397	SEG169	622.75	533	14.5	138
398	SEG170	596.25	533	14.5	138
399	SEG171	569.75	533	14.5	138
400	SEG172	543.25	533	14.5	138
401	SEG173	516.75	533	14.5	138
402	SEG174	490.25	533	14.5	138
403	SEG175	463.75	533	14.5	138
404	SEG176	437.25	533	14.5	138
405	SEG177	410.75	533	14.5	138
406	SEG178	384.25	533	14.5	138
407	SEG179	357.75	533	14.5	138
408	SEG180	331.25	533	14.5	138
409	SEG181	304.75	533	14.5	138
410	SEG182	278.25	533	14.5	138
411	SEG183	251.75	533	14.5	138
412	SEG184	225.25	533	14.5	138
413	SEG185	198.75	533	14.5	138
414	SEG186	172.25	533	14.5	138
415	SEG187	145.75	533	14.5	138
416	SEG188	119.25	533	14.5	138
417	SEG189	92.75	533	14.5	138
418	SEG190	66.25	533	14.5	138
419	SEG191	39.75	533	14.5	138
420	SEG192	13.25	533	14.5	138
421	SEG193	-13.25	533	14.5	138
422	SEG194	-39.75	533	14.5	138
423	SEG195	-66.25	533	14.5	138
424	SEG196	-92.75	533	14.5	138
425	SEG197	-119.25	533	14.5	138
426	SEG198	-145.75	533	14.5	138
427	SEG199	-172.25	533	14.5	138
428	SEG200	-198.75	533	14.5	138
429	SEG201	-225.25	533	14.5	138
430	SEG202	-251.75	533	14.5	138
431	SEG203	-278.25	533	14.5	138
432	SEG204	-304.75	533	14.5	138
433	SEG205	-331.25	533	14.5	138
434	SEG206	-357.75	533	14.5	138
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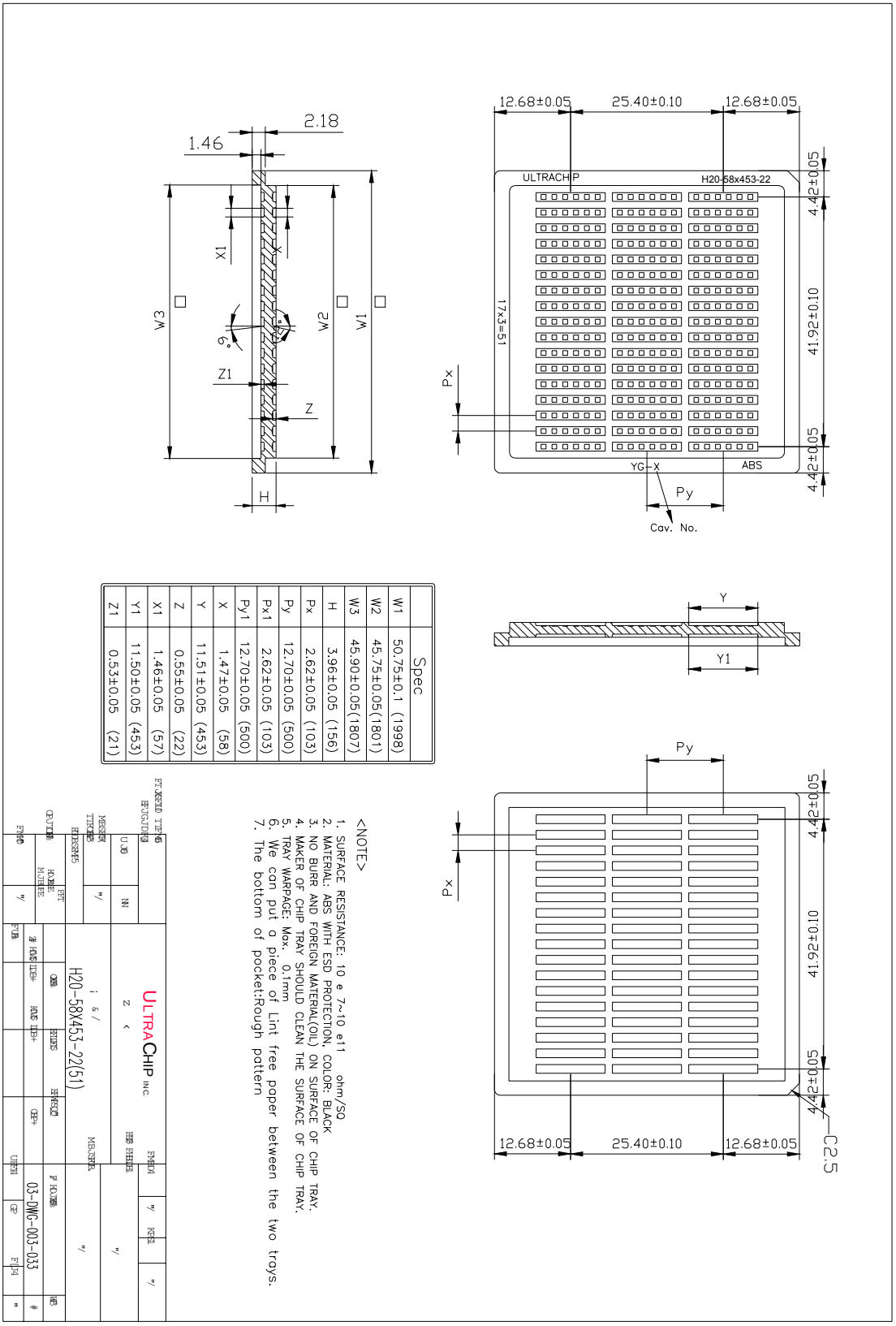
436	SEG208	-410.75	533	14.5	138
437	SEG209	-437.25	533	14.5	138
438	SEG210	-463.75	533	14.5	138
439	SEG211	-490.25	533	14.5	138
440	SEG212	-516.75	533	14.5	138
441	SEG213	-543.25	533	14.5	138
442	SEG214	-569.75	533	14.5	138
443	SEG215	-596.25	533	14.5	138
444	SEG216	-622.75	533	14.5	138
445	SEG217	-649.25	533	14.5	138
446	SEG218	-675.75	533	14.5	138
447	SEG219	-702.25	533	14.5	138
448	SEG220	-728.75	533	14.5	138
449	SEG221	-755.25	533	14.5	138
450	SEG222	-781.75	533	14.5	138
451	SEG223	-808.25	533	14.5	138

#	Pad	X	Y	W	H
452	SEG224	-834.75	533	14.5	138
453	SEG225	-861.25	533	14.5	138
454	SEG226	-887.75	533	14.5	138
455	SEG227	-914.25	533	14.5	138
456	SEG228	-940.75	533	14.5	138
457	SEG229	-967.25	533	14.5	138
458	SEG230	-993.75	533	14.5	138
459	SEG231	-1020.25	533	14.5	138
460	SEG232	-1046.75	533	14.5	138
461	SEG233	-1073.25	533	14.5	138
462	SEG234	-1099.75	533	14.5	138
463	SEG235	-1126.25	533	14.5	138
464	SEG236	-1152.75	533	14.5	138
465	SEG237	-1179.25	533	14.5	138
466	SEG238	-1205.75	533	14.5	138
467	SEG239	-1232.25	533	14.5	138
468	SEG240	-1258.75	533	14.5	138
469	SEG241	-1285.25	533	14.5	138
470	SEG242	-1311.75	533	14.5	138
471	SEG243	-1338.25	533	14.5	138
472	SEG244	-1364.75	533	14.5	138
473	SEG245	-1391.25	533	14.5	138
474	SEG246	-1417.75	533	14.5	138
475	SEG247	-1444.25	533	14.5	138
476	SEG248	-1470.75	533	14.5	138
477	SEG249	-1497.25	533	14.5	138
478	SEG250	-1523.75	533	14.5	138
479	SEG251	-1550.25	533	14.5	138
480	SEG252	-1576.75	533	14.5	138
481	SEG253	-1603.25	533	14.5	138
482	SEG254	-1629.75	533	14.5	138
483	SEG255	-1656.25	533	14.5	138
484	SEG256	-1682.75	533	14.5	138
485	SEG257	-1709.25	533	14.5	138
486	SEG258	-1735.75	533	14.5	138
487	SEG259	-1762.25	533	14.5	138
488	SEG260	-1788.75	533	14.5	138
489	SEG261	-1815.25	533	14.5	138
490	SEG262	-1841.75	533	14.5	138
491	SEG263	-1868.25	533	14.5	138
492	SEG264	-1894.75	533	14.5	138
493	SEG265	-1921.25	533	14.5	138
494	SEG266	-1947.75	533	14.5	138
495	SEG267	-1974.25	533	14.5	138
496	SEG268	-2000.75	533	14.5	138
497	SEG269	-2027.25	533	14.5	138
498	SEG270	-2053.75	533	14.5	138
499	SEG271	-2080.25	533	14.5	138
500	SEG272	-2106.75	533	14.5	138
501	SEG273	-2133.25	533	14.5	138
502	SEG274	-2159.75	533	14.5	138
503	SEG275	-2186.25	533	14.5	138
504	SEG276	-2212.75	533	14.5	138
505	SEG277	-2239.25	533	14.5	138
506	SEG278	-2265.75	533	14.5	138
507	SEG279	-2292.25	533	14.5	138
508	SEG280	-2318.75	533	14.5	138
509	SEG281	-2345.25	533	14.5	138
510	SEG282	-2371.75	533	14.5	138
511	SEG283	-2398.25	533	14.5	138
512	SEG284	-2424.75	533	14.5	138
513	SEG285	-2451.25	533	14.5	138
514	SEG286	-2477.75	533	14.5	138
515	SEG287	-2504.25	533	14.5	138
516	SEG288	-2530.75	533	14.5	138

#	Pad	X	Y	W	H
517	SEG289	-2557.25	533	14.5	138
518	SEG290	-2583.75	533	14.5	138
519	SEG291	-2610.25	533	14.5	138
520	SEG292	-2636.75	533	14.5	138
521	SEG293	-2663.25	533	14.5	138
522	SEG294	-2689.75	533	14.5	138
523	SEG295	-2716.25	533	14.5	138
524	SEG296	-2742.75	533	14.5	138
525	SEG297	-2769.25	533	14.5	138
526	SEG298	-2795.75	533	14.5	138
527	SEG299	-2822.25	533	14.5	138
528	SEG300	-2848.75	533	14.5	138
529	SEG301	-2875.25	533	14.5	138
530	SEG302	-2901.75	533	14.5	138
531	SEG303	-2928.25	533	14.5	138
532	SEG304	-2954.75	533	14.5	138
533	SEG305	-2981.25	533	14.5	138
534	SEG306	-3007.75	533	14.5	138
535	SEG307	-3034.25	533	14.5	138
536	SEG308	-3060.75	533	14.5	138
537	SEG309	-3087.25	533	14.5	138
538	SEG310	-3113.75	533	14.5	138
539	SEG311	-3140.25	533	14.5	138
540	SEG312	-3166.75	533	14.5	138
541	SEG313	-3193.25	533	14.5	138
542	SEG314	-3219.75	533	14.5	138
543	SEG315	-3246.25	533	14.5	138
544	SEG316	-3272.75	533	14.5	138
545	SEG317	-3299.25	533	14.5	138
546	SEG318	-3325.75	533	14.5	138
547	SEG319	-3352.25	533	14.5	138
548	SEG320	-3378.75	533	14.5	138
549	SEG321	-3405.25	533	14.5	138
550	SEG322	-3431.75	533	14.5	138
551	SEG323	-3458.25	533	14.5	138
552	SEG324	-3484.75	533	14.5	138
553	SEG325	-3511.25	533	14.5	138
554	SEG326	-3537.75	533	14.5	138
555	SEG327	-3564.25	533	14.5	138
556	SEG328	-3590.75	533	14.5	138
557	SEG329	-3617.25	533	14.5	138
558	SEG330	-3643.75	533	14.5	138
559	SEG331	-3670.25	533	14.5	138
560	SEG332	-3696.75	533	14.5	138
561	SEG333	-3723.25	533	14.5	138
562	SEG334	-3749.75	533	14.5	138
563	SEG335	-3776.25	533	14.5	138
564	SEG336	-3802.75	533	14.5	138
565	SEG337	-3829.25	533	14.5	138
566	SEG338	-3855.75	533	14.5	138
567	SEG339	-3882.25	533	14.5	138
568	SEG340	-3908.75	533	14.5	138
569	SEG341	-3935.25	533	14.5	138
570	SEG342	-3961.75	533	14.5	138
571	SEG343	-3988.25	533	14.5	138
572	SEG344	-4014.75	533	14.5	138
573	SEG345	-4041.25	533	14.5	138
574	SEG346	-4067.75	533	14.5	138
575	SEG347	-4094.25	533	14.5	138
576	SEG348	-4120.75	533	14.5	138
577	SEG349	-4147.25	533	14.5	138
578	SEG350	-4173.75	533	14.5	138
579	SEG351	-4200.25	533	14.5	138
580	SEG352	-4226.75	533	14.5	138
581	SEG353	-4253.25	533	14.5	138

#	Pad	X	Y	W	H
582	SEG354	-4279.75	533	14.5	138
583	SEG355	-4306.25	533	14.5	138
584	SEG356	-4332.75	533	14.5	138
585	SEG357	-4359.25	533	14.5	138
586	SEG358	-4385.75	533	14.5	138
587	SEG359	-4412.25	533	14.5	138
588	SEG360	-4438.75	533	14.5	138
589	SEG361	-4465.25	533	14.5	138
590	SEG362	-4491.75	533	14.5	138
591	SEG363	-4518.25	533	14.5	138
592	SEG364	-4544.75	533	14.5	138
593	SEG365	-4571.25	533	14.5	138
594	SEG366	-4597.75	533	14.5	138
595	SEG367	-4624.25	533	14.5	138
596	SEG368	-4650.75	533	14.5	138
597	SEG369	-4677.25	533	14.5	138
598	SEG370	-4703.75	533	14.5	138
599	SEG371	-4730.25	533	14.5	138
600	SEG372	-4756.75	533	14.5	138
601	SEG373	-4783.25	533	14.5	138
602	SEG374	-4809.75	533	14.5	138
603	SEG375	-4836.25	533	14.5	138
604	SEG376	-4862.75	533	14.5	138
605	SEG377	-4889.25	533	14.5	138
606	SEG378	-4915.75	533	14.5	138
607	SEG379	-4942.25	533	14.5	138
608	SEG380	-4968.75	533	14.5	138
609	SEG381	-4995.25	533	14.5	138
610	SEG382	-5021.75	533	14.5	138
611	SEG383	-5048.25	533	14.5	138
612	SEG384	-5074.75	533	14.5	138
613	COM2	-5101.25	533	14.5	138
614	COM4	-5127.75	533	14.5	138
615	COM6	-5154.25	533	14.5	138
616	COM8	-5180.75	533	14.5	138
617	COM10	-5207.25	533	14.5	138
618	COM12	-5233.75	533	14.5	138
619	COM14	-5260.25	533	14.5	138
620	COM16	-5286.75	533	14.5	138
621	COM18	-5313.25	533	14.5	138

TRAY INFORMATION



	Spec
W1	50.75±0.1 (1998)
W2	45.75±0.05(1801)
W3	45.90±0.05(1807)
H	3.96±0.05 (156)
Px	2.62±0.05 (103)
Py	12.70±0.05 (500)
Px1	2.62±0.05 (103)
Py1	12.70±0.05 (500)
X	1.47±0.05 (58)
Y	11.51±0.05 (453)
Z	0.55±0.05 (22)
X1	1.46±0.05 (57)
Y1	11.50±0.05 (453)
Z1	0.53±0.05 (21)

<NOTE>
1. SURFACE RESISTANCE: 10 e 7~10 e11 ohm/SQ
2. MATERIAL: ABS WITH ESD PROTECTION, COLOR: BLACK
3. NO BURR AND FOREIGN MATERIAL(OIL) ON SURFACE OF CHIP TRAY.
4. MAKER OF CHIP TRAY SHOULD CLEAN THE SURFACE OF CHIP TRAY.
5. TRAY WARPAGE: Max. 0.1mm
6. We can put a piece of Lint free paper between the two trays.
7. The bottom of pocket:Rough pattern

ULTRACHIP INC.
H20-58X453-22(51)
03-DWG-003-033

REVISION HISTORY

Revision	Contents	Date of Rev.
0.6	First Release	Feb. 7, 2007