HIGH-VOLTAGE MIXED-SIGNAL IC

UC1682

80 x 104RGB C-STN LCD Controller-Driver
w/ 32-shade per dot, 12-bit per RGB (Dither 221K)

ES Specifications
Revision 0.6

August 11, 2003

ULTRACHIP
The Coolest LCD Driver Ever!!

TABLE OF CONTENT

UC1682

Single-Chip, Ultra-Low Power
80COM x 312SEG Matrix
Passive Color LCD Controller-Driver

INTRODUCTION

UC1682 is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images, with well balanced gray shades and vivid colors.

In addition to low power COM and SEG drivers, UC1682 contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 80x104 matrix C-STN LCD with comprehensive support for input format and color depth:
  - 8-bit RGB: 256 color
  - 12-bit RGB: 4K color
  - 16-bit RGB: 56K color (dithering)
  - 24-bit RGB: 221K color (dithering)
- One software readable ID pin to support configurable vender identification.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both row ordered and column ordered display buffer RAM access.
- Support industry standard 3-wire, 4-wire serial bus (S9, S8, S8uc) and 8-bit/4-bit parallel bus (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Ultra-low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Software programmable frame rates up to 250Hz. Support the use of fast Liquid Crystal material for speedy LCD response.
- Software programmable four temperature compensation coefficients.
- On-chip Power-ON Reset and Software Reset command, make RST pin optional.
- Self-configuring 10x charge pump with on-chip pumping capacitors. Only 2/3 external capacitors are required to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Very low pin count (9~10 pins with S9) allows exceptional image quality in COG format on conventional ITO glass.
- Many on-chip and I/O pad layout features to support optimized COG applications.
- V_{DD} (digital) range: 1.8V ~ 3.3V
  V_{DD} (analog) range: 2.4V ~ 3.3V
  LCD V_{OP} range: 5.0V ~ 10.5V
- Available OTP V_{LCD} trimming option to support precise LCD contrast matching
- Available in COF and gold bump dies
  Bump pitch: 41.5μM
  Bump gap: 17μM
  Bump surface: 3,000μM^2

ORDERING INFORMATION

Part Number	Versions	Description
UC1682xHCZ	Gold Bumped Die with PI	Without OTP option
UC1682tHCZ	Gold Bumped Die with PI	With OTP option
UC1682xFBZ	COF	Without OTP option
UC1682tFBZ	COF	with OTP option

Convention note:

Grayed-out contents are functions not available yet.

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of UltraChip's delivery. There is no post waffle saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

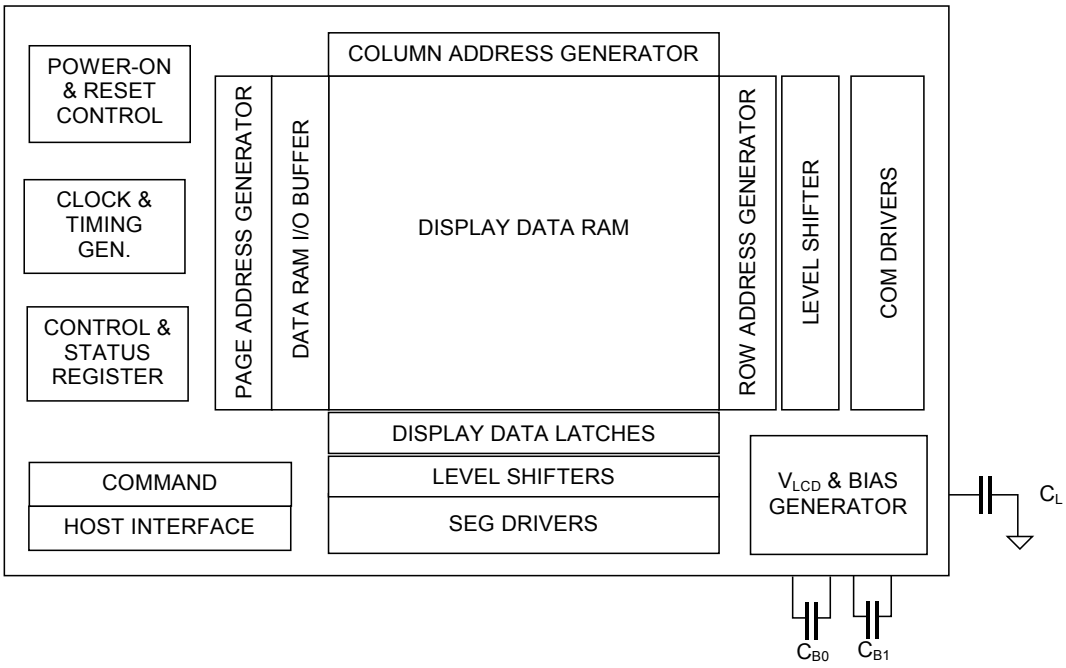
OTP CELL LIGHT SENSITIVITY

The OTP memory cell is sensitive to photon excitation. Under extended exposure to strong ambient light, the OTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light shields to realize full OTP content retention performance.

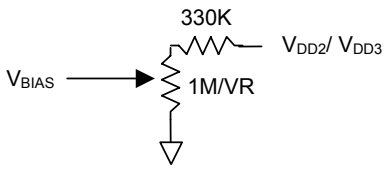
LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Pins	Description
			MAIN POWER SUPPLY
V_{DD} V_{DD2} V_{DD3}	PWR		V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. Please maintain the following relationship: $V_{DD}+1V \geqslant V_{DD2/3} \geqslant V_{DD}$. "Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND		Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for this node.
			LCD POWER SUPPLY & VOLTAGE CONTROL
V_{BIAS}	I		This is the reference voltage to generate the actual SEG driving voltage. V_{BIAS} can be used to fine tune V_{LCD} by external variable resistors. Internal resistor network has been provided to simplify external trimming circuit. The following network is sufficient for most applications.  An internal RC filter is provided to filter noise on the V_{BIAS} pin. When not used, it is OK to leave V_{BIAS} open circuit. If noise starts to cause problem, connect a small bypass capacitor between V_{BIAS} and V_{SS}. In the OTP version, this pin is disconnected from internal circuit. So, there is no need to add bypass capacitor for this pin for OTP version.
V_{B1+} V_{B1-} V_{B0+} V_{B0-}	PWR		LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
S_{B1+} S_{B1-} S_{B0+} S_{B0-}	I		Wire to corresponding $V_{B1/2x}$ pin. Merge ITO traces between corresponding S_{Bx} and V_{Bx} in COG.
V_{LCD-IN} $V_{LCD-OUT}$	PWR		High voltage LCD Power Supply. Connect these pins together. By-pass capacitor C_L is optional. It can be connected between V_{LCD} and V_{SS}. When C_L is used, keep the trace resistance under 300 Ω.

NOTE

- Recommended capacitor values:
  C_B: 150~250x LCD load capacitance or 2.2μF (2V), whichever is higher.
  C_L: (Optional) 5nF~50nF (16V) is appropriate for most applications.

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1</td><td>I</td><td></td><td>Bus mode: The interface bus mode is determined by BM[1:0] and D[7:6] by the following relationship:
<table>
<tr><th>BM[1:0]</th><th>D[7:6]</th><th>Mode</th></tr>
<tr><td>11</td><td>Data</td><td>6800/8-bit</td></tr>
<tr><td>10</td><td>Data</td><td>8080/8-bit</td></tr>
<tr><td>01</td><td>0X</td><td>6800/4-bit</td></tr>
<tr><td>00</td><td>0X</td><td>8080/4-bit</td></tr>
<tr><td>01</td><td>10</td><td>3-wire SPI w/ 9-bit token
(S9: conventional)</td></tr>
<tr><td>00</td><td>10</td><td>4-wire SPI w/ 8-bit token
(S8: conventional)</td></tr>
<tr><td>00</td><td>11</td><td>3/4-wire SPI w/ 8-bit token
(S8uc: Ultra-Compact)</td></tr>
</table></td></tr>
<tr><td>CS1
CS0</td><td>I</td><td>2</td><td>Chip Select. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, D[7:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td></td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1682 has built-in Power-ON Reset and Software Reset command, RST pin is not required for proper chip operation.
An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD</td><td>I</td><td></td><td>Select Control data or Display data for read/write operation. In S9 modes, CD pin is not used. Connect CD to V_{SS} when not used.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>ID</td><td>I</td><td></td><td>ID pin is for production control. The connection will affect the content of D[7] when using Get Status command. Connect to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td></td><td>WR[1:0] controls the read/write operation of the host interface. See Host Interface section for more detail.
In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td></td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D[0] to SCK, D[3] to SDA,
<table>
<tr><th></th><th>BM=1x
(Parallel)</th><th>BM=0x
(Parallel)</th><th>BM=01
(S9)</th><th>BM=00
(S8/S8uc)</th></tr>
<tr><td>D0</td><td>D0</td><td>D0/D4</td><td>SCK</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td>D1/D5</td><td>–</td><td>–</td></tr>
<tr><td>D2</td><td>D2</td><td>D2/D6</td><td>–</td><td>–</td></tr>
<tr><td>D3</td><td>D3</td><td>D3/D7</td><td>SDA</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D5</td><td>D5</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D6</td><td>D6</td><td>–</td><td>0</td><td>S8/S8uc</td></tr>
<tr><td>D7</td><td>D7</td><td>0</td><td>1</td><td>1</td></tr>
</table>
Connect unused pins to V_{SS}.</td></tr>
</table>

Name	Type	Pins	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG312	HV		SEG (column) driver outputs. Support up to 104 x RGB pixels. Leave unused drivers open-circuit.
COM1 ~ COM80	HV		COM (row) driver outputs. Support up to 80 rows. Leave unused COM drivers open-circuit. When designing LCM, always start from COM1. If the LCM has *N* pixel rows and *N* is less than 80, set CEN to be *N-1*, and leave COM drivers [N+1 ~ 80] open-circuit.
MISC. PINS			
V_{DDX}	O		Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus on chip. They are provided to facilitate chip configurations in COG and COF applications. These pins should not be used to provide V_{DD} power to the chip. It is not necessary to connect V_{DDX} to main V_{DD} externally.
TST4	I/HV		Test control. This pin has on-chip pull-up/down resistor. Leave it open during normal operation. TST4 is also used as one of the high voltage programming power supply for OTP operation. For COG design with OTP options, please wire out TST4 with an ITO trace resistance of 200 Ω or less.
TST2	I/O		Test I/O pins. Leave these pins open during normal use.
TP[5:1]	I		Test control. Leave these pins open during normal use.

Note: Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM*X* or SEG*X* will correspond to index *X*-1, and the value ranges for those index registers will be 0~79 for COM and 0~311 for SEG.

RECOMMENDED COG LAYOUT

Users can use either OTP control (through TST4 pin) or external circuit (through V_{BIAS} pin) to fine tune V_{LCD}. Please refer to the following figures:

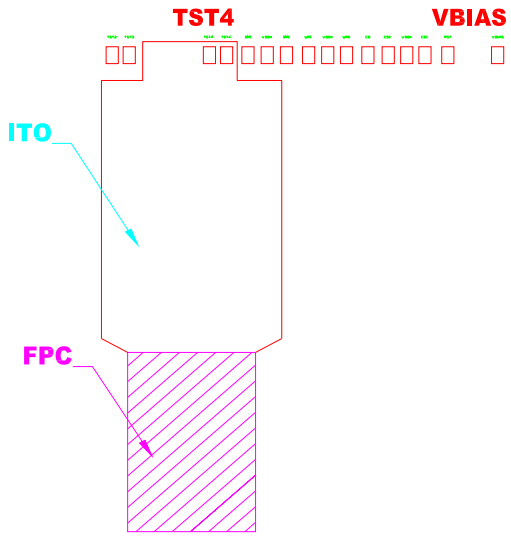


FIGURE 1: Example for TST4 COG layout when using OTP control to fine tune V_{LCD}

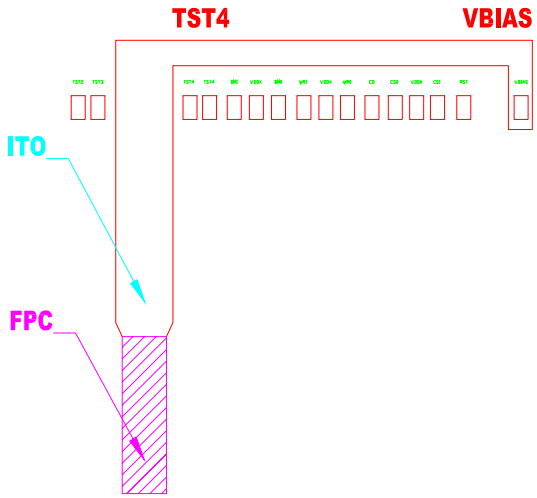
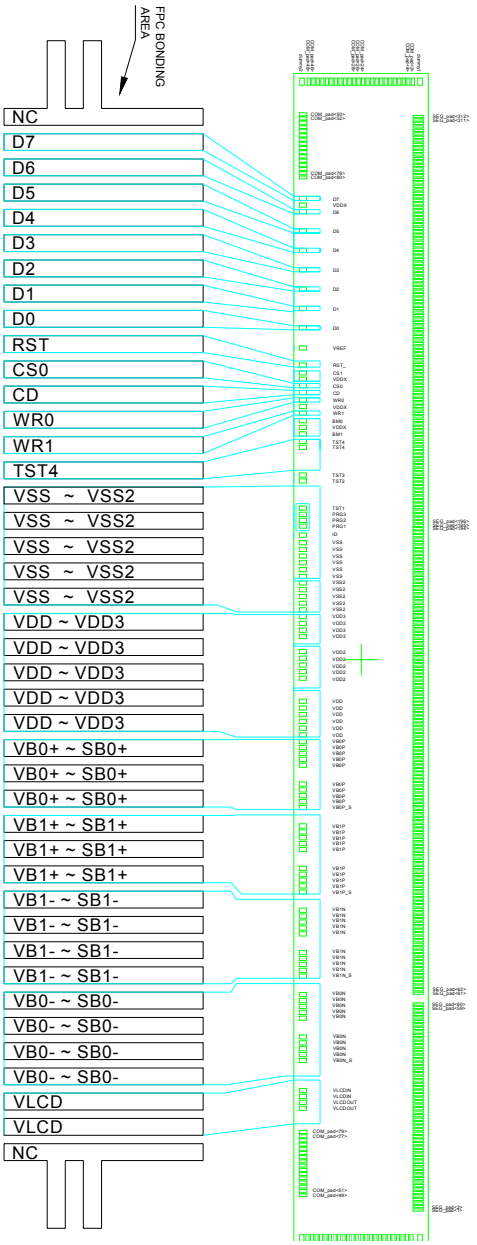


FIGURE 2: Example for V_{BIAS} COG layout when using external circuit to fine tune V_{LCD}

REFERENCE COG LAYOUT



Notes for V_{DD} with COG:

The V_{DD}=1.8V-typ operation condition of UC1682 should be met under all LCM formats. Unless V_{DD}, $V_{DD2/3}$ ITO trances can each be controlled to be 5 Ω or lower, otherwise V_{DD}-$V_{DD2/3}$ separation can cause the actual on-chip V_{DD} to drop below V_{DD}=1.7V during high speed data write condition. Therefore, for COG, V_{DD}-$V_{DD2/3}$ separation is not suitable for pure ITO based COG designs.

CONTROL REGISTERS

UC1682 contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meanings and their default values. Commands supported by UC1682 will be described in the next two sections. First, a summary table, followed by a detailed instruction-by-instruction description.

Name: The Symbolic reference of the register.
Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	7	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (79– 2xFL). Setting SL outside of this range causes undefined effect on the displayed image.
FL	4	0H	Fixed Lines. The first FLx2 lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two regions: one scrollable, one non-scrollable. When partial display mode is activated, the display of these 2xFL lines is also controlled by LC[0].
CR	7	0H	Return Column Address. Useful for cursor implementation.
CA	7	0H	Display Data RAM Column Address (counted in RGB triplet) (Used in Host to Display Data RAM access)
RA	7	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 5 01b: 7 10b: 8 **11b: 9**
TC	2	0H	Temperature Compensation (per ^{o}C) **00b: -0.05%** 01b: -0.10% 10b: -0.15% 11b: -0.20%
PM	8	55H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	6	20H	PM offset. The effective PM value PMV = PM+PMO-32. Make sure PMV formula does not overflow or underflow. (Available only on OTP version).
OM	2	–	Operating Modes (Read only) 10b: Sleep 11b: Normal 01b: (Not used) 00b: Reset
ID	1	PIN	Access the connected status of ID pin.
MSK	3	0H	R/G/B Write Data mask bits MSK[2:0] = {MR, MG, MB} (Default: **000b**) 0: Write 1: Block
RS	1		Reset in progress. Host Interface not ready
PC	4	DH	Power Control. PC[1:0]: 00b: LCD: ⩽ 9nF **01b: LCD: 9~12nF** 10b: LCD: 12~16nF 11b: LCD: 16~22nF PC[3:2]: 00b: External V_{LCD} **11b: Internal V_{LCD}** (Standard)

Name	Bits	Default	Description
DC	5	18H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) DC[3]: Gray-shade Modulation mode. 0: 8-shade mode **1: 32-shade Mode** DC[4]: Dither Function Control. 0: Disable Dither Function **1: Enable Dither Function**
AC	5	1H	Address Control: AC[0]: WA: Automatic column/row Wrap Around (Default **1: ON**) AC[1]: Auto-Increment order **0: Column (CA) first** 1: Row (RA) first AC[2]: RID: RA (row address) auto increment direction (**L:+1** H:-1) AC[3]: CUM: Cursor update mode, (Default **0: OFF**) when CUM=1, CA increment on write only, wrap around suspended AC[4] : Window Program Enable **0 : Disable** 1 : Enable
WPC0	8	00H	Window program starting column address. Value range: 0 ~103.
WPP0	8	00H	Window program starting row address. Value range: 0~79.
WPC1	8	67H	Window program ending column address. Value range: 0~103.
WPP1	8	4FH	Window program ending row address. Value range: 0~79.
OTP operation			For OTP version IC, register WPC[1:0] and WPP[1:0] are also used to control the OTP operation (when OTPC[3]=1).
CEN DST DEN	7 7 7	4FH 00H 4FH	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ⩾ DEN ⩾ DST+ 9

Name	Bits	Default	Description
LC	10	090H	LCD Control: LC[0]: Enable the first FLx2 lines in partial display mode (Default **OFF**). LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: **OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: **OFF**) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 10.0 Klps 01b: 12.8 Klps **10b: 16.0 Klps** 11b: 20.0 Klps (Frame-Rate = Line-Rate / Mux-Rate) LC[5] : RGB filter order (as mapped to SEG1, SEG2, SEG3) **0 : BGR-BGR** 1 : RGB-RGB LC[7:6] : Color and input mode for Dither-Enabled: 00b : 256 color mode. 3R-3G-2B (8-bit/RGB) 01b : 4K color mode. 4R-4G-4B (12-bit/RGB) **10b : 56K color mode**. 5R-6G-5B (16-bit/RGB) 11b : 221K color mode. 6R-7G-5B (24-bit/RGB) for Dither-Disabled: 00b : 256 color mode. 3R-3G-2B (8-bit/RGB) 01b : 4K color mode. 4R-5G-3B (12-bit/RGB) 10b : 4K color mode. 5R-6G-5B (16-bit/RGB) 11b : 4K color mode. 6R-7G-5B (24-bit/RGB) For data over 4R-5G-3B, each redundant LSB of each color will be truncated. (Example: For R4R3R2R1R0 - G5G4G3G2G1G0 - B4B3B2B1B0, R0, G0, B1, and B0 will be truncated.) LC[9:8] : Partial Display Control **0xb: Disable** Mux-Rate = CEN+1 (DST, DEN not used) 10b: Enabled Mux-Rate = CEN+1 11b: Enabled Mux-Rate = DEN-DST+1+LC[0]x2xFL
APC0 APC1	5 8	0DH 36H	Advanced Program Control. For UltraChip only. Please do not use.
OD	1	–	OTP option flag 0: No OTP 1: With OTP
OS	1	–	OTP programming in-progress
WS	1	–	OTP Command Succeeded
OTPC	6	10H	OTP Programming Control: OTP0[2:0] : OTP command **000** : Sleep 001 : Read 010 : Erase 011 : Program 1XX : For UltraChip use only OTP[3] : OTP Enable (auto clear after OTP command action done) OTP[4] : Use/Ignore OTP value. 0: Ignore **1: Normal** OTP[5] : OTP Command enable
OTPM	8	00H	OTP Write Mask

COMMAND TABLE

The following is a list of host commands supported by UC1682

C/D: 0: Control, 1: Data

W/R: 0: Write Cycle, 1: Read Cycle

\# Useful Data bits

– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	ID	MX	MY	WA	DE	WS	OD	OS	Get Status	N/A
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	-	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	1
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0, or 1	N/A
	(double byte command)	0	0	#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0
10	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	-	#	#	#	Set RA[6:4]	0
11	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	55H
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
12	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	0: Disable
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
18	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
19	Set Color Mask	0	0	1	0	1	1	0	#	#	#	Set MSK[2:0]	0
20	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
21	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
22	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b (56K)
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
	(double byte command)	0	0	#	#	#	#	#	#	#	#		
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 9
27	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	AC[3]=0
28	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	AC[3]=1
29	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	79
		0	0	-	#	#	#	#	#	#	#		
30	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
31	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	79
		0	0	-	#	#	#	#	#	#	#		
32	Set Window Program	0	0	1	1	1	1	0	1	0	0	Set WPC0[7:0]	0
	Starting Column Address	0	0	#	#	#	#	#	#	#	#		
33	Set Window Programming	0	0	1	1	1	1	0	1	0	1	Set WPP0[7:0]	0
	Starting Row Address	0	0	#	#	#	#	#	#	#	#		
34	Set Window Programming	0	0	1	1	1	1	0	1	1	0	Set WPC1[7:0]	103
	Ending Column Address	0	0	#	#	#	#	#	#	#	#		
35	Set Window Programming	0	0	1	1	1	1	0	1	1	1	Set WPP1[7:0]	79
	Ending Row Address	0	0	#	#	#	#	#	#	#	#		
36	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[4]	0: Disable

* Other than commands listed above, all other bit patterns may result in undefined behavior.

	OTP Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
37	Set OTP Operation control	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	0 #	Set OTP0[5:0]	0
38	Set OTP Write Mask	0 0	0 0	1 #	0 #	1 #	1 #	1 #	0 #	0 #	1 #	Set OTP1[7:0]	0
39	Set V_{OTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Programming commands	N/A
40	Set V_{OTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		
41	Set OTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		
42	Set OTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		

- Other than commands listed above, all other bit patterns may result in undefined behavior.
- The OTP commands listed above should only be used with OTP version of UC1682.
- Command 39~42 are shared with command 32~35, and they have exactly the same code. The interpretation of these four commands depends on register OTPC[3]. When OTPC[3]=0, they are interpreted as *Window Programming* commands. When OTPC[3]=1, they are *OTP Control* commands.
- OTPM and PM are actually the same register. The usage of this register is determined by OTPC[3] in similar ways as Command 39~42.
- After OTP-ERASE or OTP-PROGRAM operation (Set OTPC[3]=1) , always
  a) remove TST4 power source;
  b) Do a full Vdd ON-OFF cycle; before resuming normal operation.

COMMAND DESCRIPTION

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

UC1682 will convert input RAM data to 12-bits of RGB data. Please refer to command *(22) Set Color Mode* for detail data write sequence. The format of 12 bits RGB data is as following:

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R				G				B			

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Each RGB triplet is stored as 12-bit in the display RAM. Each 12 bits RGB data takes 2 RAM read cycles. The data read will start with the high byte D[11:4] and then low byte {D[3:0],4'b0000}. The read out RGB data is *after-dither* for 56K color and 221K color mode and *after-extension* for 256 color mode.

R3	R2	R1	R0	G4	G3	G2	G1	G0	B2	B1	B0	0	0	0	0
1st Read								2nd Read							

Write/Read Data Byte (command 1/2) operation uses internal Row Address register (RA) and Column Address register (CA). RA and CA can be programmed by issuing *Set Row Address* and *Set Column Address* commands. If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the CA boundary, and system programmers need to set the values of RA and CA explicitly. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and RA will be increased or decreased, depending on the setting of Row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 79), RA will be wrapped around to the other end of RAM and continue.

(3) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	ID	MX	MY	WA	DE	WS	OD	OS

Status flag definitions:

ID: Provide access to ID pin connection status.
MX: Status of register LC[1], mirror X.
MY: Status of register LC[2], mirror Y.
WA: Status of register AC[0]. Automatic column/row wrap around.
DE: Display enable flag. DE=1 when display is enabled
WS : OTP Command Succeeded
OD: OTP Option (Yes/No)
OS : OTP action status

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[6:4]	0	0	**0**	**0**	**0**	**1**	-	CA6	CA5	CA4

Set SRAM column address for read/write access. CA is counted in RGB triplets, not individual SEG electrode.

CA value range: **0~103**

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	**TC1**	**TC0**

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:
00b= -0.05%/°C 01b= -0.10%/°C 10b= -0.15%/°C 11b= -0.20%/°C

(6) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition: 00b ⩽9nF **01b=** 9~12nF 10b= 12~16nF 11b= 16~22nF

(7) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

Pump control definition:

00b=External VLCD **11b=** Internal VLCD (standard)

(8) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[1:0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	R
(Double byte command)	0	0	APC register parameter							

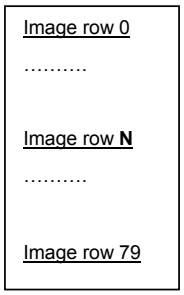
For UltraChip only. Please do NOT use.

(9) SET SCROLL LINE

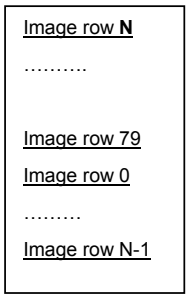
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	**0**	**1**	**0**	**1**	-	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and (79-2xFL). FL is the register value programmed by *Set Fixed Lines* command.



SL=0



SL=N

(10) SET ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address LSB RA [3:0]	0	0	**0**	**1**	**1**	**0**	RA3	RA2	RA1	RA0
Set Row Address MSB RA [6:4]	0	0	**0**	**1**	**1**	**1**	-	RA6	RA5	RA4

Set SRAM row address for read/write access.

Possible value = **0~79**

(11) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0]	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
(Double byte command)	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 255**

(12) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [9:8]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	LC9	LC8

This command is used to enable partial display function.

LC[9:8] : **0X**b: Disable Partial Display, Mux-Rate = CEN+1 (DST, DEN not used.)
10b: Enable Partial Display, Mux-Rate = CEN+1
11b: Enable Partial Display, Mux-Rate = DEN-DST+1+LC[0]x2xFL

(13) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/row wrap around.
0: CA or RA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increment by one step.

AC[1]: Auto-Increment order
0 : column (CA) increment (+1) first until CA reaches CA boundary, then RA will increment by (+/-1).
1 : row (RA) increment (+/-1) first until RA reach RA boundary, then CA will increment by (+1).

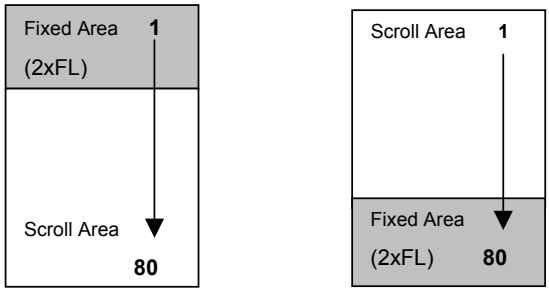
AC[2]: RID, row address (RA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, RID controls whether row address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. When Window Program is enabled (AC[4]=ON), see command description (32) ~ (36) for more details. If WPC[1:0] and WPP[1:0] values are the default values, the behavior of CA, RA auto-increment will be the same, no matter what the setting of AC[4] is.

(14) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines FL [3:0]	0	0	**1**	**0**	**0**	**1**	FL3	FL2	FL1	FL0

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. Set Fixed Lines command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFL rows for mirror Y (MY) is 0 and bottom 2xFL rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0 MY = 1

When partial display mode is activated, the display of these 2xFL lines is also controlled by LC[0].]. Before turning on LC[0], please make sure

MY=0 DST >= FLx2
DEN <= CEN.

MY=1 DST >= 0
DEN <= CEN-FLx2

(15) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate). The line rate is automatically scaled down by 1/2 and 1/3 at Mux-Rate = 38 and 24.

The following are line rates at Mux Rate = 39 ~ 80.

00b: 10.0 Klps 01b: 12.8 klps **10b: 16.0 Klps** 11b: 20.0 Klps
(Klps: Kilo-Line-per-second)

(16) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(17) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

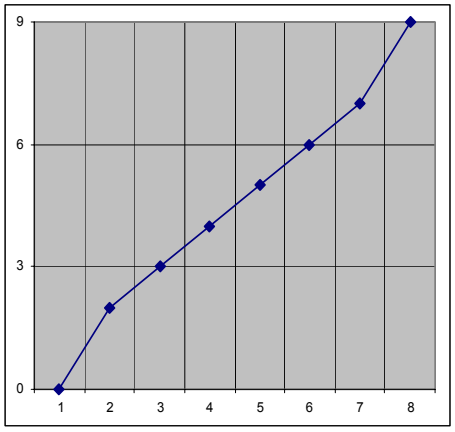
(18) SET DISPLAY ENABLE

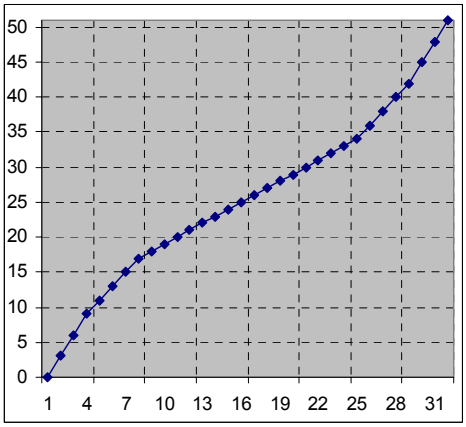
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [4:2]	0	0	**1**	**0**	**1**	**0**	**1**	DC4	DC3	DC2

This command is for programming register DC[4:2].

When DC[2] is set to **0**, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1682 will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3] controls the gray shade modulation modes. UC1682 has two gray shade modulation modes: an 8-sahde mode and a 32-shade mode. The modulation curves are shown below. Horizontal axes are the gray shade data. The vertical axes are the ON-OFF ratio. 9/9 is 100% ON for 8-shade mode, 51/51 is 100% ON for 32-shade mode.





DC[4] enables dither function. Refer to *(22) Set Color Mode* for more information.

0b: Disable **1b:** Enable

(19) SET COLOR MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mask MSK [2:0]	0	0	**1**	**0**	**1**	**1**	**0**	MSK[2:0]		

This command is used for program MSK[2:0] which will control whether the input RGB data will be blocked from updating RGB data in the RAM. (1: Block, 0: Normal. MSK[2:0] = {MSK_R, MSK_G, MSK_B})

Example: Let color mode = 256 color, MSK[2:0] = 100b (MSK_R = 1, MSK_G = 0, MSK_B = 0). There is one pixel to be updated, and the original data for the pixel is 11100110b (RRR-GGG-BB). Suppose the new input RGB data is 00000000b, since R is masked, the data for the pixel would be updated as 11100000b.

(20) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	LC0

This command is used for program LC[2:0] for COM (row) mirror (MY), SEG (column) mirror (MX).

LC[2] controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

LC[1] controls Mirror X (MX): MX is implemented by selecting the CA or 103-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

LC[0] controls whether the soft icon section (0~ 2xFL) is display or not during partial display mode.

(21) SET COLOR PATTERN

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Pattern LC [5]	0	0	**1**	**1**	**0**	**1**	**0**	**0**	**0**	LC5

UC1682 supports on-chip swapping of R⇔B data mapping to the SEG drivers.

LC[5]	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	…	SEG304	SEG311	SEG312
0	B	G	R	B	G	R	…	B	G	R
1	R	G	B	R	G	B	…	R	G	B

The definition of R/G/B input data is determined by LC[7:6], as described in *Set Color Mode* below.

(22) SET COLOR MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mode LC [7:6]	0	0	**1**	**1**	**0**	**1**	**0**	**1**	LC7	LC6

Program color mode and RGB input pattern. Color mode (LC[7:6]) definition:

Dither Options:

DC[4]=1b enables dither function. Refer to *(18) Set Display Enable* for more information.

LC[7:6] = 00b (RRR-GGG-BB, 256 color)

One byte of input data is extended and stored to 12 RAM bits.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R2	R1	R0	G2	G1	G0	B1	B0

LC[7:6] = 01b (RRRR-GGGG-BBBB, 4K color)

1-bit extension for G, 1-bit dither for B. 12 bits of input data is stored to 12 RAM bits.
3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R3	R2	R1	R0	G3	G2	G1	G0
2nd Byte Write Data	B3	B2	B1	B0	R3	R2	R1	R0
3rd Byte Write Data	G3	G2	G1	G0	B3	B2	B1	B0

LC[7:6] = **10b** (RRRRR-GGGGGG-BBBBB, 56K color)

1-bit dither for R/G, 2-bit dither for B. 16 bits input data dithered to 12 RAM bits.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R4	R3	R2	R1	R0	G5	G4	G3
2nd Byte Write Data	G2	G1	G0	B4	B3	B2	B1	B0

LC[7:6] = 11b (RRRRRR-GGGGGGG-BBBBB, 221K color)

2-bit dither per color. 18 out of 24 bits input data is dithered to 12 RAM bits.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R5	R4	R3	R2	R1	R0	--	--
2nd Byte Write Data	G6	G5	G4	G3	G2	G1	G0	--
3rd Byte Write Data	B4	B3	B2	B1	B0	--	--	--

Data Read Sequence

for LC[7:6] = 0.

Data Read Sequence	***D[7:0]***							
1st Byte Read Data	R2	R1	R0	R_M	G2	G1	G0	G_{M2}
2nd Byte Read Data	G_{M1}	B2	B1	B0	0	0	0	0

R/G/B: the input Red/Green/Blue data.

R/G_{MN}: the Red/Green bits mapped from RGB input data.

for LC[7:6] = 1, 2, 3.

Data Read Sequence	***D[7:0]***							
1st Byte Read Data	R_{D3}	R_{D2}	R_{D1}	R_{D0}	G_{D4}	G_{D3}	G_{D2}	G_{D1}
2nd Byte Read Data	G_{D0}	B_{D2}	B_{D1}	B_{D0}	0	0	0	0

$R/G/B_{DN}$: the N-th bit of after-dither Red/Green/Blue input data

Note:

For system designers who want to use their own dithering algorithm, please set LC[7:6] = 10b (56k color mode) and use the following input pattern to bypass on-chip dithering algorithm:

R3-R2-R1-R0-1-G4-G3-G2-G1-G0-1-B2-B1-B0-1-0

No-Dither Options:

DC[4]=0b disables dither function. Refer to *(18) Set Display Enable* for more information.

LC[7:6] = 00b (RRR-GGG-BB, 256 color)

One byte of input data is extended and stored to 12 RAM bits.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R2	R1	R0	G2	G1	G0	B1	B0

LC[7:6] = 01b (RRRR-GGGGG-BBB, 4K color)

12 bits of input data is stored to 12 RAM bits. 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R3	R2	R1	R0	G4	G3	G2	G1
2nd Byte Write Data	G0	B2	B1	B0	R3	R2	R1	R0
3rd Byte Write Data	G4	G3	G2	G1	G0	B2	B1	B0

LC[7:6] = **10b** (RRRRR-GGGGGG-BBBBB, 56K color)

1-bit truncation for R/G, 2-bit for B. 16 bits input data truncated to 12 RAM bits.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R4	R3	R2	R1	R0	G5	G4	G3
2nd Byte Write Data	G2	G1	G0	B4	B3	B2	B1	B0

LC[7:6] = 11b (RRRRRR-GGGGGGG-BBBBB, 221K color)

2-bit truncation for per color. 18 out of 24 bits input data is truncated to 12 RAM bits.

Data Write Sequence	***D[7:0]***							
1st Byte Write Data	R5	R4	R3	R2	R1	R0	--	--
2nd Byte Write Data	G6	G5	G4	G3	G2	G1	G0	--
3rd Byte Write Data	R4	R3	R2	R1	R0	--	--	--

Data Read Sequence

for LC[7:6] = 0.

Data Read Sequence	***D[7:0]***							
1st Byte Read Data	R2	R1	R0	R_M	G2	G1	G0	G_{M2}
2nd Byte Read Data	G_{M1}	B2	B1	B0	0	0	0	0

R/G/B: the input Red/Green/Blue data.

R/G_{MN}: the Red/Green bits mapped from RGB input data.

for LC[7:6] = 1, 2, 3.

Data Read Sequence	***D[7:0]***							
1st Byte Read Data	R_{T3}	R_{T2}	R_{T1}	R_{T0}	G_{T4}	G_{T3}	G_{T2}	G_{T1}
2nd Byte Read Data	G_{T0}	B_{T2}	B_{T1}	B_{T0}	0	0	0	0

$R/G/B_{TN}$: the N-th bit of after-truncated Red/Green/Blue input data

(23) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(24) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

(25) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
(Double byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do not use.

(26) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:

00b= 5 01b=7 10b=8 **11b**=9

(27) RESET CURSOR UPDATE MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Reset Cursor Update Mode AC[3]=0 CA=CR	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

This command is used to reset cursor update mode function.

(28) SET CURSOR UPDATE MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=1 CR=CA	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**

This command is used for set cursor update mode function. When cursor update mode is set, UC1682 will update register CR with the value of register CA. The column address CA will increment with write RAM data operation but the address wraps around will be suspended no matter what WA setting is. However, the column address will not increment in read RAM data operation.

The set cursor update mode can be used to implement “write after read RAM” function. The column address (CA) will be restored to the value, which is before the set cursor update mode command, when resetting cursor update mode.

The purpose of this pair of commands and their features is to support “write after read” function for cursor implementation.

***(29)* SET COM END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(Double byte command)	0	0	*CEN* register parameter							

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD.

***(30)* SET PARTIAL DISPLAY START**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(Double byte command)	0	0	*DST* register parameter							

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

***(31)* SET PARTIAL DISPLAY END**

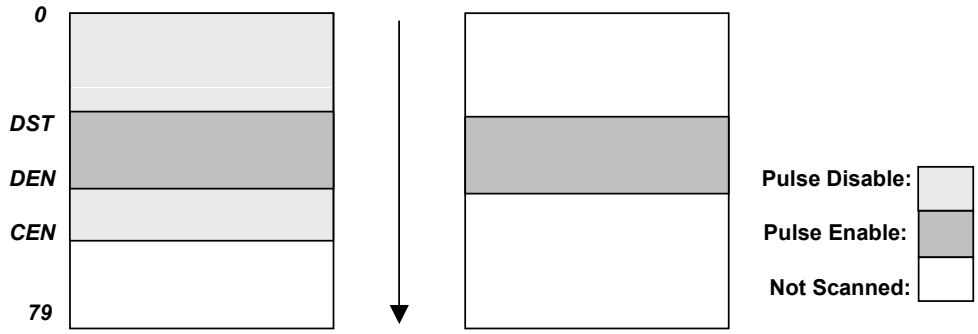
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(Double byte command)			*DEN* register parameter							

This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[9]=1, two partial display modes are possible with UC1682:
LC[8]=1: ON-OFF only, ultra-low-power mode (if Mux-Rate ⩽ 32, set BR=5).
LC[8]=0: Full gray shade low power mode (BR and PM stays the same)

When LC[9:8]=11b, the Mux-Rate is narrowed down to just the range between DST and DEN. When Mux-Rate is under 32, set BR=5, PC[3:2]=01b, and adjust PM to reduce VLCD and achieve the lowest power consumption. When LC[9:8]=10b, the Mux-Rate is still CEN+1. This is achieved by suppressing only the scanning pulses, but not the scanning time slots, for COM electrodes that is outside of DST~DEN. Under this mode, the gray-scale quality of the display is preserved, while the power can be reduced significantly. In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(32) SET WINDOW PROGRAM STARTING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
(Double byte command)			*WPC0[7:0]* register parameter							

This command is to program the starting column address of RAM program window.

(33) SET WINDOW PROGRAM STARTING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (Double byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
			WPP0 register parameter							

This command is to program the starting row address of RAM program window.

(34) SET WINDOW PROGRAM ENDING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (Double byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
			WPC1[7:0] register parameter							

This command is to program the ending column address of RAM program window.

(35) SET WINDOW PROGRAM ENDING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (Double byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
			WPP1 register parameter							

This command is to program the ending row address of RAM program window.

(36) SET WINDOW PROGRAM ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[4]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	AC4

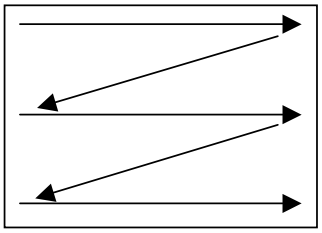
This command is to enable the Window Program Function. Window Program Enable should always be reset when changing the window program boundary and then set right before starting the new boundary program.

Window Program Function can be used to refresh the RAM data in a specified window of SRAM address. When window programming is enabled, the CA and RA increment and wrap around will be automatically adjusted, and therefore allow effective data update within the window.

The direction of Window Program will depend on the WA (AC[0]), RID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting. WA decides whether the program RAM address advances to next row/column after reaching the specified window column / row boundary. RID controls the RAM address incrementing from WPP0 toward WPP1 (RID=0) or reverse the direction (RID=1). Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0). MX results the RAM column address incrementing from 103-WPC0 to 103-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

Auto-increment order = 0 MX=0 RID = 0

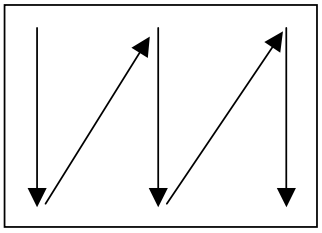
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 1 MX=0 RID = 0

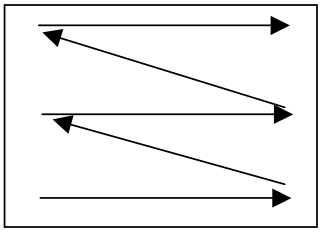
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 0 MX=0 RID = 1

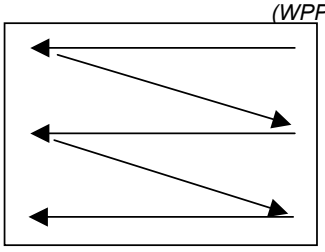
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 0 MX=1 RID = 0

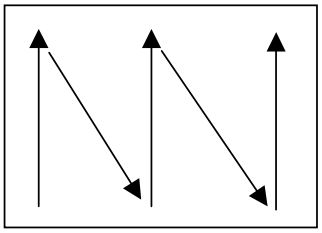
(WPP0,103-WPC0)



(WPP1,103-WPC1)

Auto-increment order = 1 MX=0 RID = 1

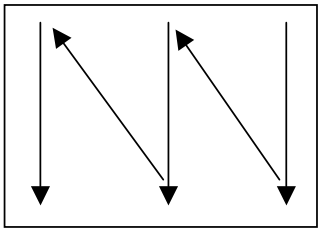
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 1 MX=1 RID = 0

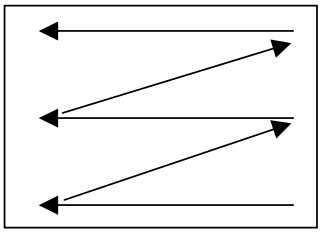
(WPP0,103-WPC0)



(WPP1,103-WPC1)

Auto-increment order = 0 MX=1 RID = 1

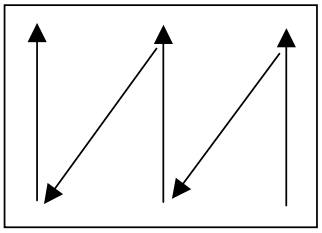
(WPP0,103-WPC0)



(WPP1,103-WPC1)

Auto-increment order = 1 MX=1 RID = 1

(WPP0,103-WPC0)



(WPP1,103-WPC1)

(37) SET OTP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTPC (Double byte command)	0	0	1	0	1	1	1	0	0	0
			OTP0 register parameter							

This command is for OTP operation control:

OTPC[2:0] : OTP command

000 : Sleep
001 : OTP Read
010 : OTP Erase
011 : OTP Program
1XX : For UltraChip use only.

OTPC[3] : OTP Enable (automatically cleared each time after OTP command is done)
OTPC[4] : OTP value valid (ignore OTP value when L)
OTPC[5] : OTP operation mode – Set [5] before OTP external V connection

(38) SET OTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTPM (Double byte command)	0	0	1	0	1	1	1	0	0	1
			OTP1 register parameter							

This command is enable write to each of the 8 individual OTP bits

(39) SET V_{OTP1} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTP2 (Double byte command)	0	0	1	1	1	1	0	1	0	0
			OTP2 register parameter							

This command is for fine tuning V_{OPT1} setting (use with BR=00)

(40) SET V_{OTP2} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTP3 (Double byte command)	0	0	1	1	1	1	0	1	0	1
			OTP3 register parameter							

This command is for fine tuning V_{OTP2} PM setting (use with BR=10)

(41) SET OTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTP4 (Double byte command)	0	0	1	1	1	1	0	1	1	0
			OTP4 register parameter							

(42) SET OTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set OTP5 (Double byte command)	0	0	1	1	1	1	0	1	1	1
			OTP5 register parameter							

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1682 via registers CEN, DST, DEN, and partial display control LC[9:8].

Combined with low power partial display mode and a low bias ratio of 5, UC1682 can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD}/V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=80), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally can not maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1682 supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	5	7	8	9

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per ^{o}C	-0.05	-0.10	-0.15	-0.20

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2]. For good product reliability, it is recommended to keep V_{LCD} under 12V over the entire operating range.

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

Gray shade and color STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best results, software or OTP based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning.

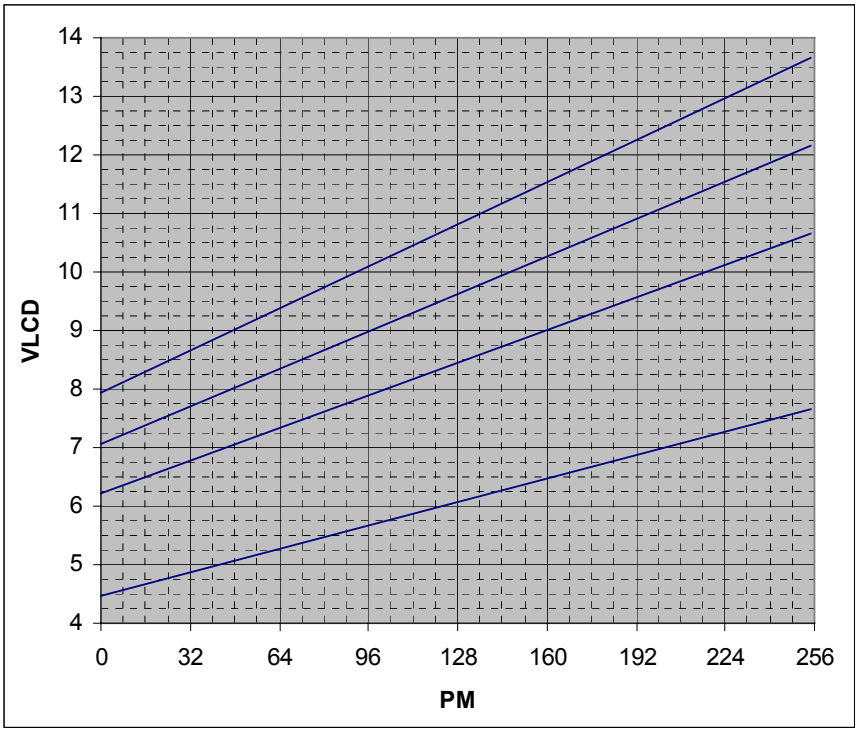
For applications where mechanical manual fine tuning of V_{LCD} becomes necessary, then V_{BIAS} pin may be used with an external trim pot to fine tune the V_{LCD}.

LOAD DRIVING STRENGTH

The power supply circuit of UC1682 is designed to handle LCD panels with load capacitance up to ~20nF when V_{DD2} = 2.5V. For larger LCD panels use higher V_{DD} and COF packaging.

20nF is also the recommended limit for LCD panel size for COG applications.

V_{LCD} QUICK REFERENCE



VLCD-PM relationship for different BR setting at 25°C.

BR	C_{V0} (V)	C_{PM} (mV)	PM	V_{LCD} (V)
5	4.474	12.50	0	4.47
			255	7.66
7	6.206	17.50	0	6.21
			255	10.67
8	7.070	20.00	0	7.07
			255	12.17
9	7.931	22.50	0	7.93
			255	13.67

Note:

1. For good product reliability, keep VLCD under 10.3V at room temperature, and keep VLCD under 10.5V under all temperature and operating conditions.
2. The integer values of BR above are for reference only and probably have slight shift.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

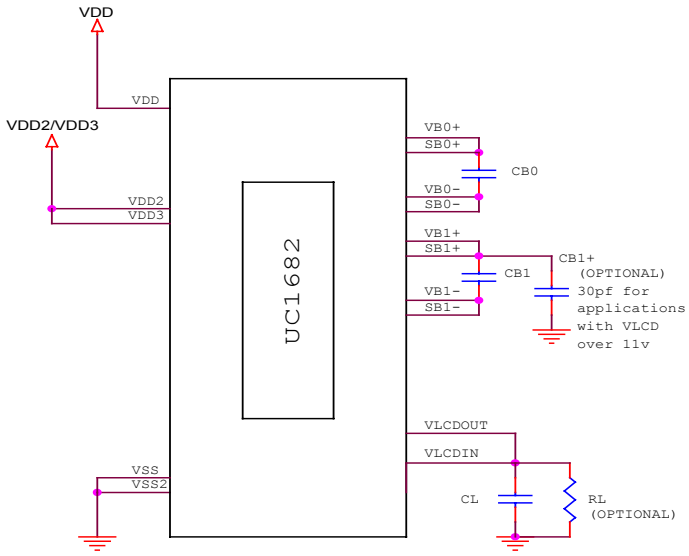


FIGURE 3: Reference circuit using internal Hi-V generator circuit

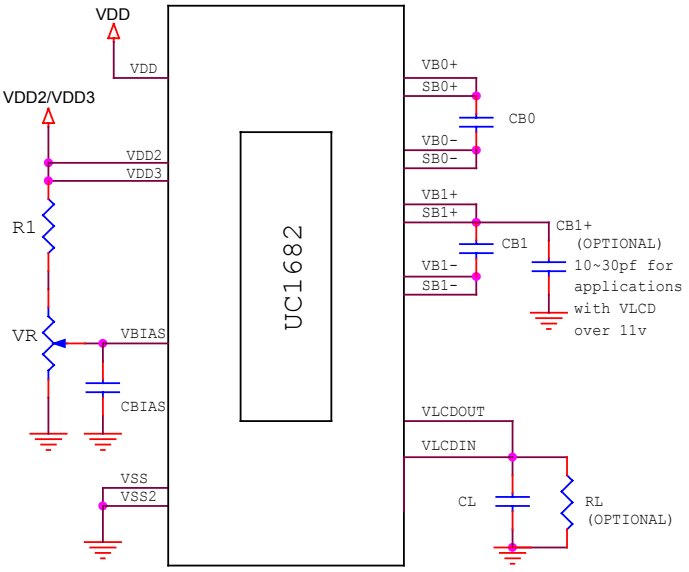


FIGURE 4: Reference circuit using external Bias source

Note

Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

- C_B: 150 ~ 250x LCD load capacitance or 2.2µF (2V), whichever is higher.
- C_L: 5nF ~ 50nF (16V) is appropriate for most applications.
- R_L: 3 ~ 10M Ω, RC time constant of CL x RL should be roughly 0.2~1sec
- V_R: 1M Ω
- R_1: 330K Ω
- C_{BIAS}: 10nF ~ 0.1uF is the recommended default value (not required for OTP version).

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1682 contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 38, frame rate is calculated as:

Frame Rate = Line-Rate / Mux-Rate.

When Mux-Rate is lowered to 38 (and 24), line rate will be scaled down by 2 (and 3) times automatically reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Frame rate 175Hz is recommended for 32-shade mode. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When switching from 32-shade modulation to 8-shade modulation, line rate will be scaled down automatically by ~30%. Under most situations, flicker behavior is similar between these two different modulation schemes.

When switching from 32-shade modulation to 8-shade modulation, line rate will be scaled down automatically by ~35%. Under most situations, flicker behavior is similar between these two different modulation schemes. However, it is always recommended to test each mode to make sure flicker behavior is acceptable

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG drivers are in Idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where x=1~80, refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display Enable* command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1682 will put itself into Sleep mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1682 will first exit from Sleep mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FL specifies a region of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can be used to implement fixed region when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1682 provides flexible control of Mux Rate and active display area. Please refer to command *Set COM End, Set Partial Display Start*, and *Set Partial Display End* for more detail.

GRAY-SHADE MODULATION MODE

UC1682 has two gray-shade modulation modes: 32-shade and 8-shade.

The 8-shade mode will consume ~30% less power than the 32-shade mode, and can be used for situations where power consumption is more critical than color fidelity.

Changing gray-shade modulation mode does not affect the content of SRAM display buffer, and the image data will remain the same after switching back and forth between 8-shade mode and 32-shade mode.

INPUT COLOR FORMATS

UC1682 supports the following four different input color formats.

256C (8-bit/RGB): This is the most compact color mode, and is intended to minimize the bus cycle required to refresh the display buffer. On-chip extension circuit will automatically expand the input RGB data into on-chip RAM buffer format.

4KC (12-bit/RGB): In this color mode, G will be extended while B will be dithered, and the input data will be converted into 4R-5G-3B format before they are stored to display RAM.

56KC (16-bit/RGB): On-chip dither engine will convert the input data into internal 12-bit-per-RGB pixel format and store it to on-chip display RAM. This is the default mode.

221KC (24-bit/RGB): On-chip dither engine will convert input data into 4R-5G-3B format and store it to on-chip display RAM. This mode provides the smoothest shades and the most vivid color in the LCD.

Changing color mode does not affect the content already stored in the display buffer RAM. Users can use several color modes together in real time.

For example, the menu portion can be painted in 256-color mode for fast update speed, and then switch to 221K-color mode, together with window programming option, and take advantage of built-in dither engine to produce smooth graphics images.

LAYOUT CONSIDERATIONS FOR COM SIGNALS

Since the COM scanning pulse of UC1682 can be as short as 30µS, it is critical to control the RC delay of COM signal to minimize distortion of COM scanning pulse.

For the best image quality, limit the worst case of RC delay of COM signal as calculated below.

$$(R_{ROW} / 2.7 + R_{COM} + R_{OUT}) \times C_{ROW} < 2\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area

R_{OUT}: COM output impedance

In addition, please make sure

$$| RC_{MAX} - RC_{MIN} | < 0.3 \times RC_{MAX}$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

LAYOUT CONSIDERATIONS FOR SEG SIGNALS

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase of SEG direction crosstalk.

Please limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.5\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / #_of column, C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance

LAYOUT CONSIDERATIONS FOR SEG SIGNALS

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase of SEG direction crosstalk.

For good image quality, please limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.4\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / #_of column, C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance

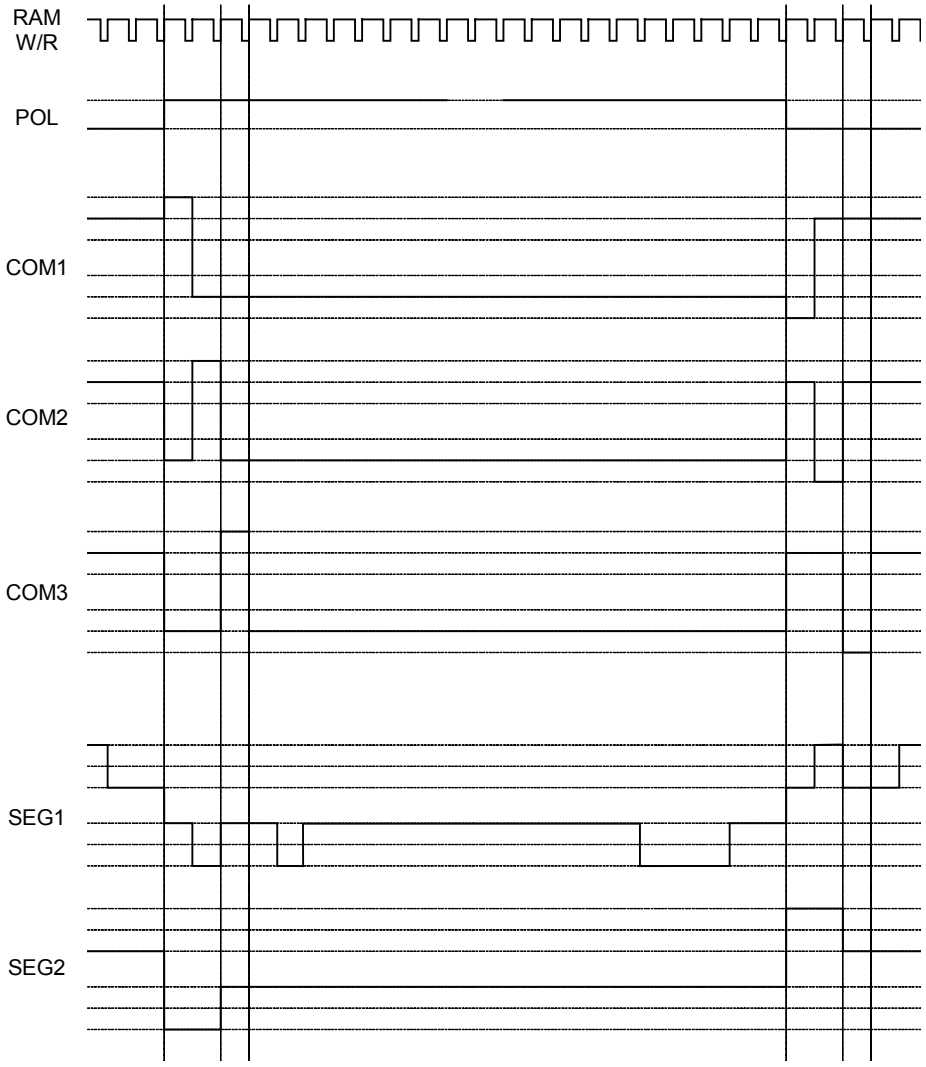


FIGURE 5: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1682 supports two parallel bus protocols, in either 8-bit or 4-bit bus width, and three serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

Bus Type		8080		6800		S8 (4wr)	S8uc (3wr)	S9 (3wr)
Width		8-bit	4-bit	8-bit	4-bit	Serial		
Access		Read/Write				Write Only		
Control & Data Pins	BM[1:0]	10	00	11	01	00	00	01
	D[7:6]	Data	0X	Data	0X	10	11	1X
	CS[1:0]	Chip Select						
	CD	Control/Data						–
	WR0	$\overline{WR}$		R/$\overline{W}$		–		
	WR1	$\overline{RD}$		EN		–		
	D[5:4]	Data	–	Data	–	–		
	D[3:0]	Data	Data	Data	Data	D0=SCK, D3=SDA		

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

	CS Disable Interface	CS Init bus state	CD 1<=>0 Init bus state	CD 1=>0 init color mapping	RESET Init bus state	RESET init color mapping
8-bit	✓	–	–	✓	✓	✓
4-bit	✓	–	✓	✓	✓	✓
S8 or S9	✓	✓	–	✓	✓	✓
S8uc	✓	–	✓	✓	✓	✓

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- CD refers to CD transitions within valid CS window. CD = 0 means write command or read status.
- CS / CD Sync / RESET can be used to initialize bus state machine (like 4 bits / S8 / S9).
- RESET can be pin reset / soft reset / power on reset.
- CD can be used to initialize the multi-byte input RGB format to/from on-chip SRAM mapping.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1682 internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in 8-bit mode or 4-bit mode, by either *Set CA,* or *Set RA* command, a dummy read cycle needs to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

8-BIT & 4-BIT BUS OPERATION

UC1682 supports both 8-bit and 4-bit bus width. The bus width is determined by pin BM[1].

4-bit bus operation exactly doubles the clock cycles of 8-bit bus operation, MSB followed by LSB, including the dummy read, which also requires two clock cycles. The bus cycle of 4-bit mode is reset each time CD pin changes state (when CS is active).

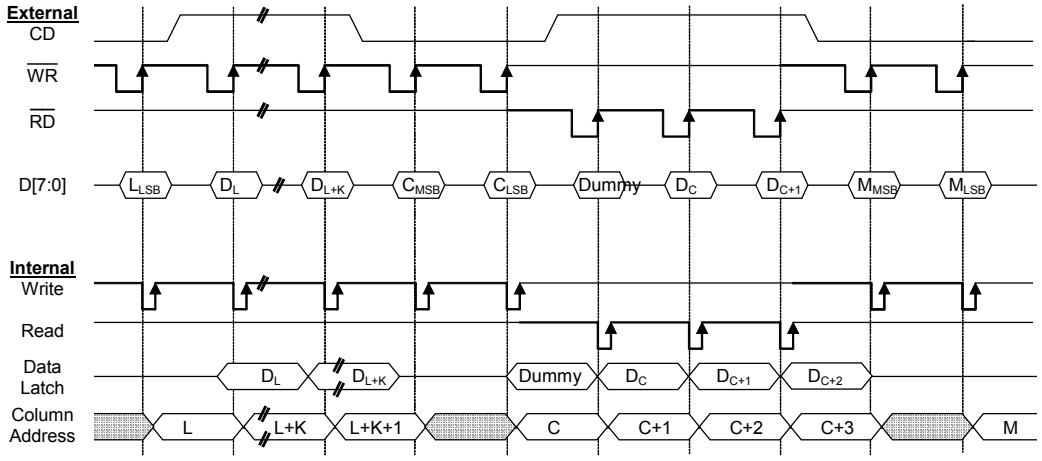


FIGURE 6: 8 bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1682 supports three serial modes, one 4-wire SPI mode (S8), one compact 3/4-wire mode (S8uc) and one 3-wire SPI mode (S9). Bus interface mode is determined by the wiring of the BM[1:0] and D[7:6]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

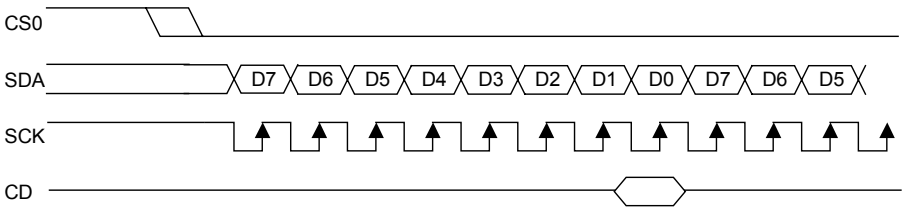


FIGURE 7.a: 4-wire Serial Interface (S8)

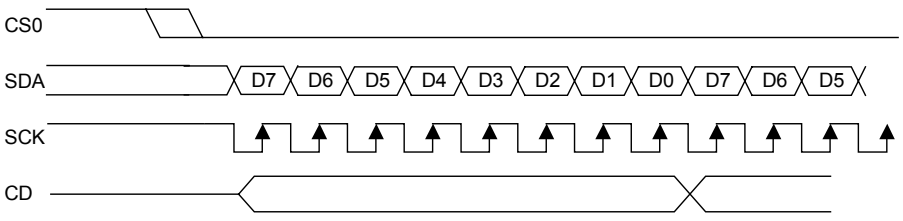


FIGURE 7.b: 3/4-wire Serial Interface (S8uc)

S8UC (3/4-WIRE) INTERFACE

Only write operations are supported in this 3/4-wire serial mode. The data format is identical to S8. However, in addition to CS pins, CD pin transitions will also reset the bus cycle in this mode. So, if CS pins are hardwired to enable chip-select, the bus can work properly with only three signal pins.

S9 (3-WIRE) INTERFACE

Only write operations are supported in this 3-wire serial mode. Pin CS[1-0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

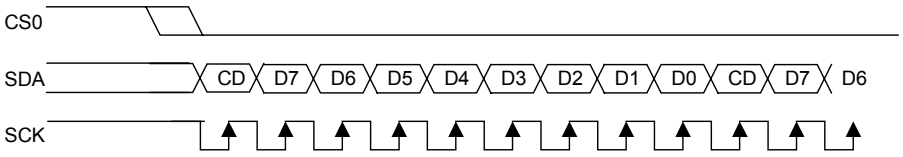


FIGURE 7.C: 3-wire Serial Interface (S9)

HOST INTERFACE REFERENCE CIRCUIT

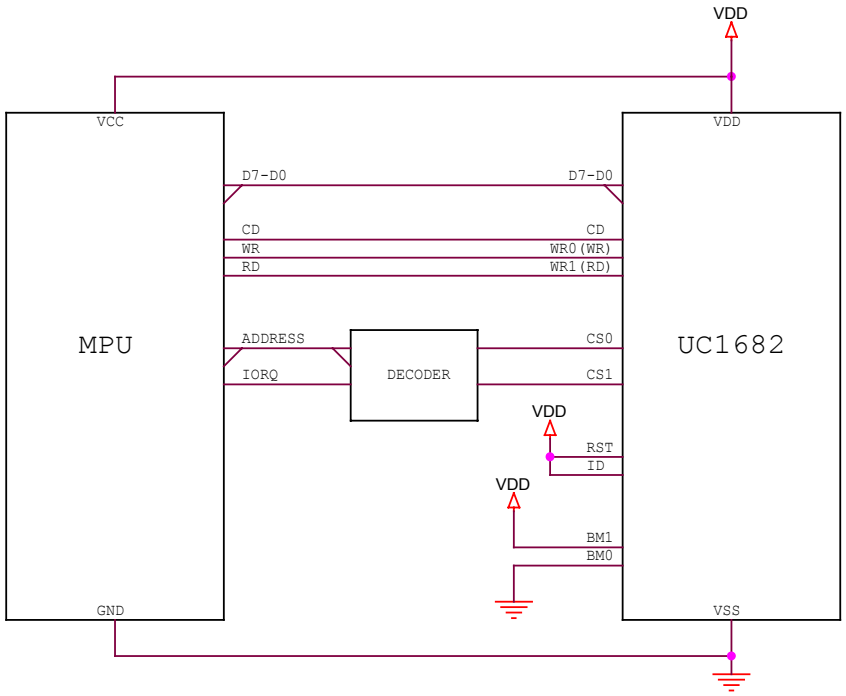


FIGURE 8: 8080/8bit parallel mode reference circuit

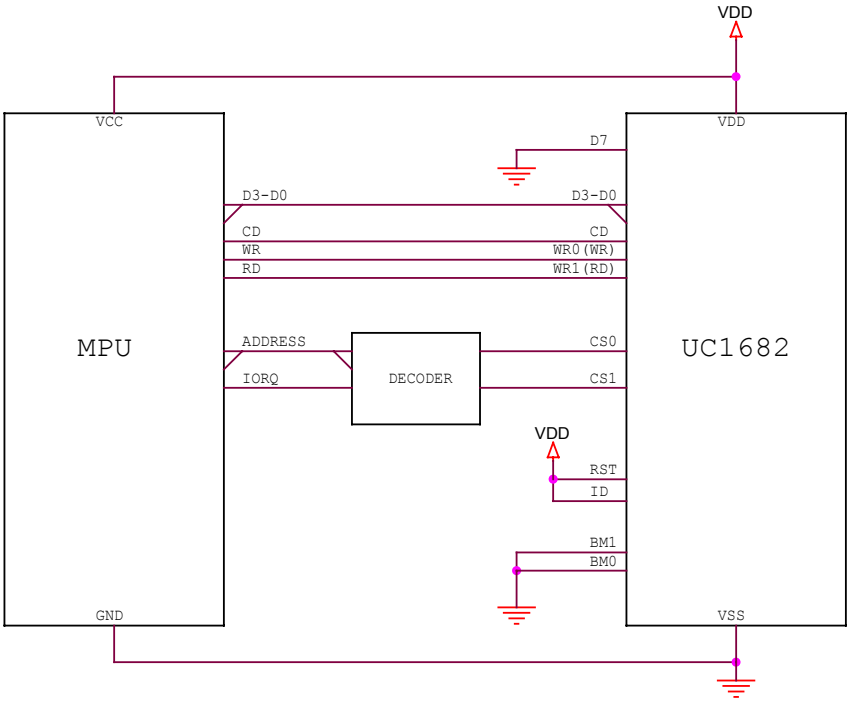


FIGURE 9: 8080/4bit parallel mode reference circuit

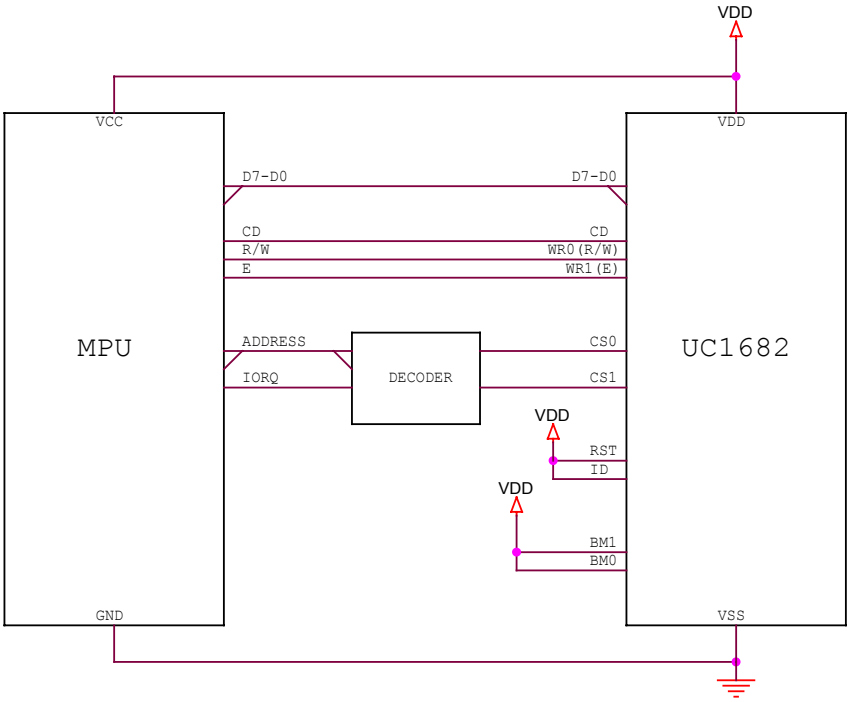


FIGURE 10: 6800/8bit parallel mode reference circuit

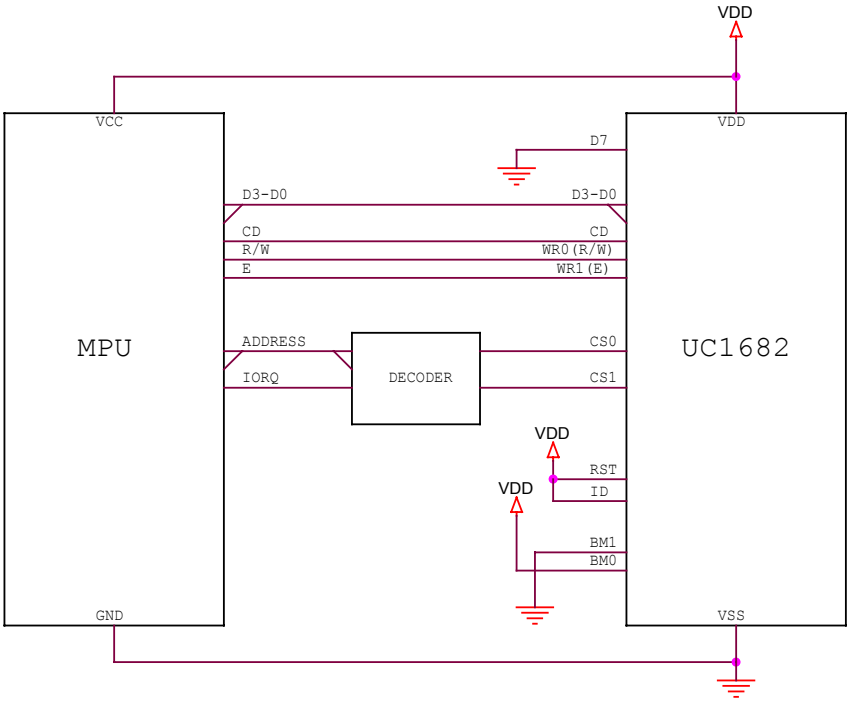


FIGURE 11: 6800/4bit parallel mode reference circuit

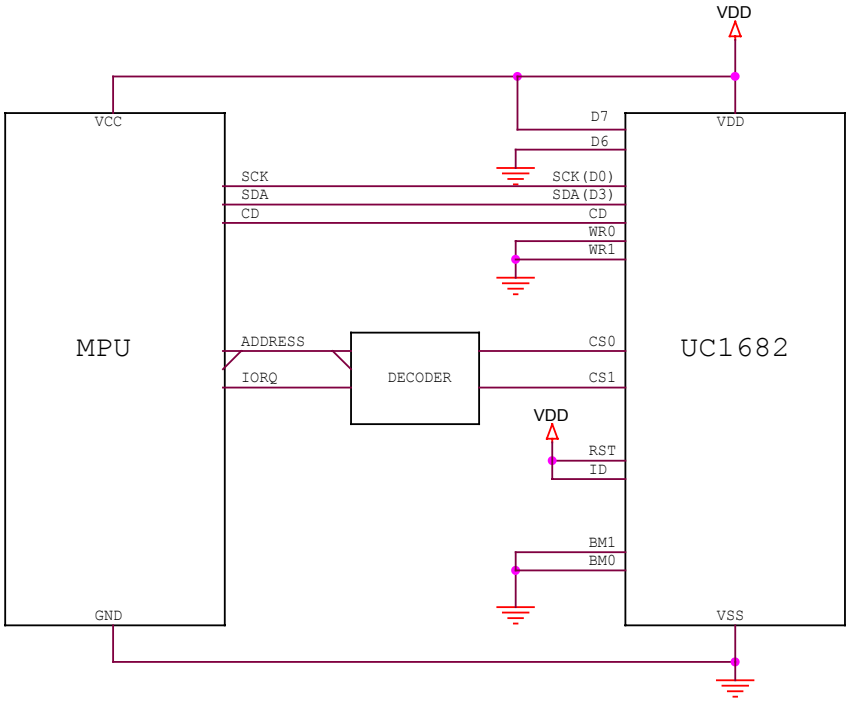


FIGURE 12: 4-Wires SPI (S8) serial mode reference circuit

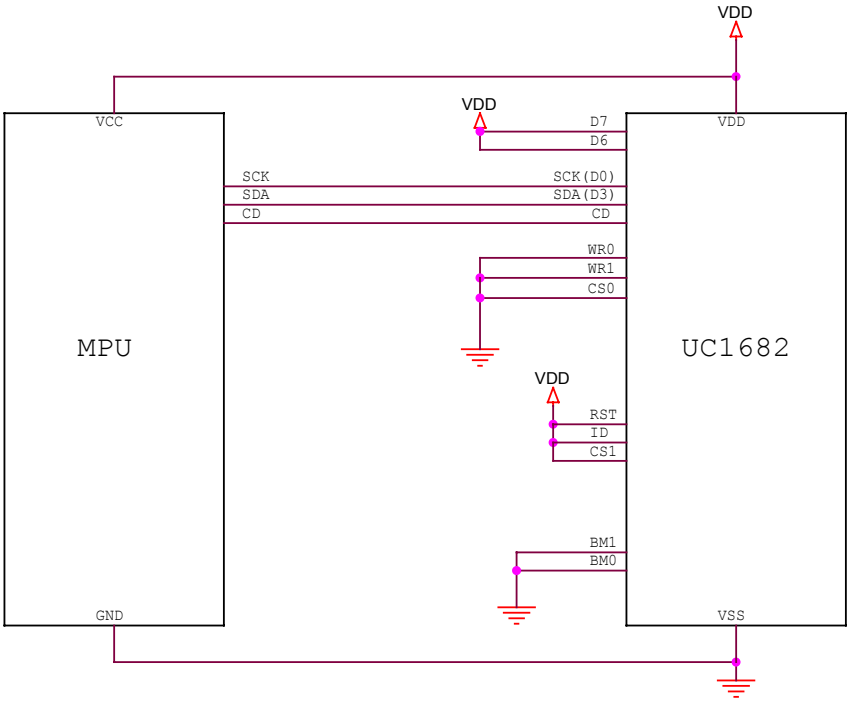


FIGURE 13: 3/4-Wires SPI (S8uc) serial mode reference circuit

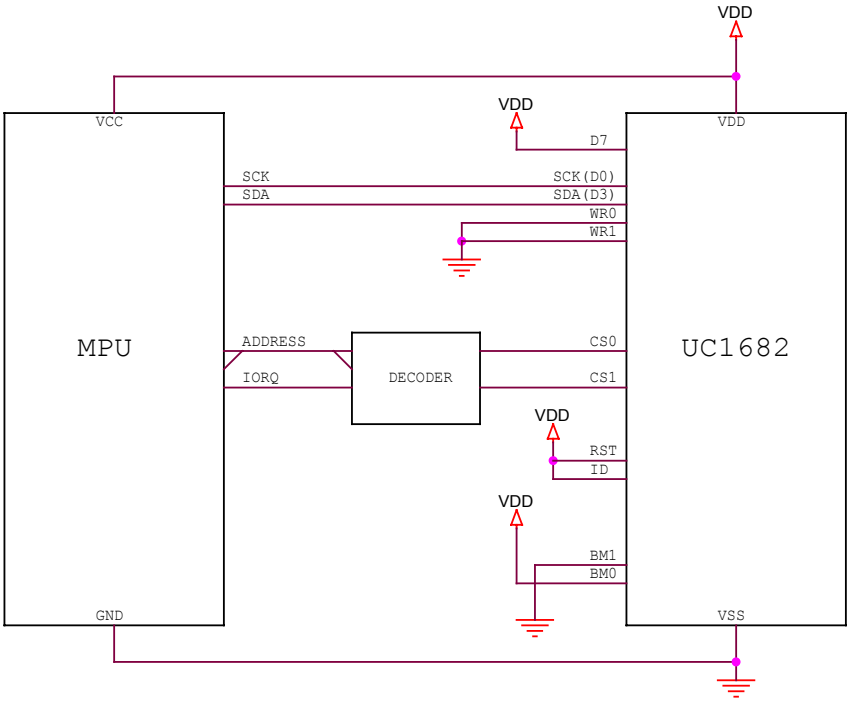


FIGURE 14: 3-Wires SPI (S9) serial mode reference circuit

Note

- ID pin is for production control. The connection will affect the content of D[7] when using *Get Status* command. Connect to V_{DD} for "H" or V_{SS} for "L".
- RST pin is optional. When RST pin is not used, connect the pin to V_{DD}.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data (depend on color mode) are stored to a dual port static RAM (RAM, for Display Data RAM) organized as 80x104X12.

After setting CA and RA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *Set Row Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (103), and system programmers need to set the values of RA and CA explicitly.

If WA is ON (1), when CA reaches the end of a row, CA will be reset to 0 and RA will increment or decrement, depending on the setting of row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 79), RA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (103–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FL) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FL=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field

Line = *SL*

Otherwise

Line = Mod(*Line*+1, 80)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches *80*. Effects such as scrolling can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field

Line = Mod(*SL* + *MUX-1*, *80*)
where MUX = CEN + 1

Otherwise

Line = Mod(*Line-1* , *80*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM are not affected by MY.

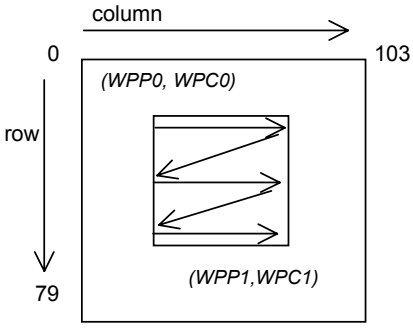
WINDOW PROGRAM

Window program is designed for data write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and then enable AC[4]. After AC[4] sets, data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). AC[4] should be cleared after any modification of window boundary registers and then set again in order to initialize another window program.

The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or row direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial column address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

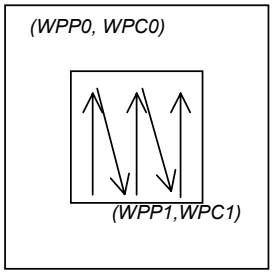
Example1:

AC[2:0] = 001 MX=0



Example 2:

AC[2:0] = 111 MX = 0



RAM

Row Adderss	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
00H	COM1	COM65	COM80	COM16
01H	COM2	COM66	COM79	COM15
02H	COM3	COM67	COM78	COM14
03H	COM4	COM68	COM77	COM13
04H	COM5	COM69	COM76	COM12
05H	COM6	COM70	COM75	COM11
06H	COM7	COM71	COM74	COM10
07H	COM8	COM72	COM73	COM9
08H	COM9	COM73	COM72	COM8
09H	COM10	COM74		COM7
0AH	COM11	COM75		COM6
0BH	COM12	COM76		COM5
0CH	COM13	COM77		COM4
0DH	COM14	COM78		COM3
0EH	COM15	COM79		COM2
0FH	COM16	COM80		COM1
10H	COM17	COM1		COM80
11H	COM18	COM2		COM79
12H	COM19	COM3		COM78
13H	COM20	COM4		COM77
14H	COM21	COM5		COM76
15H	COM22	COM6		COM75
16H	COM23	COM7		COM74
17H	COM24	COM8		COM73
18H	COM25	COM9		COM72
19H	COM26	COM10		
1AH	COM27	COM11		
1BH	COM28	COM12		
1CH	COM29	COM13		
38H				COM40
39H				COM39
3AH				COM38
3BH				COM37
3CH				COM36
3DH				COM35
3EH				COM34
3FH				COM33
40H				COM32
41H				COM31
42H				COM30
43H				COM29
44H				COM28
45H				COM27
46H				COM26
47H				COM25
48H				COM24
49H				COM23
4AH				COM22
4BH	COM76	COM60	COM5	COM21
4CH	COM77	COM61	COM4	COM20
4DH	COM78	COM62	COM3	COM19
4EH	COM79	COM63	COM2	COM18
4FH	COM80	COM64	COM1	COM17

MX	SEG1	SEG2	SEG3	SEG4	SEG5			SEG308	SEG309	SEG310	SEG311	SEG312
0												
1	SEG312	SEG311	SEG310	SEG309	SEG308			SEG5	SEG4	SEG3	SEG2	SEG1

Example for memory mapping: let MX = 0, MY = 0, SL = 0, LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 56K color), according to the data shown in the above table (R: 11111b, G: 111111b, B: 11111b):

⇒ 1st Byte write data: 11111111b

⇒ 2nd Byte write data: 11111111b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1682 has two different types of Reset:
Power-ON-Reset and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about 5~10mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1682 enters RESET sequence:

- Operation mode will be "Reset"
- System Status bits RS and BZ will stay as "1" until the Reset process is completed. When RS=1, the IC will only respond to *Read Status* command. All other commands are ignored.
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1682 has three operating modes (OM):
Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	OFF	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

For maximum energy utilization, Sleep mode is designed to retain charges stored in external capacitors C_{B0}, C_{B1}, and C_L. To drain these capacitors, use Reset command to activate the on-chip draining circuit.

Action	Mode	OM
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11
Reset command or RST_ pin pulled "L" Power ON Reset	Reset	00

Table 5: OM changes

Even though UC1682 consumes very little energy in Sleep mode (typically 5uA or less); however, since all capacitors are still charged, the leakage through COM drivers may damage the LCD over the long term. It is therefore recommended to use Sleep mode only for brief Display OFF operations, such as full-frame screen updates, and to use RESET for extended screen OFF operations.

EXITING SLEEP MODE

UC1682 contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1682 internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1682 power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 5~ 10 ms before the CPU starting to issue commands to UC1682. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands. However, while turning on V_{DD}, $V_{DD2/3}$ should be started not later than V_{DD}.

Delay allowance between V_{DD} and $V_{DD2/3}$ is illustrated as Figure 15-1.

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+}, C_{BX-}, and C_L from damaging the LCD, when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K Ω for both V_{LCD} and V_{B+}. It is recommended to wait *3* x *RC* for V_{LCD} and *1.5 x RC* for V_{B+}. For example, if C_L is 15nF, then the draining time required for V_{LCD} is 0.5~1mS.

When internal V_{LCD} is not used, UC1682 will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

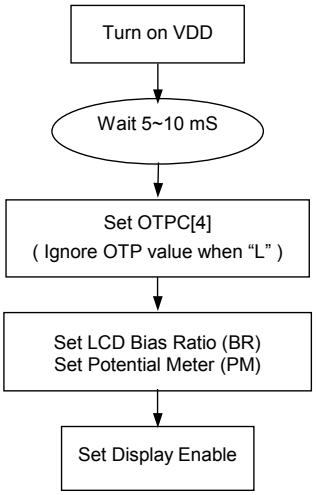


Figure 15: Reference Power-Up Sequence

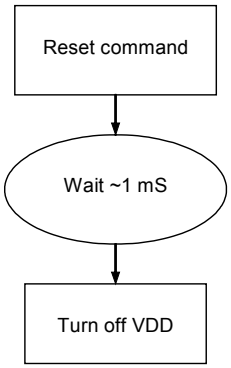


Figure 16: Reference Power-Down Sequence

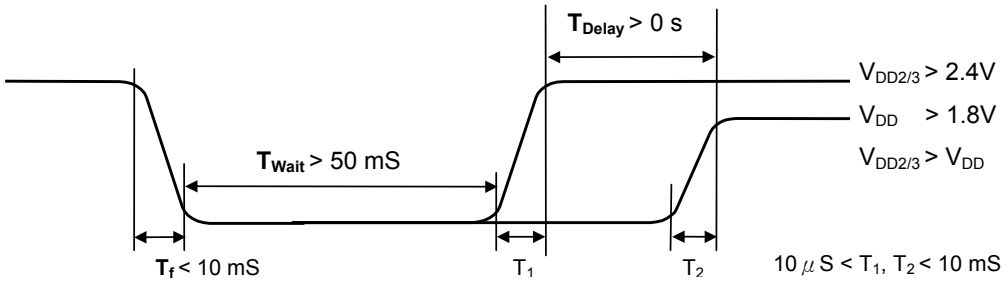


Figure 15-1: Delay allowance and Power Off-On Sequence

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

Type Required: These items are required
Customer: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait 5~10ms after V_{DD} is ON
R	0 0	0 0	1 0	0 0	1 0	1 0	1 0	0 0	0 0	0 0	(37) Set OTP operation Control. (Double-type Command)	Ignore OTP value
C	0	0	0	0	1	0	0	1	#	#	(5) Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	(20) Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	(15) Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	(22) Set Color Mode	
C	0	0	1	1	1	0	1	0	#	#	(26) Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	(11) Set V_{BIAS} Potentiometer	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	(18) Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(23) System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1ms before V_{DD} OFF

BRIEF DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	(18) Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	(18) Set Display Enable	

* This is only recommended for very brief display OFF (under 10mS).
If image becomes unstable use the *Extended Display OFF* approach shown below.

EXTENDED DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(23) System Reset.	C_{B1}, C_{B1}, C_{LCD} discharged.
–	–	–	–	–	–	–	–	–	–	–		Extended display OFF *Z z z z . . .*
–	–	–	–	–	–	–	–	–	–	–		System waking up
R											Repeat power-up sequence	Repeat power up register setting sequence
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the RESET state.)
R	0	0	1	0	1	0	1	1	1	1	(18) Set Display Enable	

* The sequence is basically the same as the power up sequence, except *Power-ON Reset* is replaced by *System Reset* command, and an extended idle time in between.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
V_{LCD}	LCD Driving voltage (-25^{O}C ~ +75^{O}C)	-0.3	+12.0	V
V_{IN}	Digital input signal	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Notes

1. V_{DD} based on V_{SS} = 0V
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.8		3.3	V
$V_{DD2/3}$	Supply for bias & pump		2.4		3.3	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant 2.4V$, 25°C		9.9	10.5	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant 2.4V$, 25°C	0.9		1.5	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
C_{IN}	Input capacitance			5	10	pF
C_{OUT}	Output capacitance			5	10	pF
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 9.9V		1.5	3.0	kΩ
$R_{0(COM)}$	COM output impedance	V_{LCD} = 9.9V		2.0	4.0	KΩ
f_{LINE}	Average Line rate	LC[4:3] = 11b	18.4	20	22.4	Klps

Note: When V_{DD} < 2.0, letting V_{IL} = 0 and V_{IH} = V_{DD} is recommended.

POWER CONSUMPTION

V_{DD} = 2.8V, Bias Ratio = 8, PM = 142, V_{LCD} = 9.9V, Line Rate =10b, PL = 11b, MR =80, Bus mode =6800, C_L = 5nF~50nF, C_B = 2μF. All SEG/COM outputs are open-circuit.

Display Pattern	Conditions	Typ. (μA)	Max. (μA)
All-OFF	Bus = idle	665	2000
2-pixel checker	Bus = idle	860	2000
V_{LCD}	Bus = idle (standby current)	-	5

AC CHARACTERISTICS

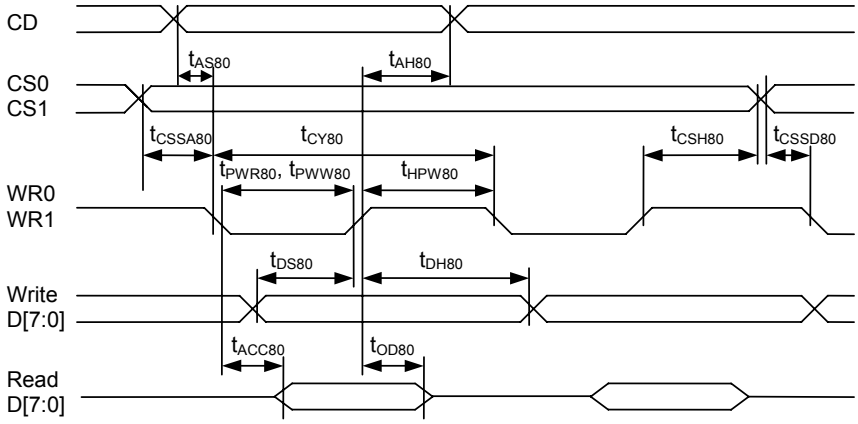


FIGURE 17: Parallel Bus Timing Characteristics (for 8080 MCU)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 15	–	ns
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	ns
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		70 70	–	ns
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		40 40	–	ns
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 70 40 70 40	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 15	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 25	80 40	ns
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		ns

($1.8V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 30	–	ns
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 280 160 280 160	–	ns
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits (read)		140 140	–	ns
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits (write)		80 80	–	ns
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		60 30	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	- 50	160 80	ns
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		20 20 40		ns

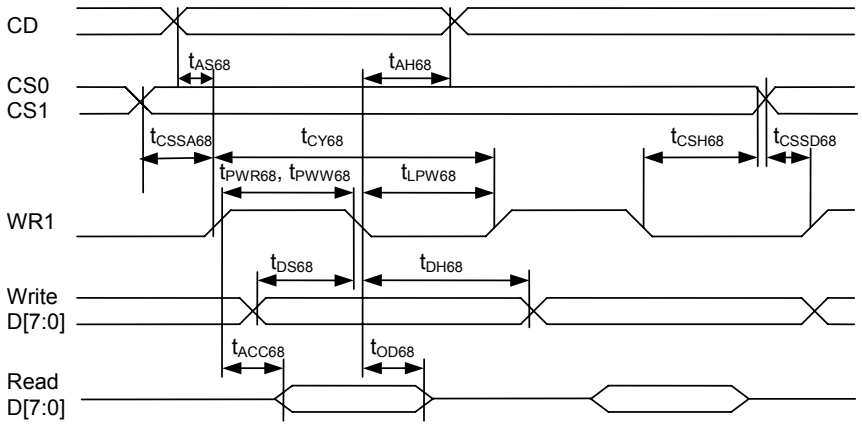


FIGURE 18: Parallel Bus Timing Characteristics (for 6800 MCU)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 20	–	ns
T_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	ns
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		70 70	–	ns
t_{PWW68}		Pulse width 8 bits (write) 4 bits		40 40	–	ns
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 70 40 70 40	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 15	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 25	80 40	ns
t_{CSSA68} t_{CSSD68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		ns

($1.8V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 40	–	ns
T_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 280 160 280 160	–	ns
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		140 140	–	ns
t_{PWW68}		Pulse width 8 bits (write) 4 bits		80 80	–	ns
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 80 140 80	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		60 30	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	- 50	160 80	ns
T_{CSSA68} T_{CSSD68} T_{CSH68}	CS1/CS0	Chip select setup time		20 20 40		ns

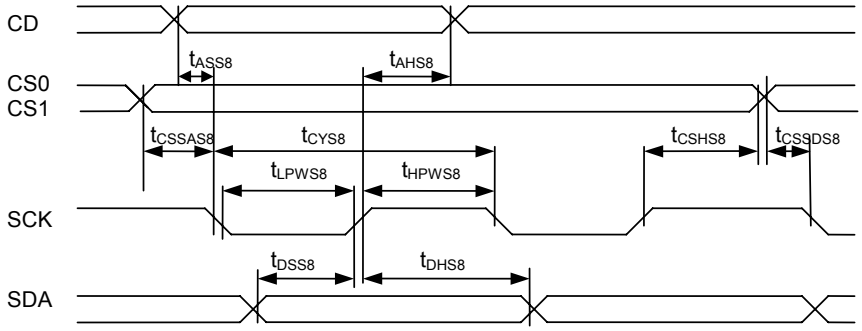


FIGURE 19: Serial Bus Timing Characteristics (for S8)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	ns
t_{AHS8}		Address hold time		15	–	ns
t_{CYS8}	SCK	System cycle time		80	–	ns
t_{LPWS8}		Low pulse width		35	–	ns
t_{HPWS8}		High pulse width		35	–	ns
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 20	–	ns
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10 20		ns

($1.8V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	ns
t_{AHS8}		Address hold time		30	–	ns
t_{CYS8}	SCK	System cycle time		160	–	ns
t_{LPWS8}		Low pulse width		70	–	ns
t_{HPWS8}		High pulse width		70	–	ns
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		60 40	–	ns
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1/CS0	Chip select setup time		20 20 40		ns

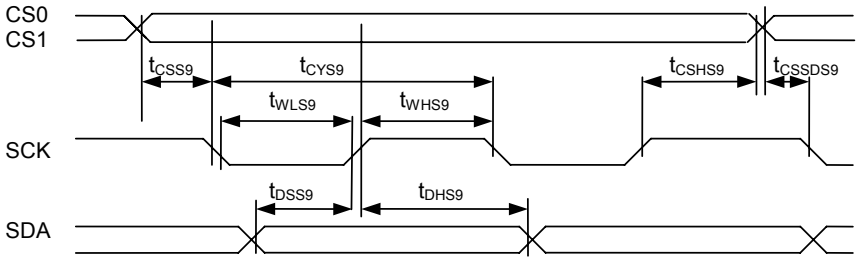


FIGURE 20: Serial Bus Timing Characteristics (for S9)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		80	–	ns
t_{LPWS9}		Low pulse width		35	–	ns
t_{HPWS9}		High pulse width		35	–	ns
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 20	–	ns
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10 20		ns

($1.8V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		160	–	ns
t_{LPWS9}		Low pulse width		70	–	ns
t_{HPWS9}		High pulse width		70	–	ns
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		60 40	–	ns
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS1/CS0	Chip select setup time		20 20 40		ns

FIGURE 21: Reset Characteristics

($1.8V \leq V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		500	–	µS

PHYSICAL DIMENSIONS

PAD COORDINATES

DIE SIZE:
13.944mm x 1.494mm

DIE THICKNESS:
0.5mm

BUMP HEIGHT:
17µm ±1µm (within die)

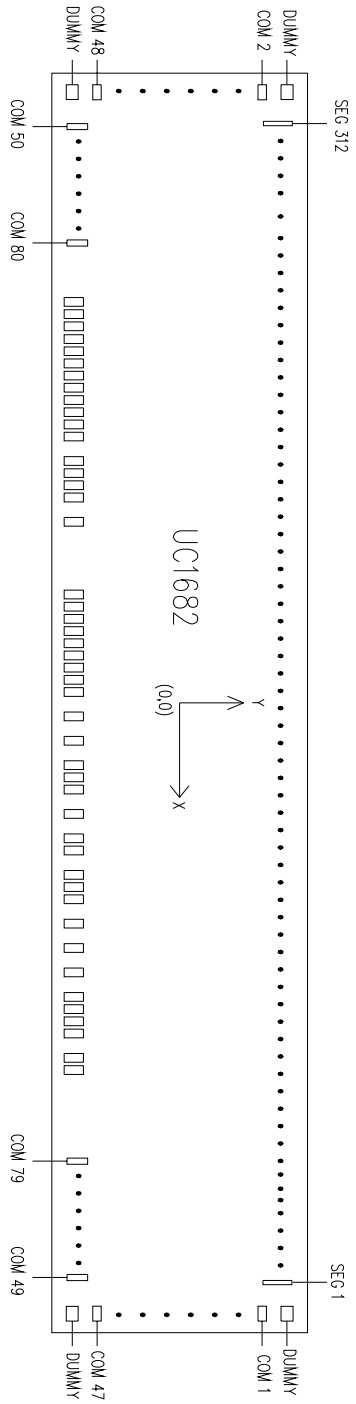
MINIMUM BUMP PITCH:
SEG: 41.5µm (Typ.)
COM: 50.0µm (Typ.)

MINIMUM BUMP GAP:
17µm (Typ.)

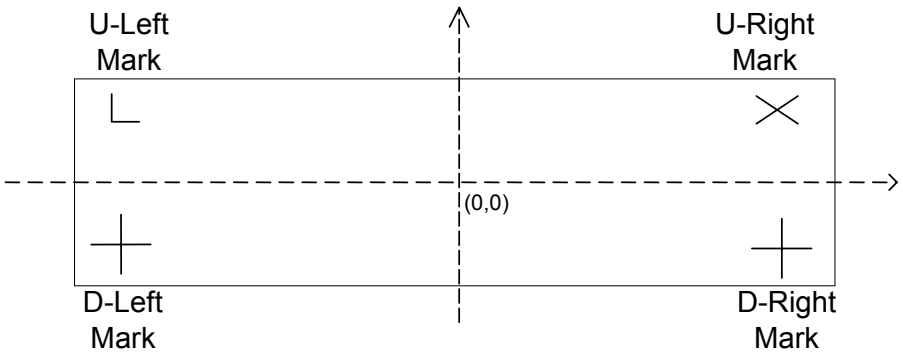
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

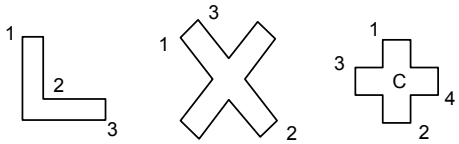
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

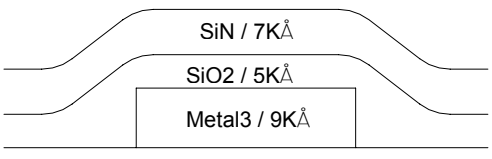
Alignment mark is on Metal3 under Passivation.

COORDINATES:

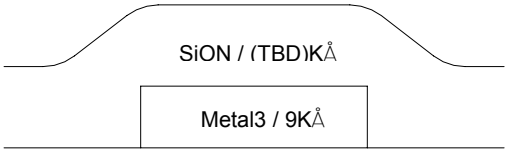
	U-Left Mark		U-Right Mark	
	X	Y	X	Y
1	-6887.1	615.7	6853.2	608.5
2	-6879.1	606.5	6882.4	589.2
3	-6846.2	598.5	6858.1	613.4

	D-Left Mark		D-Right Mark	
	X	Y	X	Y
1	-5690.3	-612.1	5535.4	-612.1
2	-5678.3	-667.2	5547.4	-667.2
3	-5701.8	-633.7	5523.9	-633.7
4	-5666.8	-645.7	5558.9	-645.7
C	-5684.3	-639.7	5541.4	-639.7

TOP METAL AND PASSIVATION:



FOR NON-OTP PROCESS CROSS-SECTION



FOR OTP PROCESS CROSS-SECTION

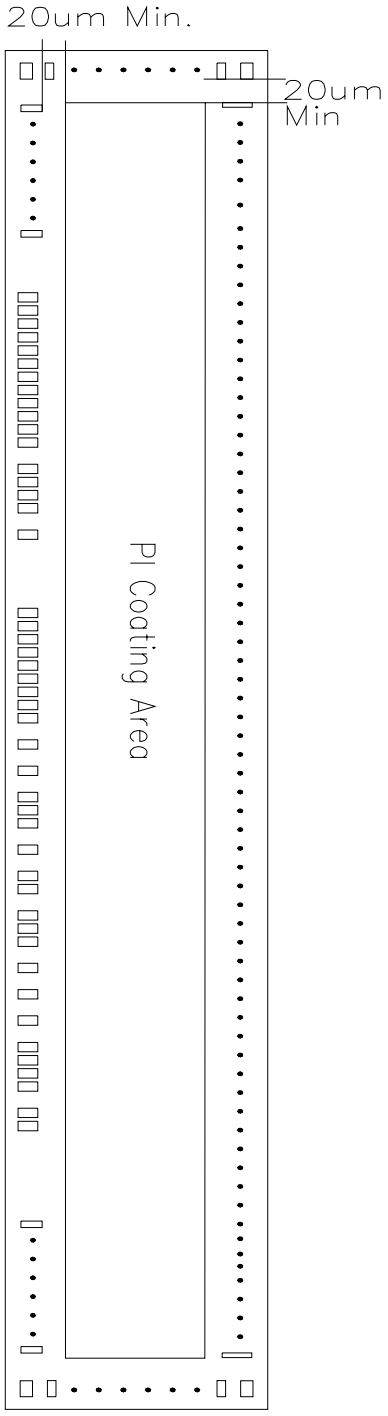
PI INFORMATION

PI THICKNESS:

3.6 ± 0.4 µm

MINIMUM SEPARATION OF BUMP TO EDGE OF POLYIMIDE LAYER:

20 µm



PAD COORDINATES

#	Pad Name	X	Y	W	H
1	DUMMY	-6867.9	649.7	85	50
2	COM2	-6867.4	570.3	95	33
3	COM4	-6867.4	520.3	95	33
4	COM6	-6867.4	470.3	95	33
5	COM8	-6867.4	420.3	95	33
6	COM10	-6867.4	370.3	95	33
7	COM12	-6867.4	320.3	95	33
8	COM14	-6867.4	270.3	95	33
9	COM16	-6867.4	220.3	95	33
10	COM18	-6867.4	170.3	95	33
11	COM20	-6867.4	120.3	95	33
12	COM22	-6867.4	70.3	95	33
13	COM24	-6867.4	20.3	95	33
14	COM26	-6867.4	-29.8	95	33
15	COM28	-6867.4	-79.8	95	33
16	COM30	-6867.4	-129.8	95	33
17	COM32	-6867.4	-179.8	95	33
18	COM34	-6867.4	-229.8	95	33
19	COM36	-6867.4	-279.8	95	33
20	COM38	-6867.4	-329.8	95	33
21	COM40	-6867.4	-379.8	95	33
22	COM42	-6867.4	-429.8	95	33
23	COM44	-6867.4	-479.8	95	33
24	COM46	-6867.4	-529.8	95	33
25	COM48	-6867.4	-579.8	95	33
26	DUMMY	-6867.9	-654.4	85	50
27	COM50	-6479.6	-642.4	33	95
28	COM52	-6429.6	-642.4	33	95
29	COM54	-6379.6	-642.4	33	95
30	COM56	-6329.6	-642.4	33	95
31	COM58	-6279.6	-642.4	33	95
32	COM60	-6229.6	-642.4	33	95
33	COM62	-6179.6	-642.4	33	95
34	COM64	-6129.6	-642.4	33	95
35	COM66	-6079.6	-642.4	33	95
36	COM68	-6029.6	-642.4	33	95
37	COM70	-5979.6	-642.4	33	95
38	COM72	-5929.6	-642.4	33	95
39	COM74	-5879.6	-642.4	33	95
40	COM76	-5829.6	-642.4	33	95
41	COM78	-5779.6	-642.4	33	95
42	COM80	-5729.6	-642.4	33	95
43	D7	-5481.6	-645.4	50	80
44	VDDX	-5402.3	-645.4	50	80
45	D6	-5323.8	-645.4	50	80
46	D5	-5093.8	-645.4	50	80
47	D4	-4863.8	-645.4	50	80
48	D3	-4633.8	-645.4	50	80
49	D2	-4403.8	-645.4	50	80
50	D1	-4173.8	-645.4	50	80
51	D0	-3943.8	-645.4	50	80
52	VBIAS	-3706.0	-645.4	50	80
53	RST_	-3501.3	-645.4	50	80
54	CS1_	-3407.5	-645.4	50	80
55	VDDX	-3333.2	-645.4	50	80
56	CS0	-3256.9	-645.4	50	80
57	CD	-3173.6	-645.4	50	80
58	WR0	-3086.1	-645.4	50	80
59	VDDX	-3009.0	-645.4	50	80
60	WR1	-2930.4	-645.4	50	80

#	Pad Name	X	Y	W	H
61	BM0	-2840.0	-645.4	50	80
62	VDDX	-2760.8	-645.4	50	80
63	BM1	-2681.9	-645.4	50	80
64	TST4	-2593.9	-645.4	50	80
65	TST4	-2523.9	-645.4	50	80
66	TP5	-2195.0	-645.4	50	80
67	TST2	-2124.8	-645.4	50	80
68	TP4	-1800.8	-645.4	50	80
69	TP3	-1727.1	-645.4	50	80
70	TP2	-1657.1	-645.4	50	80
71	TP1	-1587.1	-645.4	50	80
72	ID	-1480.7	-645.4	50	80
73	VSS	-1391.6	-645.4	50	80
74	VSS	-1311.6	-645.4	50	80
75	VSS	-1231.6	-645.4	50	80
76	VSS	-1151.6	-645.4	50	80
77	VSS	-1071.6	-645.4	50	80
78	VSS	-991.5	-645.4	50	80
79	VSS2	-911.5	-645.4	50	80
80	VSS2	-831.5	-645.4	50	80
81	VSS2	-751.5	-645.4	50	80
82	VSS2	-671.5	-645.4	50	80
83	VSS2	-591.5	-645.4	50	80
84	VDD3	-511.5	-645.4	50	80
85	VDD3	-431.5	-645.4	50	80
86	VDD3	-351.5	-645.4	50	80
87	VDD3	-275.1	-645.4	50	80
88	VDD2	-97.5	-645.4	50	80
89	VDD2	-17.5	-645.4	50	80
90	VDD2	62.5	-645.4	50	80
91	VDD2	141.1	-645.4	50	80
92	VDD2	219.5	-645.4	50	80
93	VDD	493.0	-645.4	50	80
94	VDD	573.0	-645.4	50	80
95	VDD	653.0	-645.4	50	80
96	VDD	733.0	-645.4	50	80
97	VDD	813.0	-645.4	50	80
98	VDD	893.0	-645.4	50	80
99	VB0+	972.9	-645.4	50	80
100	VB0+	1042.9	-645.4	50	80
101	VB0+	1112.9	-645.4	50	80
102	VB0+	1182.9	-645.4	50	80
103	VB0+	1252.9	-645.4	50	80
104	VB0+	1475.7	-645.4	50	80
105	VB0+	1546.0	-645.4	50	80
106	VB0+	1616.0	-645.4	50	80
107	VB0+	1686.0	-645.4	50	80
108	SB0+	1756.0	-645.4	50	80
109	VB1+	1974.9	-645.4	50	80
110	VB1+	2044.9	-645.4	50	80
111	VB1+	2114.9	-645.4	50	80
112	VB1+	2184.9	-645.4	50	80
113	VB1+	2254.9	-645.4	50	80
114	VB1+	2477.7	-645.4	50	80
115	VB1+	2548.0	-645.4	50	80
116	VB1+	2618.0	-645.4	50	80
117	VB1+	2688.0	-645.4	50	80
118	SB1+	2758.0	-645.4	50	80
119	VB1-	2976.9	-645.4	50	80
120	VB1-	3046.9	-645.4	50	80

#	Pad Name	X	Y	W	H
121	VB1-	3116.9	-645.4	50	80
122	VB1-	3186.9	-645.4	50	80
123	VB1-	3256.9	-645.4	50	80
124	VB1-	3479.7	-645.4	50	80
125	VB1-	3550.0	-645.4	50	80
126	VB1-	3620.0	-645.4	50	80
127	VB1-	3690.0	-645.4	50	80
128	SB1-	3760.0	-645.4	50	80
129	VB0-	3978.9	-645.4	50	80
130	VB0-	4048.9	-645.4	50	80
131	VB0-	4118.9	-645.4	50	80
132	VB0-	4188.9	-645.4	50	80
133	VB0-	4258.9	-645.4	50	80
134	VB0-	4481.7	-645.4	50	80
135	VB0-	4552.0	-645.4	50	80
136	VB0-	4622.0	-645.4	50	80
137	VB0-	4692.0	-645.4	50	80
138	SB0-	4762.0	-645.4	50	80
139	VLCDIN	5118.4	-645.4	50	80
140	VLCDIN	5188.7	-645.4	50	80
141	VLCDOUT	5258.7	-645.4	50	80
142	VLCDOUT	5328.7	-645.4	50	80
143	COM79	5610.6	-642.4	33	95
144	COM77	5660.6	-642.4	33	95
145	COM75	5710.6	-642.4	33	95
146	COM73	5760.6	-642.4	33	95
147	COM71	5810.6	-642.4	33	95
148	COM69	5860.6	-642.4	33	95
149	COM67	5910.6	-642.4	33	95
150	COM65	5960.6	-642.4	33	95
151	COM63	6010.6	-642.4	33	95
152	COM61	6060.6	-642.4	33	95
153	COM59	6110.6	-642.4	33	95
154	COM57	6160.6	-642.4	33	95
155	COM55	6210.6	-642.4	33	95
156	COM53	6260.6	-642.4	33	95
157	COM51	6310.6	-642.4	33	95
158	COM49	6360.6	-642.4	33	95
159	DUMMY	6868.1	-658.7	85	50
160	COM47	6867.6	-594.9	95	33
161	COM45	6867.6	-544.9	95	33
162	COM43	6867.6	-494.9	95	33
163	COM41	6867.6	-444.9	95	33
164	COM39	6867.6	-394.9	95	33
165	COM37	6867.6	-344.9	95	33
166	COM35	6867.6	-294.9	95	33
167	COM33	6867.6	-244.9	95	33
168	COM31	6867.6	-194.9	95	33
169	COM29	6867.6	-144.9	95	33
170	COM27	6867.6	-94.9	95	33
171	COM25	6867.6	-44.9	95	33
172	COM23	6867.6	5.1	95	33
173	COM21	6867.6	55.1	95	33
174	COM19	6867.6	105.1	95	33
175	COM17	6867.6	155.1	95	33
176	COM15	6867.6	205.1	95	33
177	COM13	6867.6	255.1	95	33
178	COM11	6867.6	305.1	95	33
179	COM9	6867.6	355.1	95	33
180	COM7	6867.6	405.1	95	33
181	COM5	6867.6	455.1	95	33
182	COM3	6867.6	505.1	95	33
183	COM1	6867.6	555.1	95	33

#	Pad Name	X	Y	W	H
184	DUMMY	6868.1	649.7	85	50
185	SEG1	6538.0	628.6	24.5	123
186	SEG2	6496.5	628.6	24.5	123
187	SEG3	6455.0	628.6	24.5	123
188	SEG4	6413.5	628.6	24.5	123
189	SEG5	6372.0	628.6	24.5	123
190	SEG6	6330.5	628.6	24.5	123
191	SEG7	6289.0	628.6	24.5	123
192	SEG8	6247.5	628.6	24.5	123
193	SEG9	6206.0	628.6	24.5	123
194	SEG10	6164.5	628.6	24.5	123
195	SEG11	6123.0	628.6	24.5	123
196	SEG12	6081.5	628.6	24.5	123
197	SEG13	6040.0	628.6	24.5	123
198	SEG14	5998.5	628.6	24.5	123
199	SEG15	5957.0	628.6	24.5	123
200	SEG16	5915.5	628.6	24.5	123
201	SEG17	5874.0	628.6	24.5	123
202	SEG18	5832.5	628.6	24.5	123
203	SEG19	5791.0	628.6	24.5	123
204	SEG20	5749.5	628.6	24.5	123
205	SEG21	5708.0	628.6	24.5	123
206	SEG22	5666.5	628.6	24.5	123
207	SEG23	5625.0	628.6	24.5	123
208	SEG24	5583.5	628.6	24.5	123
209	SEG25	5542.0	628.6	24.5	123
210	SEG26	5500.5	628.6	24.5	123
211	SEG27	5459.0	628.6	24.5	123
212	SEG28	5417.5	628.6	24.5	123
213	SEG29	5376.0	628.6	24.5	123
214	SEG30	5334.5	628.6	24.5	123
215	SEG31	5293.0	628.6	24.5	123
216	SEG32	5251.5	628.6	24.5	123
217	SEG33	5210.0	628.6	24.5	123
218	SEG34	5168.5	628.6	24.5	123
219	SEG35	5127.0	628.6	24.5	123
220	SEG36	5085.5	628.6	24.5	123
221	SEG37	5044.0	628.6	24.5	123
222	SEG38	5002.5	628.6	24.5	123
223	SEG39	4961.0	628.6	24.5	123
224	SEG40	4919.5	628.6	24.5	123
225	SEG41	4878.0	628.6	24.5	123
226	SEG42	4836.5	628.6	24.5	123
227	SEG43	4795.0	628.6	24.5	123
228	SEG44	4753.5	628.6	24.5	123
229	SEG45	4712.0	628.6	24.5	123
230	SEG46	4670.5	628.6	24.5	123
231	SEG47	4629.0	628.6	24.5	123
232	SEG48	4587.5	628.6	24.5	123
233	SEG49	4546.0	628.6	24.5	123
234	SEG50	4504.5	628.6	24.5	123
235	SEG51	4463.0	628.6	24.5	123
236	SEG52	4421.5	628.6	24.5	123
237	SEG53	4380.0	628.6	24.5	123
238	SEG54	4338.5	628.6	24.5	123
239	SEG55	4297.0	628.6	24.5	123
240	SEG56	4255.5	628.6	24.5	123
241	SEG57	4214.0	628.6	24.5	123
242	SEG58	4172.5	628.6	24.5	123
243	SEG59	4131.0	628.6	24.5	123
244	SEG60	4089.5	628.6	24.5	123
245	SEG61	3962.3	628.6	24.5	123
246	SEG62	3920.8	628.6	24.5	123

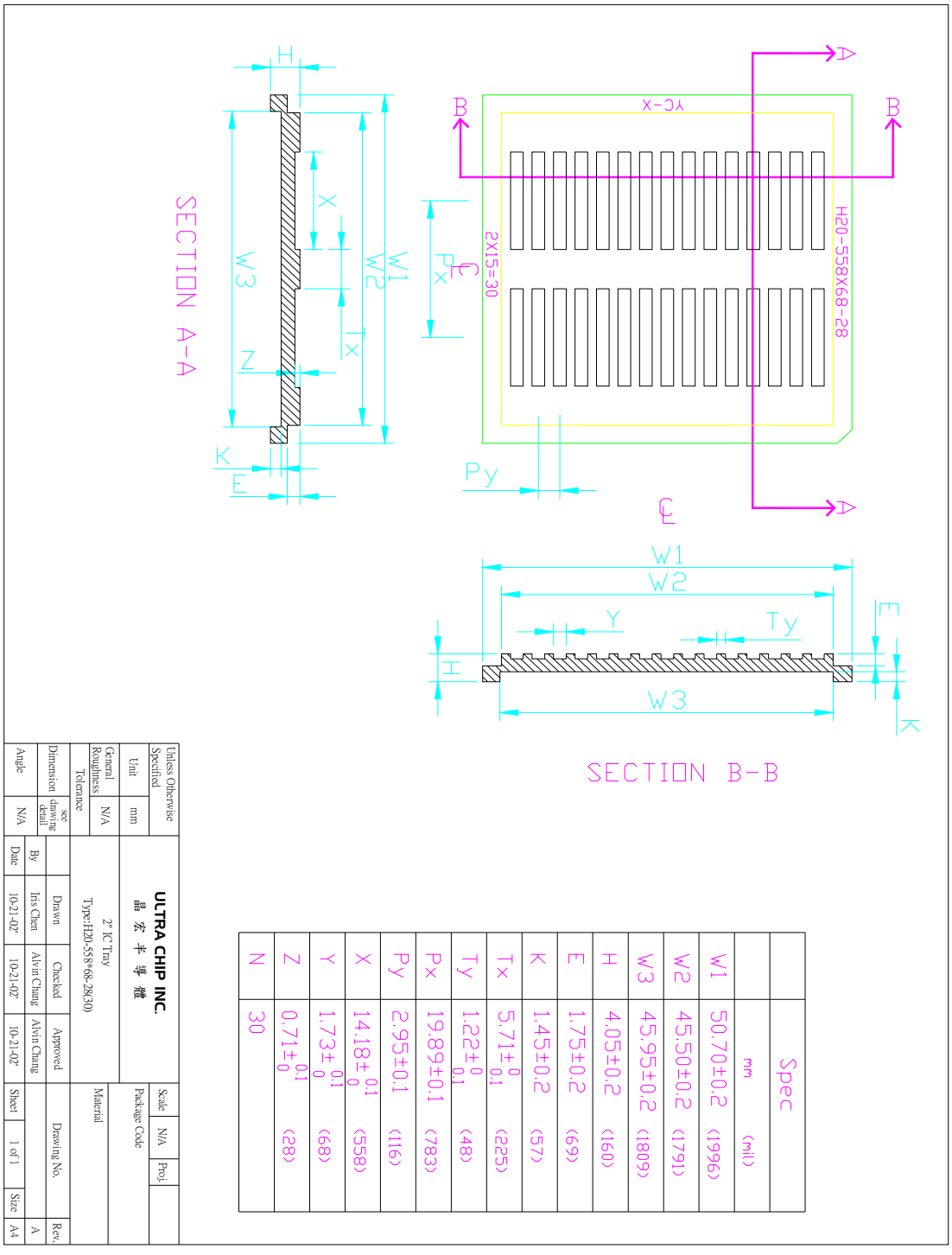
#	Pad Name	X	Y	W	H
247	SEG63	3879.3	628.6	24.5	123
248	SEG64	3837.8	628.6	24.5	123
249	SEG65	3796.3	628.6	24.5	123
250	SEG66	3754.8	628.6	24.5	123
251	SEG67	3713.3	628.6	24.5	123
252	SEG68	3671.8	628.6	24.5	123
253	SEG69	3630.3	628.6	24.5	123
254	SEG70	3588.8	628.6	24.5	123
255	SEG71	3547.3	628.6	24.5	123
256	SEG72	3505.8	628.6	24.5	123
257	SEG73	3464.3	628.6	24.5	123
258	SEG74	3422.8	628.6	24.5	123
259	SEG75	3381.3	628.6	24.5	123
260	SEG76	3339.8	628.6	24.5	123
261	SEG77	3298.3	628.6	24.5	123
262	SEG78	3256.8	628.6	24.5	123
263	SEG79	3215.3	628.6	24.5	123
264	SEG80	3173.8	628.6	24.5	123
265	SEG81	3132.3	628.6	24.5	123
266	SEG82	3090.8	628.6	24.5	123
267	SEG83	3049.3	628.6	24.5	123
268	SEG84	3007.8	628.6	24.5	123
269	SEG85	2966.3	628.6	24.5	123
270	SEG86	2924.8	628.6	24.5	123
271	SEG87	2883.3	628.6	24.5	123
272	SEG88	2841.8	628.6	24.5	123
273	SEG89	2800.3	628.6	24.5	123
274	SEG90	2758.8	628.6	24.5	123
275	SEG91	2717.3	628.6	24.5	123
276	SEG92	2675.8	628.6	24.5	123
277	SEG93	2634.3	628.6	24.5	123
278	SEG94	2592.8	628.6	24.5	123
279	SEG95	2551.3	628.6	24.5	123
280	SEG96	2509.8	628.6	24.5	123
281	SEG97	2468.3	628.6	24.5	123
282	SEG98	2426.8	628.6	24.5	123
283	SEG99	2385.3	628.6	24.5	123
284	SEG100	2343.8	628.6	24.5	123
285	SEG101	2302.3	628.6	24.5	123
286	SEG102	2260.8	628.6	24.5	123
287	SEG103	2219.3	628.6	24.5	123
288	SEG104	2177.8	628.6	24.5	123
289	SEG105	2136.3	628.6	24.5	123
290	SEG106	2094.8	628.6	24.5	123
291	SEG107	2053.3	628.6	24.5	123
292	SEG108	2011.8	628.6	24.5	123
293	SEG109	1970.3	628.6	24.5	123
294	SEG110	1928.8	628.6	24.5	123
295	SEG111	1887.3	628.6	24.5	123
296	SEG112	1845.8	628.6	24.5	123
297	SEG113	1804.3	628.6	24.5	123
298	SEG114	1762.8	628.6	24.5	123
299	SEG115	1721.3	628.6	24.5	123
300	SEG116	1679.8	628.6	24.5	123
301	SEG117	1638.3	628.6	24.5	123
302	SEG118	1596.8	628.6	24.5	123
303	SEG119	1555.3	628.6	24.5	123
304	SEG120	1513.8	628.6	24.5	123
305	SEG121	1472.3	628.6	24.5	123
306	SEG122	1430.8	628.6	24.5	123
307	SEG123	1389.3	628.6	24.5	123
308	SEG124	1347.8	628.6	24.5	123
309	SEG125	1306.3	628.6	24.5	123

#	Pad Name	X	Y	W	H
310	SEG126	1264.8	628.6	24.5	123
311	SEG127	1223.3	628.6	24.5	123
312	SEG128	1181.8	628.6	24.5	123
313	SEG129	1140.3	628.6	24.5	123
314	SEG130	1098.8	628.6	24.5	123
315	SEG131	1057.3	628.6	24.5	123
316	SEG132	1015.8	628.6	24.5	123
317	SEG133	974.3	628.6	24.5	123
318	SEG134	932.8	628.6	24.5	123
319	SEG135	891.3	628.6	24.5	123
320	SEG136	849.8	628.6	24.5	123
321	SEG137	808.3	628.6	24.5	123
322	SEG138	766.8	628.6	24.5	123
323	SEG139	725.3	628.6	24.5	123
324	SEG140	683.8	628.6	24.5	123
325	SEG141	642.3	628.6	24.5	123
326	SEG142	600.8	628.6	24.5	123
327	SEG143	559.3	628.6	24.5	123
328	SEG144	517.8	628.6	24.5	123
329	SEG145	476.3	628.6	24.5	123
330	SEG146	434.8	628.6	24.5	123
331	SEG147	393.3	628.6	24.5	123
332	SEG148	351.8	628.6	24.5	123
333	SEG149	310.3	628.6	24.5	123
334	SEG150	268.8	628.6	24.5	123
335	SEG151	227.3	628.6	24.5	123
336	SEG152	185.8	628.6	24.5	123
337	SEG153	144.3	628.6	24.5	123
338	SEG154	102.8	628.6	24.5	123
339	SEG155	61.3	628.6	24.5	123
340	SEG156	19.8	628.6	24.5	123
341	SEG157	-21.7	628.6	24.5	123
342	SEG158	-63.2	628.6	24.5	123
343	SEG159	-104.7	628.6	24.5	123
344	SEG160	-146.2	628.6	24.5	123
345	SEG161	-187.7	628.6	24.5	123
346	SEG162	-229.2	628.6	24.5	123
347	SEG163	-270.7	628.6	24.5	123
348	SEG164	-312.2	628.6	24.5	123
349	SEG165	-353.7	628.6	24.5	123
350	SEG166	-395.2	628.6	24.5	123
351	SEG167	-436.7	628.6	24.5	123
352	SEG168	-478.2	628.6	24.5	123
353	SEG169	-519.7	628.6	24.5	123
354	SEG170	-561.2	628.6	24.5	123
355	SEG171	-602.7	628.6	24.5	123
356	SEG172	-644.2	628.6	24.5	123
357	SEG173	-685.7	628.6	24.5	123
358	SEG174	-727.2	628.6	24.5	123
359	SEG175	-768.7	628.6	24.5	123
360	SEG176	-810.2	628.6	24.5	123
361	SEG177	-851.7	628.6	24.5	123
362	SEG178	-893.2	628.6	24.5	123
363	SEG179	-934.7	628.6	24.5	123
364	SEG180	-976.2	628.6	24.5	123
365	SEG181	-1017.7	628.6	24.5	123
366	SEG182	-1059.2	628.6	24.5	123
367	SEG183	-1100.7	628.6	24.5	123
368	SEG184	-1142.2	628.6	24.5	123
369	SEG185	-1183.7	628.6	24.5	123
370	SEG186	-1225.2	628.6	24.5	123
371	SEG187	-1266.7	628.6	24.5	123
372	SEG188	-1308.2	628.6	24.5	123

#	Pad Name	X	Y	W	H
373	SEG189	-1349.7	628.6	24.5	123
374	SEG190	-1391.2	628.6	24.5	123
375	SEG191	-1432.7	628.6	24.5	123
376	SEG192	-1474.2	628.6	24.5	123
377	SEG193	-1515.7	628.6	24.5	123
378	SEG194	-1557.2	628.6	24.5	123
379	SEG195	-1598.7	628.6	24.5	123
380	SEG196	-1640.2	628.6	24.5	123
381	SEG197	-1681.7	628.6	24.5	123
382	SEG198	-1723.2	628.6	24.5	123
383	SEG199	-1764.7	628.6	24.5	123
384	SEG200	-1806.2	628.6	24.5	123
385	SEG201	-1847.7	628.6	24.5	123
386	SEG202	-1889.2	628.6	24.5	123
387	SEG203	-1930.7	628.6	24.5	123
388	SEG204	-1972.2	628.6	24.5	123
389	SEG205	-2013.7	628.6	24.5	123
390	SEG206	-2055.2	628.6	24.5	123
391	SEG207	-2096.7	628.6	24.5	123
392	SEG208	-2138.2	628.6	24.5	123
393	SEG209	-2179.7	628.6	24.5	123
394	SEG210	-2221.2	628.6	24.5	123
395	SEG211	-2262.7	628.6	24.5	123
396	SEG212	-2304.2	628.6	24.5	123
397	SEG213	-2345.7	628.6	24.5	123
398	SEG214	-2387.2	628.6	24.5	123
399	SEG215	-2428.7	628.6	24.5	123
400	SEG216	-2470.2	628.6	24.5	123
401	SEG217	-2511.7	628.6	24.5	123
402	SEG218	-2553.2	628.6	24.5	123
403	SEG219	-2594.7	628.6	24.5	123
404	SEG220	-2636.2	628.6	24.5	123
405	SEG221	-2677.7	628.6	24.5	123
406	SEG222	-2719.2	628.6	24.5	123
407	SEG223	-2760.7	628.6	24.5	123
408	SEG224	-2802.2	628.6	24.5	123
409	SEG225	-2843.7	628.6	24.5	123
410	SEG226	-2885.2	628.6	24.5	123
411	SEG227	-2926.7	628.6	24.5	123
412	SEG228	-2968.2	628.6	24.5	123
413	SEG229	-3009.7	628.6	24.5	123
414	SEG230	-3051.2	628.6	24.5	123
415	SEG231	-3092.7	628.6	24.5	123
416	SEG232	-3134.2	628.6	24.5	123
417	SEG233	-3175.7	628.6	24.5	123
418	SEG234	-3217.2	628.6	24.5	123
419	SEG235	-3258.7	628.6	24.5	123
420	SEG236	-3300.2	628.6	24.5	123
421	SEG237	-3341.7	628.6	24.5	123
422	SEG238	-3383.2	628.6	24.5	123
423	SEG239	-3424.7	628.6	24.5	123
424	SEG240	-3466.2	628.6	24.5	123
425	SEG241	-3507.7	628.6	24.5	123
426	SEG242	-3549.2	628.6	24.5	123
427	SEG243	-3590.7	628.6	24.5	123
428	SEG244	-3632.2	628.6	24.5	123
429	SEG245	-3673.7	628.6	24.5	123
430	SEG246	-3715.2	628.6	24.5	123
431	SEG247	-3756.7	628.6	24.5	123
432	SEG248	-3798.2	628.6	24.5	123
433	SEG249	-3839.7	628.6	24.5	123
434	SEG250	-3881.2	628.6	24.5	123
435	SEG251	-3922.7	628.6	24.5	123

#	Pad Name	X	Y	W	H
436	SEG252	-3964.2	628.6	24.5	123
437	SEG253	-4005.7	628.6	24.5	123
438	SEG254	-4047.2	628.6	24.5	123
439	SEG255	-4088.7	628.6	24.5	123
440	SEG256	-4130.2	628.6	24.5	123
441	SEG257	-4171.7	628.6	24.5	123
442	SEG258	-4213.2	628.6	24.5	123
443	SEG259	-4254.7	628.6	24.5	123
444	SEG260	-4296.2	628.6	24.5	123
445	SEG261	-4337.7	628.6	24.5	123
446	SEG262	-4379.2	628.6	24.5	123
447	SEG263	-4420.7	628.6	24.5	123
448	SEG264	-4462.2	628.6	24.5	123
449	SEG265	-4503.7	628.6	24.5	123
450	SEG266	-4545.2	628.6	24.5	123
451	SEG267	-4586.7	628.6	24.5	123
452	SEG268	-4628.2	628.6	24.5	123
453	SEG269	-4669.7	628.6	24.5	123
454	SEG270	-4711.2	628.6	24.5	123
455	SEG271	-4752.7	628.6	24.5	123
456	SEG272	-4794.2	628.6	24.5	123
457	SEG273	-4835.7	628.6	24.5	123
458	SEG274	-4877.2	628.6	24.5	123
459	SEG275	-4918.7	628.6	24.5	123
460	SEG276	-4960.2	628.6	24.5	123
461	SEG277	-5001.7	628.6	24.5	123
462	SEG278	-5043.2	628.6	24.5	123
463	SEG279	-5084.7	628.6	24.5	123
464	SEG280	-5126.2	628.6	24.5	123
465	SEG281	-5167.7	628.6	24.5	123
466	SEG282	-5209.2	628.6	24.5	123
467	SEG283	-5250.7	628.6	24.5	123
468	SEG284	-5292.2	628.6	24.5	123
469	SEG285	-5333.7	628.6	24.5	123
470	SEG286	-5375.2	628.6	24.5	123
471	SEG287	-5416.7	628.6	24.5	123
472	SEG288	-5458.2	628.6	24.5	123
473	SEG289	-5499.7	628.6	24.5	123
474	SEG290	-5541.2	628.6	24.5	123
475	SEG291	-5582.7	628.6	24.5	123
476	SEG292	-5624.2	628.6	24.5	123
477	SEG293	-5665.7	628.6	24.5	123
478	SEG294	-5707.2	628.6	24.5	123
479	SEG295	-5748.7	628.6	24.5	123
480	SEG296	-5790.2	628.6	24.5	123
481	SEG297	-5831.7	628.6	24.5	123
482	SEG298	-5873.2	628.6	24.5	123
483	SEG299	-5914.7	628.6	24.5	123
484	SEG300	-5956.2	628.6	24.5	123
485	SEG301	-5997.7	628.6	24.5	123
486	SEG302	-6039.2	628.6	24.5	123
487	SEG303	-6080.7	628.6	24.5	123
488	SEG304	-6122.2	628.6	24.5	123
489	SEG305	-6163.7	628.6	24.5	123
490	SEG306	-6205.2	628.6	24.5	123
491	SEG307	-6246.7	628.6	24.5	123
492	SEG308	-6288.2	628.6	24.5	123
493	SEG309	-6329.7	628.6	24.5	123
494	SEG310	-6371.2	628.6	24.5	123
495	SEG311	-6412.7	628.6	24.5	123
496	SEG312	-6454.2	628.6	24.5	123

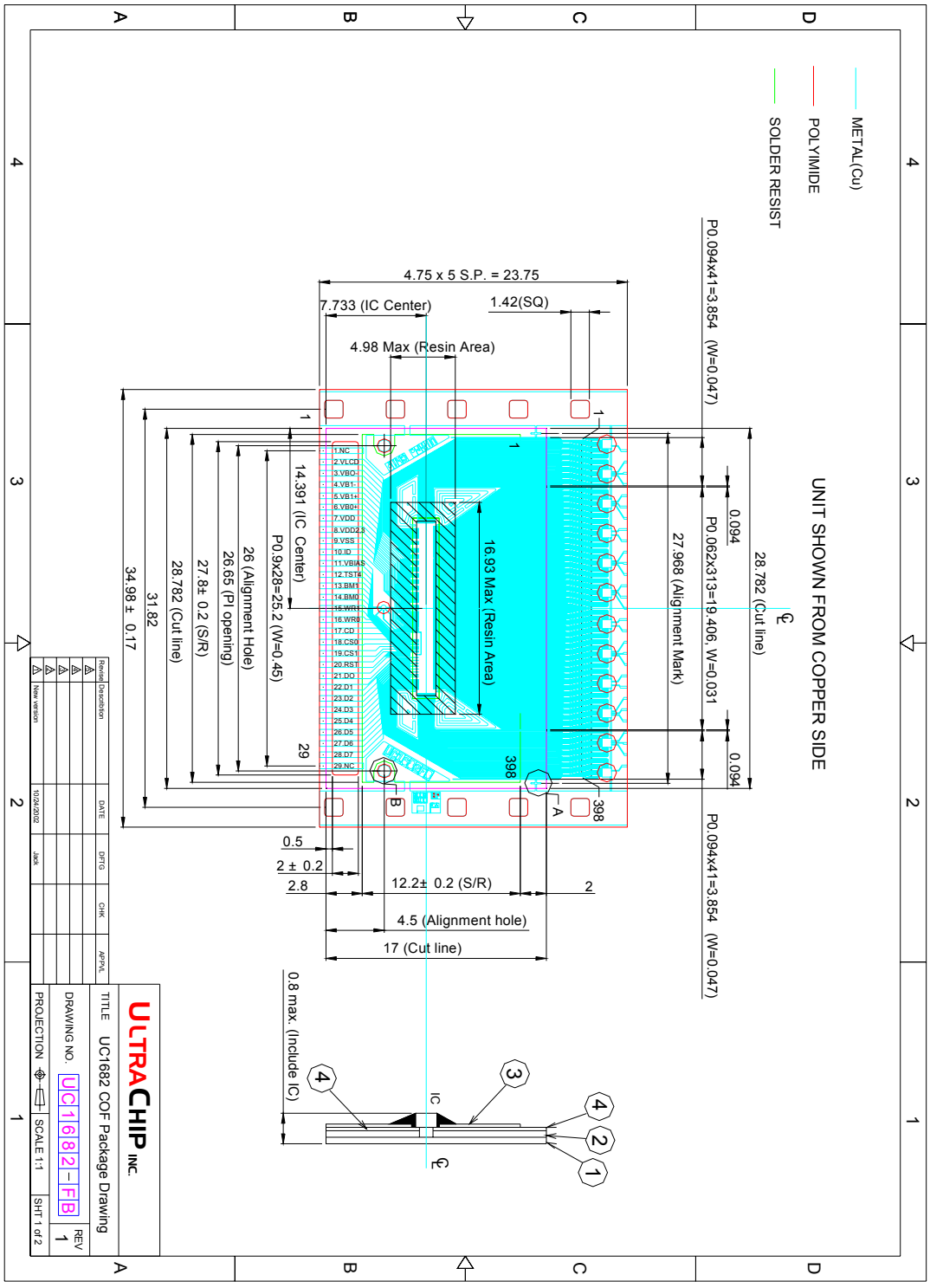
TRAY INFORMATION

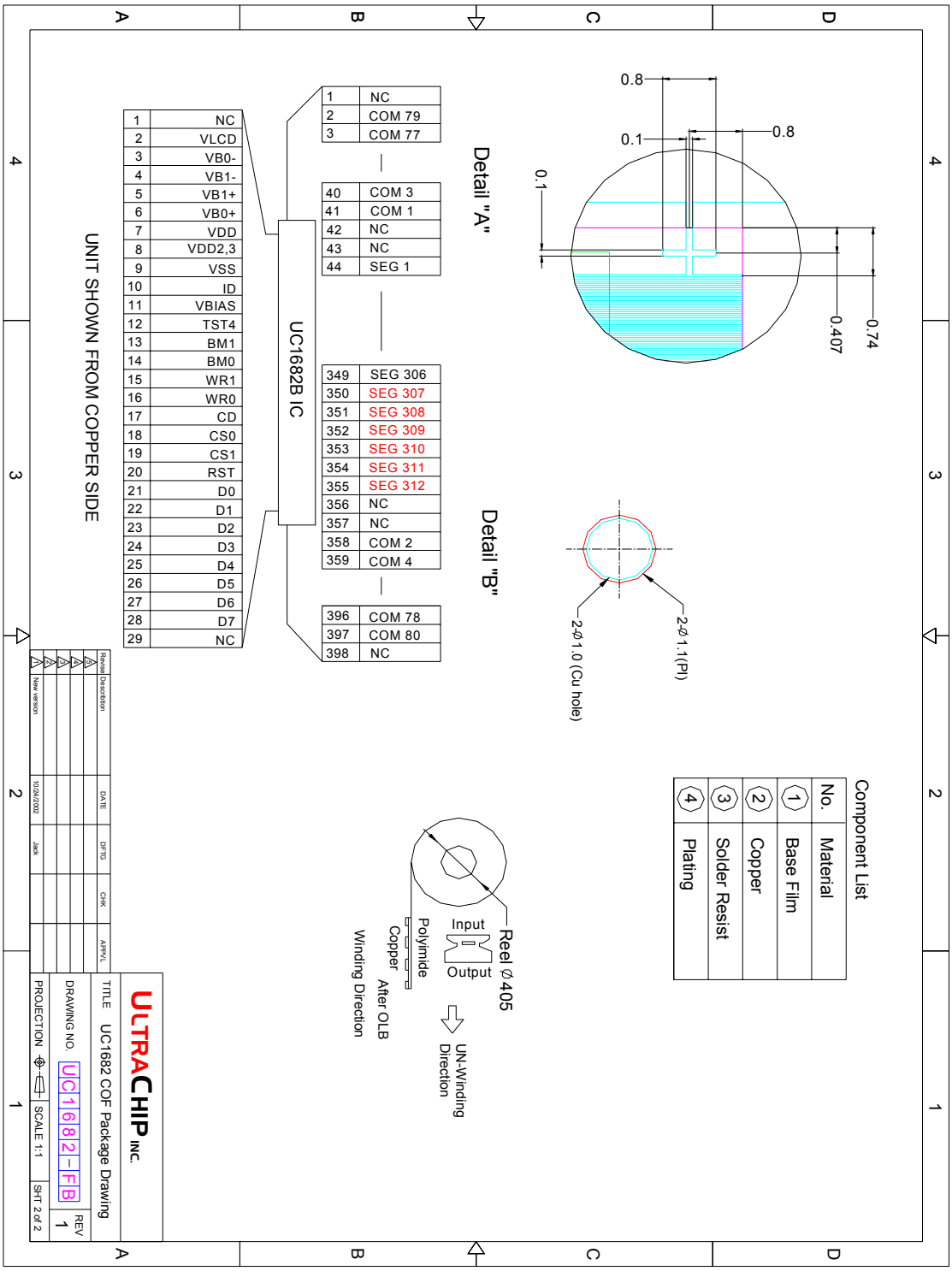


	Spec
	mm (mil)
W1	50.70±0.2 (1996)
W2	45.50±0.2 (1791)
W3	45.95±0.2 (1809)
H	4.05±0.2 (160)
E	1.75±0.2 (69)
K	1.45±0.2 (57)
Tx	5.71± 0 / 0.1 (225)
Ty	1.22± 0 / 0.1 (48)
Px	19.89±0.1 (783)
Py	2.95±0.1 (116)
X	14.18± 0.1 / 0 (558)
Y	1.73± 0.1 / 0 (68)
Z	0.71± 0.1 / 0 (28)
N	30

Unless Otherwise Specified		**ULTRA CHIP INC.** 晶宏半導體					
Unit	mm	2" IC Tray Type:H20-558*68-28(30)				Scale	N/A
General Roughness Tolerance	N/A					Proj.	
Dimension	see drawing detail					Material	
Angle	N/A					Drawing No.	
	By	Drawn	Checked	Approved	Date	Sheet	Size
	Iris Chen	Iris Chen	Alvin Chang	Alvin Chang	10-21-02'	1 of 1	A4
	10-21-02'	10-21-02'	10-21-02'	10-21-02'		Rev.	A

COF INFORMATION





1	NC
2	VLCD
3	VB0-
4	VB1-
5	VB1+
6	VB0+
7	VDD
8	VDD2,3
9	VSS
10	ID
11	VBIAS
12	TST4
13	BM1
14	BM0
15	WR1
16	WR0
17	CD
18	CS0
19	CS1
20	RST
21	D0
22	D1
23	D2
24	D3
25	D4
26	D5
27	D6
28	D7
29	NC

1	NC
2	COM 79
3	COM 77
40	COM 3
41	COM 1
42	NC
43	NC
44	SEG 1
349	SEG 306
350	SEG 307
351	SEG 308
352	SEG 309
353	SEG 310
354	SEG 311
355	SEG 312
356	NC
357	NC
358	COM 2
359	COM 4
396	COM 78
397	COM 80
398	NC

REVISION HISTORY

Version	Contents	Date of Rev.
0.0	Preliminary specification	Jul. 10, 2003
0.1	New release	Jul. 24, 2003
0.6	Figure 15 “Reference Power-Up Sequence” is updated for OTP. (Section “Reset & Power Management”, page 46; “Power Up” table, page 47.)	Aug. 11, 2003