EV1380
Product Brief
8A Synchronous Highly Integrated DC-DC DDR2/3/QDR™ Memory Termination Power SoC with Integrated Inductor

Description

The EV1380 is a Power System on a Chip (PowerSoC) DC to DC converter in a 68 pin QFN that is optimized for DDR2, DDR3, and QDR™ VTT applications. It requires a power supply (AVIN) for the controller and operates from an input supply (VDDQ) voltage range of 1.185V to 1.8V and provides a tightly regulated and very stable output voltage (VTT) which tracks VDDQ while sinking and sourcing up to 8A of output current. Enpirion's integrated inductor technology significantly helps to reduce noise, and offers a high efficiency solution for VTT applications with a very low external component count.

Advanced circuit techniques, optimized switching frequency, and very advanced, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion.

The complete power converter solution enhances productivity by offering greatly simplified board design, layout and manufacturing requirements.

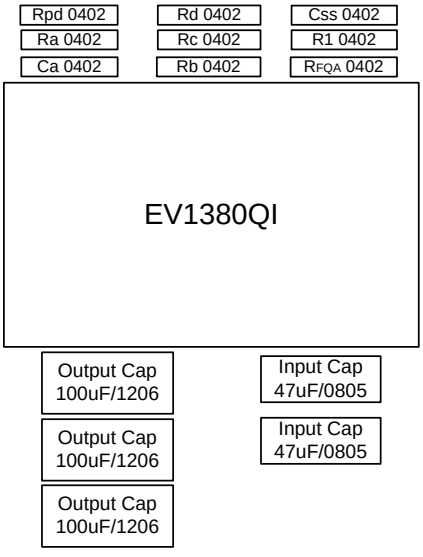

Figure 1: EV1380 Total Solution Size < 200mm² (not to scale)

Features

- High efficiency, up to 94%.
- Scaled version of VDDQ applied to VREF
- Output voltage tracks VDDQ +/- 1%
- Nominal 1.5MHz operating frequency with ability to synchronize to an external clock source or serve as the primary source.
- Optional externally programmable frequency between 1MHz and 1.5MHz for application tuning.
- Monotonic start-up with pre-bias.
- Programmable soft-start time. Soft Shutdown.
- Master/slave configuration for parallel operation.
- Thermal shutdown, over current, short circuit, and under-voltage protection.
- RoHS compliant, MSL level 3, 260C reflow.

Application

- Bus Termination: DDR2, DDR3, & QDR™ memory

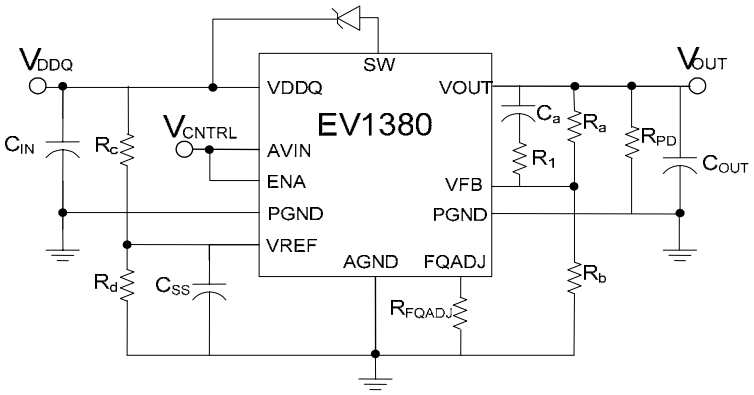

Figure 2: Typical Application Schematic (V_{DDQ} is the memory core voltage; V_{TT} is memory termination voltage that tracks V_{DDQ})

Pin Assignments (Top View)

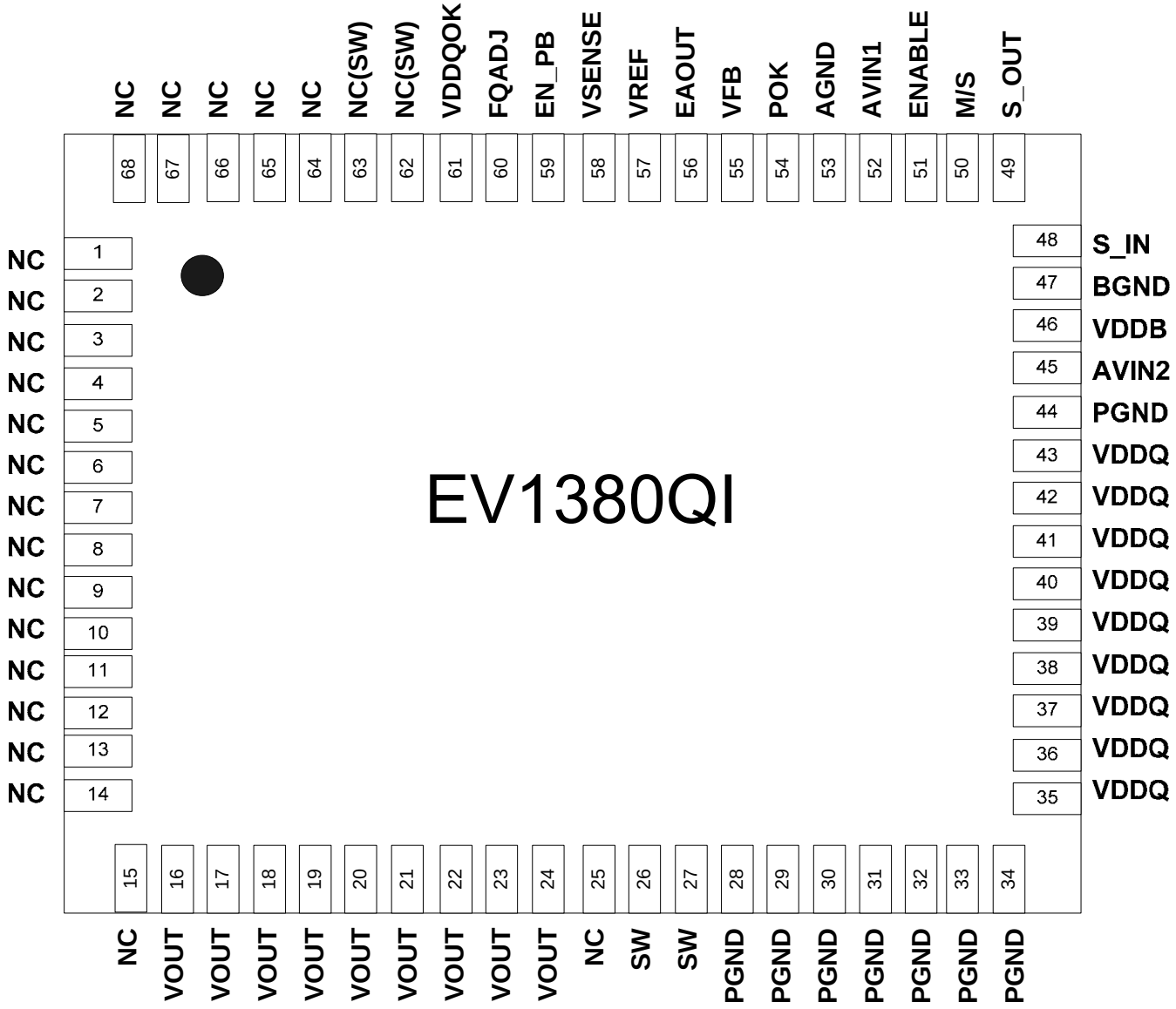

Figure 3: Pin Out Diagram (Top View)

NOTE: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

Pin Description

NAME	FUNCTION
PGND	Input and output power ground. Refer to layout section for specific layout requirements.
VOUT	Regulated converter output. Decouple with output filter capacitor to PGND. Refer to layout section for specific layout requirements
NC(SW)	No Connect – these pins are internally connected to the common switching node of the internal MOSFETs. They are not to be electrically connected to any external signal, ground, or voltage. Failure to follow these guidelines may result in damage to the device.
SW	These pins are internally connected to the common switching node of the internal MOSFETs. The anode of a schottky diode needs to be connected to these pins. The cathode of the diode needs to be connected to VDDQ.
VDDQ	In DDR applications the input to this pin is the DDR core voltage. This is the input power supply to the power train which will be divided by two to create an output voltage that tracks with the input voltage applied to this pin. Decouple with input capacitor to PGND. Refer to layout section for specific layout requirements
S_OUT	Digital Output. Depending on the M_S pin, either a clock signal synchronous with the internal switching frequency or the PWM signal is output on this pin.
S_IN	Digital Input. Depending on the M_S pin, this pin accepts either an input clock to phase lock the internal switching frequency or a PWM input from another Enpirion PoL device.
M_S	This is a Ternary Input put. Floating the pin disables parallel operation. A low level configures the device as Master and a High level configures the device as a slave.
ENABLE	This is the Device Enable pin. Floating this pin or a high level enables the device while a low level disables the device.
AVIN1, AVIN2	Analog input voltage for the controller circuits. Each of these pins needs to be separately connected to the 3.3V input supply. Decouple with a capacitor to AGND.
POK	POK is a logical AND of VDDQOK and the internally generated POK of the EV1380. POK is an open drain logic output that requires an external pull-up resistor. POK is logic high when VOUT is within -10% to +10% of VOUT nominal. This pin guarantees a logic low even when the EV1380 is completely un-powered. This pin can sink a maximum 4mA. The pull-up resistor may be connected to a power supply other than AVIN or VDDQ but the voltage should be <3.6Volts.
AGND	This is the quiet ground for the controller.
VFB	This is the Feedback input pin which is always active. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. (A feed-forward capacitor and a resistor are required across the upper resistor.) The output voltage regulates so as to make the VFB node voltage = 600mV.
EAOUT	Optional Error Amplifier Output. Allows for customization of the control loop dynamics.
VREF	External voltage reference input. A resistor divider connects from VDDQ to AGND. The mid-point of the resistor divider is connected to VREF. The resistor divider has to be chosen to make the voltage applied to this pin 600mV. An optional capacitor (for soft start) may be connected from VREF to AGND.
VSENSE	This pin senses the output voltage.
FQADJ	The free running frequency of the internal oscillator may be reduced by connecting a suitable value resistor from this pin to AGND.
EN_PB	Monotonic start-up with pre-bias is enabled by either pulling this pin high or letting it float. A logical low on this pin will disable pre-bias mode operation.
VDDQOK	This is an input pin to indicate the externally supplied VDDQ has settled sufficiently. This pin should be tied to the VDDQ regulator POK output, or let float if unused.

Package and Mechanical

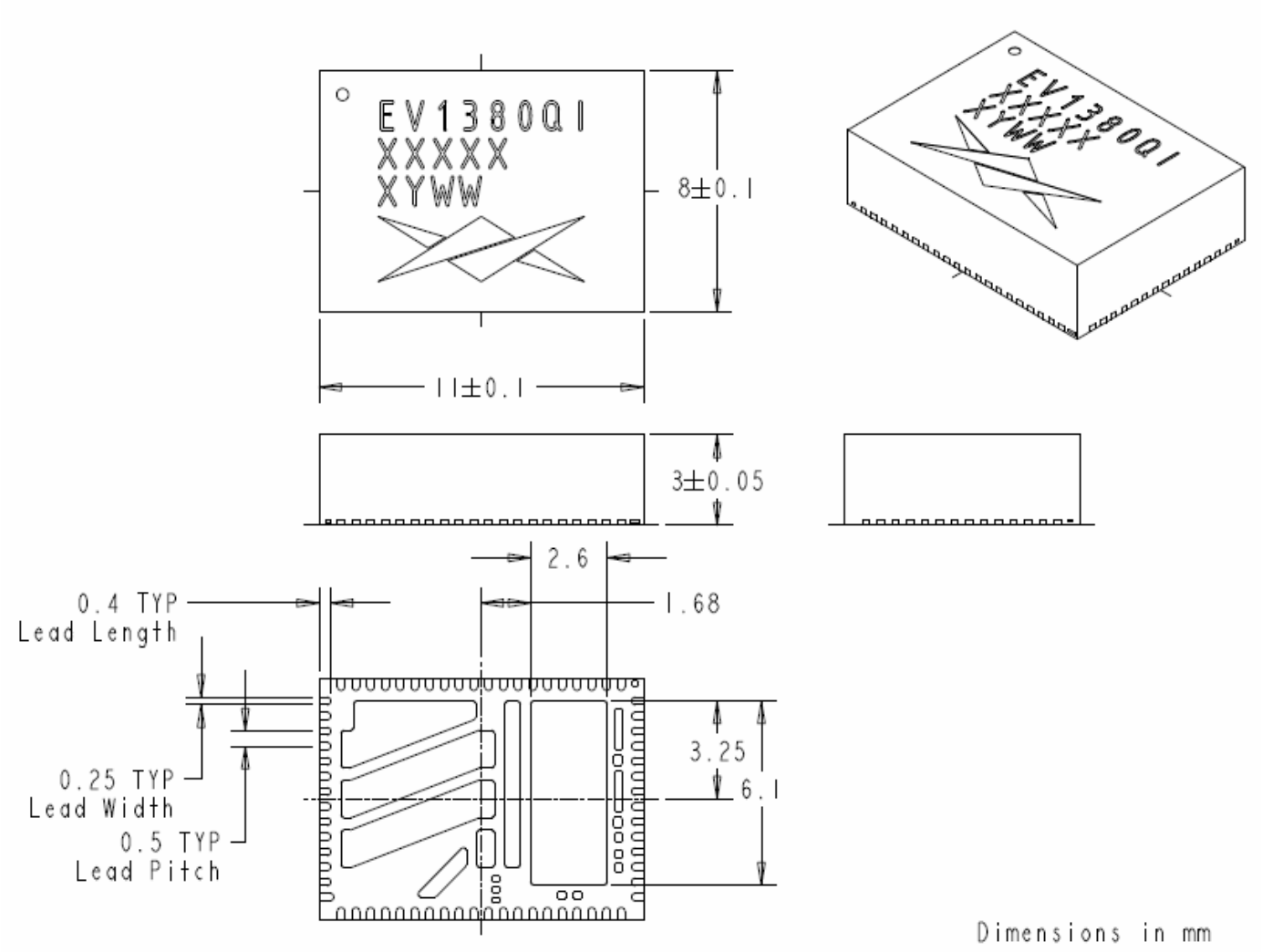

Figure 4: EV1380 Package Dimensions

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