HCTS164MS

Radiation Hardened 8-Bit Serial-In/Parallel-Out Shift Register

August 1995

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K RAD (Si)
- Dose Rate Survivability >10^{12} RAD (Si)/s (20ns Pulse)
- Dose Rate Upset >10^{10} RAD (Si)/s (20ns Pulse)
- Single Event Ray Upset Rate < 2 x 10^{-9} Errors/Bit Day (Typ)
- LET Threshold >100 MEV-cm^2/mg
- Latch-Up-Free Under Any Conditions
- Military Temperature Range: -55^{o}C to +125^{o}C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - -VIL = 0.8 VCC (Max)
  - -VIH = VCC/2 (Min)
- Input Current Levels Ii ≤5μA at VOL, VOH

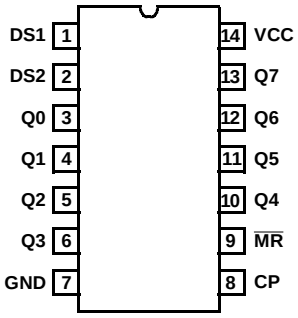
Description

The Intersil HCTS164MS is a radiation hardened 8-bit Serial-In/ Parallel-Out Shift Register with asynchronous reset.

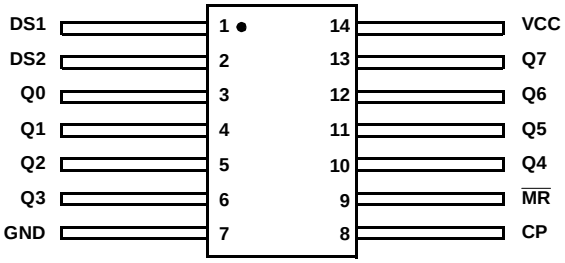
The HCTS164MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of the radiation hardened, high-speed, CMOS/SOS Logic Family.

Pinouts

14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835, CDIP2-T14
TOP VIEW



14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835, CDFP3-F14
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCTS164DMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	14 Lead SBDIP
HCTS164KMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	14 Lead Ceramic Flatpack
HCTS164D/Sample	+25^{o}C	Sample	14 Lead SBDIP
HCTS164K/Sample	+25^{o}C	Sample	14 Lead Ceramic Flatpack
HCTS164HMSR	+25^{o}C	Die	Die

Truth Table

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	DS1†	$\overline{DS2}$†	Q0	$\overline{Q1\text{-}Q7}$
Reset (Clear)	L	X	X	X	L	L-L
Shift	H	↗	L	L	L	q0 -q6
	H	↗	L	H	L	q0 - q6
	H	↗	H	L	L	q0 - q6
	H	↗	H	H	H	q0 - q6

H = High Voltage Level
L = Low Voltage Level
↗ = LOW-to-HIGH clock transition
q = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition
† = DS1 and DS2 inputs must be at state one setup prior to CP (rising edge)

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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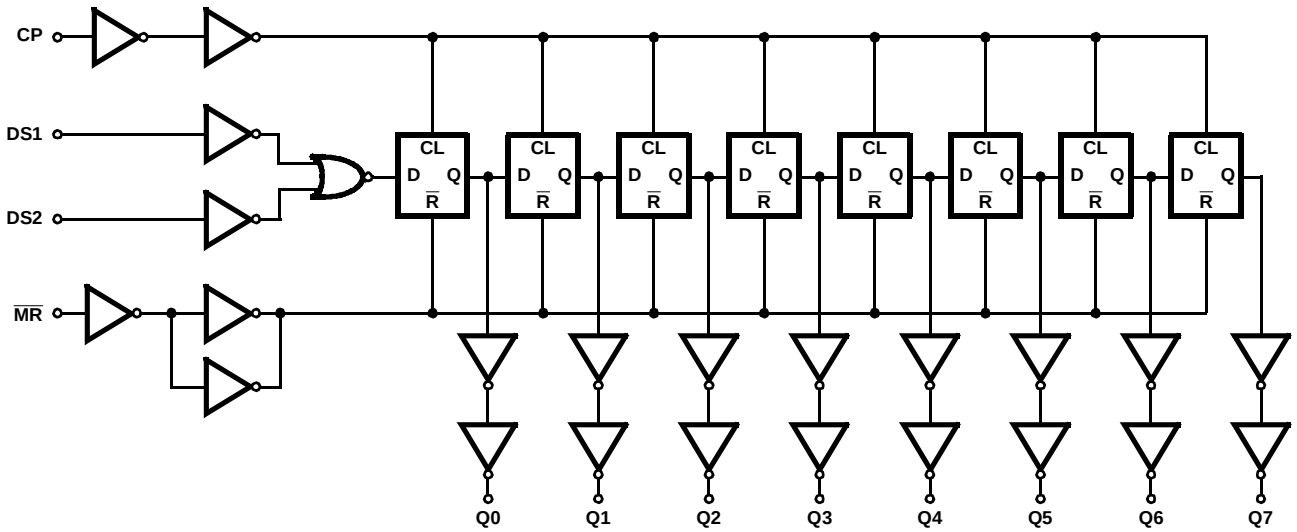
FN 3386.1
Spec Number 518613

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG). . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering 10s). . . . . $+265^oC$
Junction Temperature (TJ) . . . . . $+175^oC$
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package.	$74^oC/W$	$24^oC/W$
Ceramic Flatpack Package	$116^oC/W$	$30^oC/W$

Maximum Package Power Dissipation at $+125^o$ Ambient
SBDIP Package. 0.68W
Ceramic Flatpack Package 0.43W
If device power exceeds package dissipation capability provide heat sinking or derate linearly at the following rate:
SBDIP Package. . . . . $13.5mW/^oC$
Ceramic Flatpack Package . . . . . $8.6mW/^oC$

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5 VCC (TR, TF) . . . . . 100ns/V Max
Operating Temperature Range (T_A) . . . . . -55^oC to $+125^oC$
Input Low Voltage (VIL). . . . . 0V to 0.8V
Input High Voltage (VIH) . . . . . VCC to VCC/2V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	$+25^oC$	-	40	µA
			2, 3	$+125^oC$, -55^oC	-	750	µA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	$+25^oC$	4.8	-	mA
			2, 3	$+125^oC$, -55^oC	4.0	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V (Note 2)	1	$+25^oC$	-4.8	-	mA
			2, 3	$+125^oC$, -55^oC	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	$+25^oC$	-	±0.5	µA
			2, 3	$+125^oC$, -55^oC	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	$+25^oC$, $+125^oC$, -55^oC	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥4.0V is recognized as a logic "1", and VO ≤0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Qn	TPLH	VCC = 4.5V	9	+25°C	2	26	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	33	ns
CP to Qn	TPHL	VCC = 4.5V	9	+25°C	2	33	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	40	ns
$\overline{MR}$ to Qn	TPHL	VCC = 4.5V	9	+25°C	2	34	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	42	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3.0V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	-	135	pF
			1	+125°C, -55°C	-	210	pF
Input Capacitance	CIN	VCC = 5.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C, -55°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Minimum and Maximum Limits are guaranteed, but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP	200K RAD LIMITS MIN	200K RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V, IOL = 50µA	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V, IOH = -50µA	+25°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = VCC/2, VIL = 0.8V, (Note 3)	+25°C	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP	200K RAD LIMITS		UNITS
				MIN	MAX	
CP to Qn	TPLH	VCC = 4.5V	+25°C	2	33	ns
CP to Qn	TPHL	VCC = 4.5V	+25°C	2	40	ns
$\overline{MR}$ to Qn	TPHL	VCC = 4.5V	+25°C	2	42	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥4.0V is recognized as a logic “1”, and VO ≤0.5V is recognized as a logic “0”.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test 1 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test 2 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test 3 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTE:

1. Alternate Group A Testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN Test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ±0.5V	VCC = 6V ±0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3 - 6, 10 - 13	1, 2, 7 - 9	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3 - 6, 10 - 13	7	-	1, 2, 8, 9, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	3 - 6, 10 - 13	9, 14	8	1, 2

NOTES:

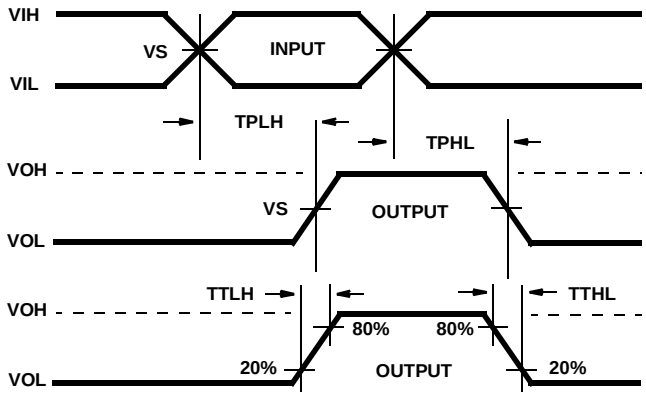
1. Each pin except VCC and GND will have a resistor of 10KΩ ±5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ±5% for dynamic burn-in.

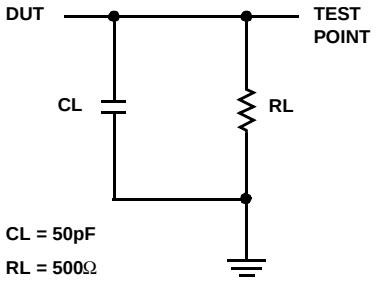
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ±0.5V
3 - 6, 10 - 13	7	1, 2, 8, 9, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ±5% for Irradiation Testing. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

AC Timing Diagrams and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.0	V
VS	1.3	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
95 mils x 95 mils
2.380mm x 2.410mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ±1kÅ

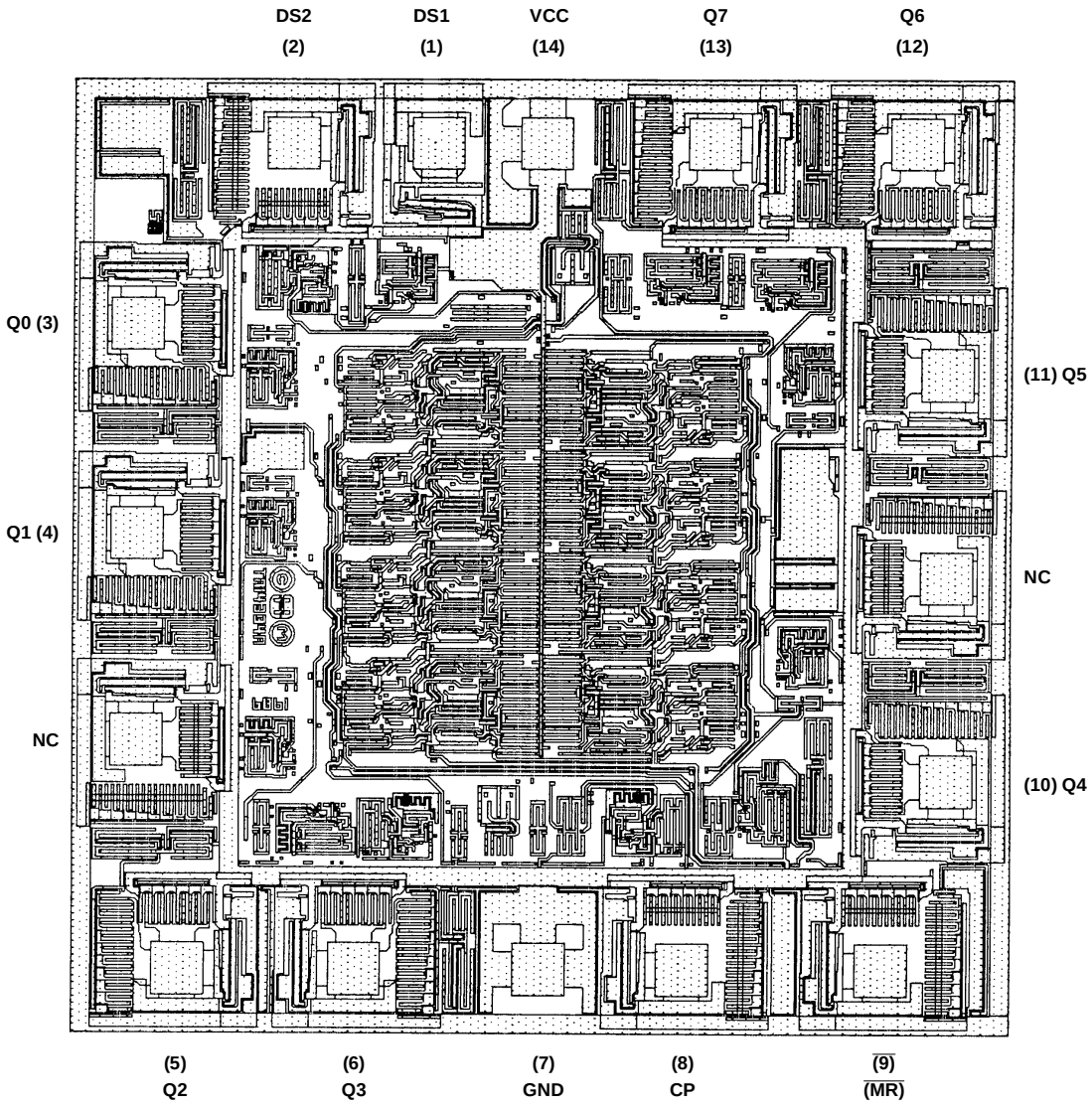
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ±2.6kÅ

WORST CASE CURRENT DENSITY:
< 2.0 x 10^5A/cm^2

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS164MS



Spec Number **518613**

Intersil Space Level Product Flow - MS

Wafer Lot Acceptance, All Lots (including SEM); Method 5007

Gamma Radiation Verification, Each Wafer, 4 Samples/ Wafer, 0 Rejects, Method 1019

100% Nondestructive Bond Pull, Method 2023

Sample Wire Bond Pull Monitor, Method 2011

Sample Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection - Method 2010, Condition A

100% Temperature Cycling, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Method 1015, Condition A or B, 24 Hours Minimum, +125^{o}C minimum

100% Interim Electrical Test (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Method 1015, Condition A or B, 24 Hours Minimum, + 125^{o}C Minimum

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (see Notes 1, 2)

100% Dynamic Burn-In, Condition D, 240 Hours, +125^{o}C or Equivalent per Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (see Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (see Note 3)

100% External Visual, Method 2009

Sample Group A, Method 5005 (see Note 4)

100% Data Package Generation (see Note 5)

NOTES:

1. Failures from Interim Electrical Test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroups 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A as allowed by MIL-STD-883, Method 5005 may be performed.
5. Data package contains:
   - Cover Sheet (Intersil name and/or logo, PO #, customer part #, lot date code, Intersil part #, lot #, quantity).
   - Wafer lot acceptance report (Method 5007). Includes reproductions of SEM photos with % step coverage. GAMMA Radiation Report. Contains cover page, disposition, rad dose, Lot #, test package used, specifications #s, test equipment, etc. radiation read and record data on file at Intersil.
   - X- Ray report and film. Includes pentrameter measurements.
   - Screening, electrical, and group A attributes (screening attributes begin after package seal).
   - Lot serial number sheet (good units serial # and lot #).
   - Variables data (all delta operations). Data is identified by serial number. The data header includes lot # and date of test.
   - The Certification of Conformance is part of the shipping invoice and is not part of the data book. The Certificate of Conformance is signed by an authorized quality representative.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

For information regarding Intersil Corporation and its products, see www.intersil.com

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