intersil

HCTS160MS

Radiation Hardened Synchronous Counter

September 1995

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm^2/mg
- Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10^{12} RAD (Si)/s
- Dose Rate Upset: >10^{10} RAD (Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - -Standard Outputs 10 LSTTL Loads
- Military Temperature Range: -55^{o}C to +125^{o}C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - -VIL = 0.8V Max
  - -VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5µA @ VOL, VOH

Description

The Intersil HCTS160MS is a Radiation Hardened high speed presettable BCD decade synchronous counter that features an asynchronous reset and look-ahead carry logic. Counting and parallel presetting are accomplished synchronously with the low-to-high transition of the clock. A low level on the synchronous parallel enable input, $\overline{SPE}$, disables counting and allows data at the preset inputs, P0 - P3, to be loaded into the counter. The counter is reset by a low on the master reset input, $\overline{MR}$. Two count enables, PE and TE are provided for n-bit cascading. TE also controls the terminal count output, TC. The terminal count output indicates a maximum count for one clock pulse and is used to enable the next cascaded stage to count.

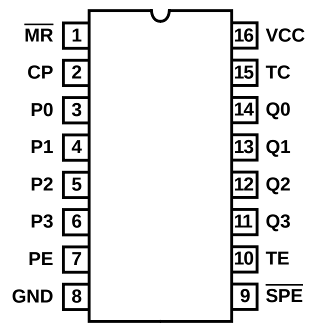
The HCTS160MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

The HCTS160MS is supplied in a 16 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Pinouts

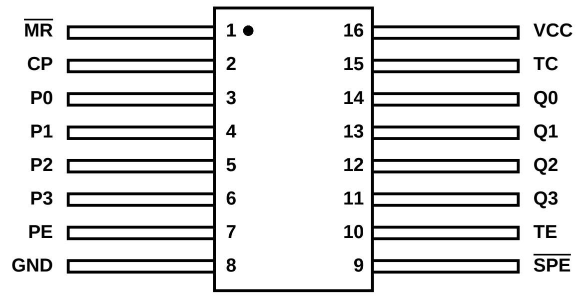
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835 CDIP2-T16

TOP VIEW



16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835 CDFP4-F16

TOP VIEW



Ordering Information

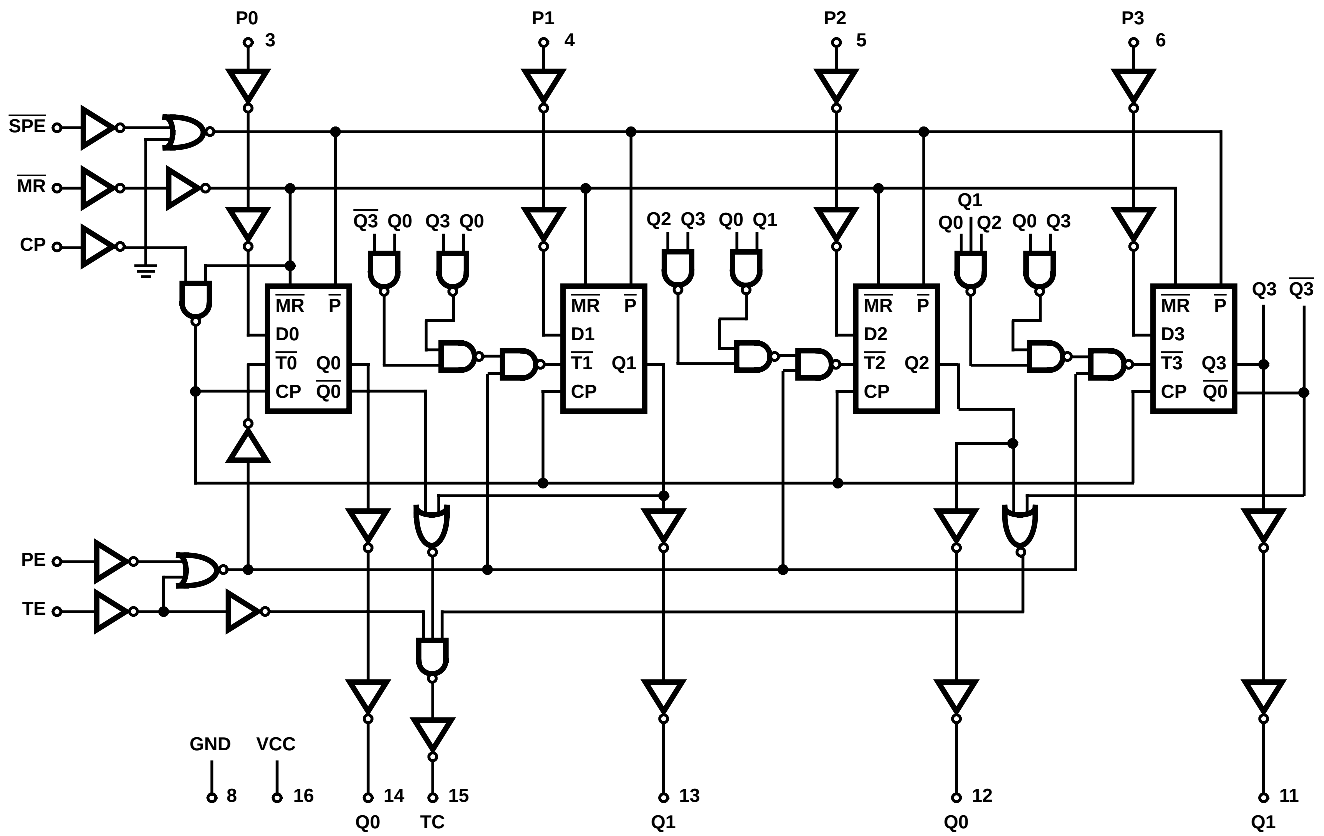
PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCTS160DMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	16 Lead SBDIP
HCTS160KMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	16 Lead Ceramic Flatpack
HCTS160D/Sample	+25^{o}C	Sample	16 Lead SBDIP
HCTS160K/Sample	+25^{o}C	Sample	16 Lead Ceramic Flatpack
HCTS160HMSR	+25^{o}C	Die	Die

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Spec Number 518611

File Number 2484.2

Functional Block Diagram



TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	Pn	Qn	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	_/¯	X	X	l	l	L	L
	H	_/¯	X	X	l	h	H	(Note 1)
Count	H	_/¯	h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	H	X	l (Note 2)	X	h (Note 3)	X	qn	(Note 1)
	H	X	X	l (Note 2)	h (Note 3)	X	qn	L

H = HIGH Voltage Level

L = LOW Voltage Level

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X = Immaterial

q = Lower case letterindicate the state of the referenced output prior to the LOW-to-HIGH clock transition

_/¯ = LOW-to-HIGH clock transition

NOTES:

1. The TC output is HIGH when TE is HIGH and the counter is at terminal count (HHHH for 161 and HLLH for 160)
2. The HIGH-to-LOW transition of PE or TE on the 54/74161 and 54/74160 should only occur while CP is high for conventional operation
3. The LOW-to-HIGH transition of $\overline{SPE}$ on the 54/74161 and 54/74160 should only occur while CP is high for conventional operation

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering 10sec) . . . . $+265^oC$
Junction Temperature (TJ) . . . . $+175^oC$
ESD Classification . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	$73^oC/W$	$24^oC/W$
Ceramic Flatpack Package	$114^oC/W$	$29^oC/W$

Maximum Package Power Dissipation at $+125^oC$ Ambient
SBDIP Package 0.68W
Ceramic Flatpack Package 0.44W

If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package . . . . $13.7mW/^oC$
Ceramic Flatpack Package . . . . $8.8mW/^oC$

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . 500ns Max
Operating Temperature Range (T_A) . . . . -55^oC to $+125^oC$
Input Low Voltage (VIL) . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	$+25^oC$	-	40	µA
			2, 3	$+125^oC$, -55^oC	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	$+25^oC$	4.8	-	mA
			2, 3	$+125^oC$, -55^oC	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	$+25^oC$	-4.8	-	mA
			2, 3	$+125^oC$, -55^oC	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	$+25^oC$	-	±0.5	µA
			2, 3	$+125^oC$, -55^oC	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	$+25^oC$, $+125^oC$, -55^oC	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to QN	TPHL	VCC = 4.5V	9	+25^{o}C	2	26	ns
			10, 11	+125^{o}C, -55^{o}C	2	30	ns
	TPLH	VCC = 4.5V	9	+25^{o}C	2	23	ns
			10, 11	+125^{o}C, -55^{o}C	2	26	ns
CP to TC	TPHL	VCC = 4.5V	9	+25^{o}C	2	28	ns
			10, 11	+125^{o}C, -55^{o}C	2	32	ns
	TPLH	VCC = 4.5V	9	+25^{o}C	2	24	ns
			10, 11	+125^{o}C, -55^{o}C	2	28	ns
TE to TC	TPHL	VCC = 4.5V	9	+25^{o}C	2	27	ns
			10, 11	+125^{o}C, -55^{o}C	2	29	ns
	TPLH	VCC = 4.5V	9	+25^{o}C	2	18	ns
			10, 11	+125^{o}C, -55^{o}C	2	20	ns
$\overline{MR}$ to QN, TC	TPHL	VCC = 4.5V	9	+25^{o}C	2	46	ns
			10, 11	+125^{o}C, -55^{o}C	2	51	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25^{o}C	-	104	pF
			1	+125^{o}C, -55^{o}C	-	260	pF
Input Capacitance	CIN	VCC = 5.0V,, f = 1MHz	1	+25^{o}C	-	10	pF
			1	+125^{o}C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25^{o}C	-	15	ns
			1	+125^{o}C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K LIMITS		UNITS
				MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25^{o}C	-	0.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25^{o}C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25^{o}C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V, IOL = 50µA	+25^{o}C	-	-0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V, IOH = -50µA	+25^{o}C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25^{o}C	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, (Note 3)	+25^{o}C	-	-	-
CP to QN	TPHL	VCC = 4.5V	+25^{o}C	2	30	ns
	TPLH	VCC = 4.5V	+25^{o}C	2	26	ns
CP to TC	TPHL	VCC = 4.5V	+25^{o}C	2	32	ns
	TPLH	VCC = 4.5V	+25^{o}C	2	28	ns
TE to TC	TPHL	VCC = 4.5V	+25^{o}C	2	29	ns
	TPLH	VCC = 4.5V	+25^{o}C	2	20	ns
$\overline{MR}$ to QN, TC	TPHL	VCC = 4.5V	+25^{o}C	2	51	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic “1”, and VO ≤ 0.5V is recognized as a logic “0”.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25^{o}C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/6005	1, 7, 9	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% go/no-go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC I BURN-IN					
11 - 15	1 - 10	-	16	-	-
STATIC II BURN-IN					
11 - 15	8	-	1 - 7, 9, 10, 16	-	-
DYNAMIC BURN-IN					
-	4, 6, 8	11 - 15	1, 3, 5, 7, 9, 10, 16	2	-

NOTES:

1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
11 - 15	8	1 - 7, 9, 10, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Intersil Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125^{o}C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125^{o}C min., Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Notes 1and 2)

100% Dynamic Burn-In, Condition D, 240 hrs., +125^{o}C or Equivalent, Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 3)

100% External Visual, Method 2009

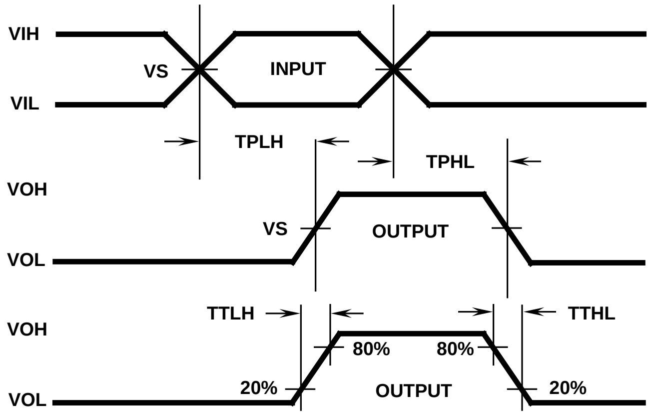
Sample - Group A, Method 5005 (Note 4)

100% Data Package Generation (Note 5)

NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

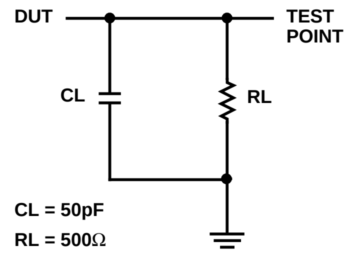
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

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Die Characteristics

DIE DIMENSIONS:
104 x 86 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

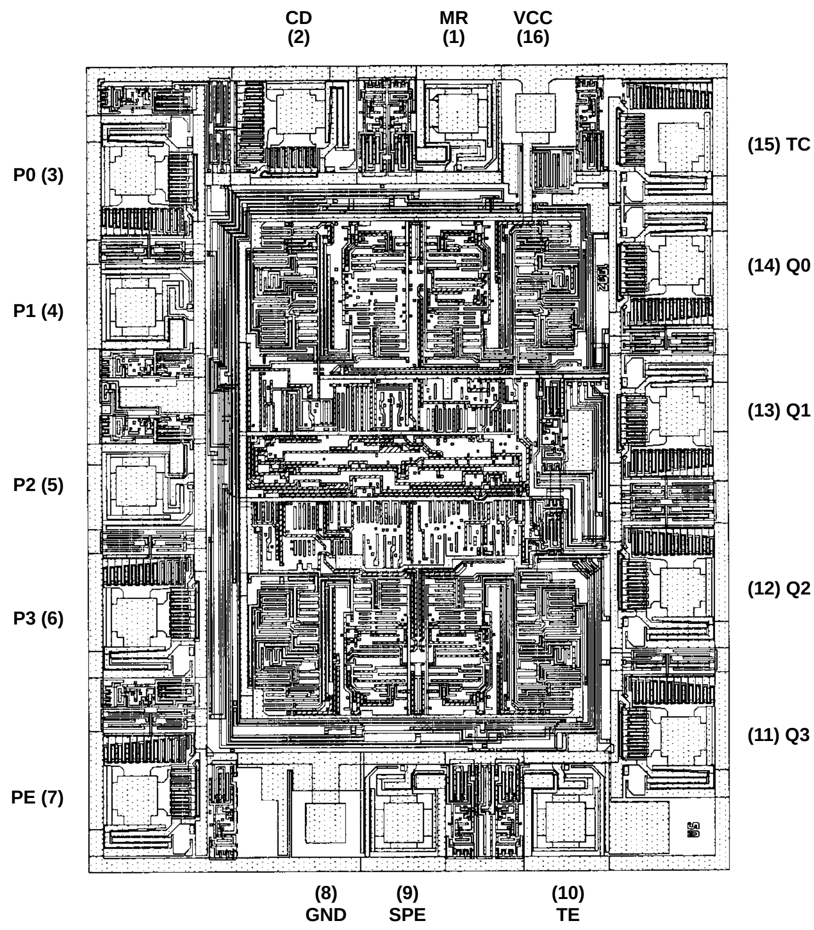
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS160MS



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS160 is TA14445A.