# R8A66120FFA

## 4M-bit x 2 MULTIPLE FIELD MEMORY

## Description

R8A66120FFA is high-speed field memory with two FIFO (First In First Out) memories of 4M-bit, which uses high-performance silicon gate process technology.
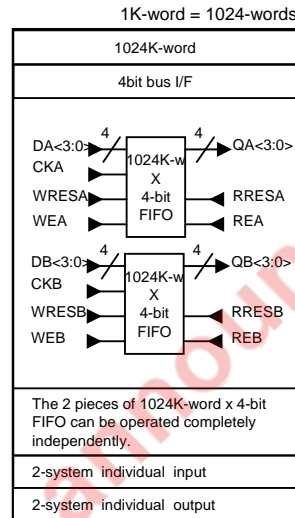
## Features

- Total memory Capacity — 8Mega-bit
- High speed operation
  - cycle time — 10.0ns(Min.)   fmax = 100MHz
  - output access time — 6.0ns(Max.)
- Output hold time — 1.0ns(Min.)
- Supply voltage — 3.3 ± 0.3V
- Variable length delay bit
- Synchronous write/read operation
- 3 states output
- Package — PLQP0048KB-A (48P6Q-A)
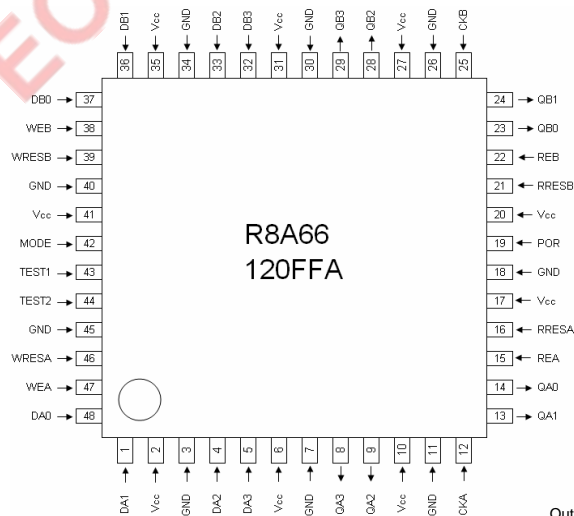  ( 48pins 7x7mm body LQFP )

## Application

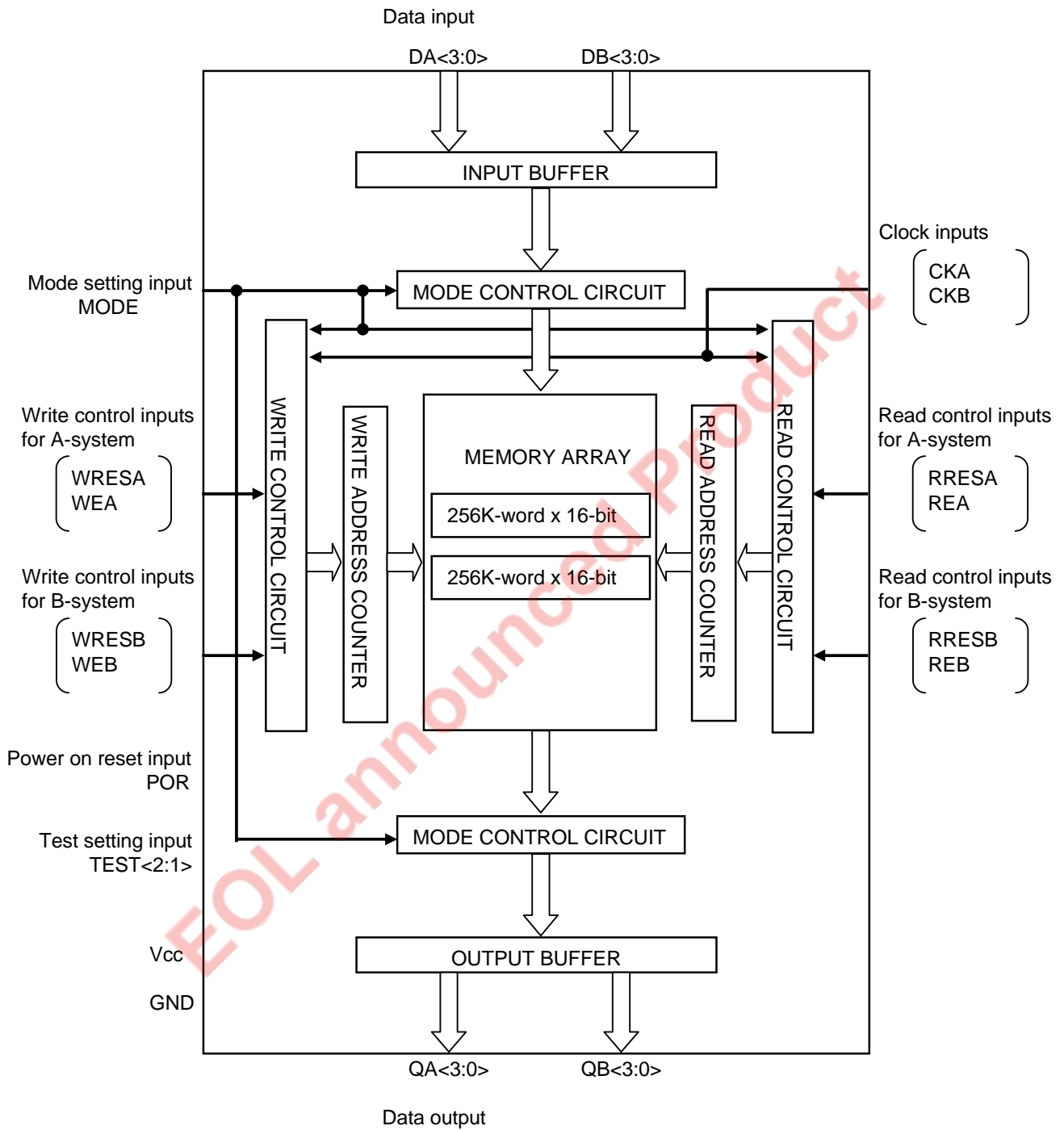W-CDMA base station, Digital PPC, Digital TV,VTR and so on.

## Mode Descriptions



1K-word = 1024-words

1024K-word

4bit bus I/F

DA<3:0>, CKA, WRESA, WEA → 1024K-w X 4-bit FIFO → QA<3:0>, RRESA, REA

DB<3:0>, CKB, WRESB, WEB → 1024K-w X 4-bit FIFO → QB<3:0>, RRESB, REB

The 2 pieces of 1024K-word x 4-bit FIFO can be operated completely independently.

2-system individual input

2-system individual output

## Pin Configuration (Top view)



Top pins (left to right): 36 DB1, 35 Vcc, 34 GND, 33 DB2, 32 DB3, 31 Vcc, 30 GND, 29 QB3, 28 QB2, 27 Vcc, 26 GND, 25 CKB

Left pins (top to bottom): DB0 37, WEB 38, WRESB 39, GND 40, Vcc 41, MODE 42, TEST1 43, TEST2 44, GND 45, WRESA 46, WEA 47, DA0 48

Right pins (top to bottom): 24 QB1, 23 QB0, 22 REB, 21 RRESB, 20 Vcc, 19 POR, 18 GND, 17 Vcc, 16 RRESA, 15 REA, 14 QA0, 13 QA1

Bottom pins (left to right): 1 DA1, 2 Vcc, 3 GND, 4 DA2, 5 DA3, 6 Vcc, 7 GND, 8 QA3, 9 QA2, 10 Vcc, 11 GND, 12 CKA

R8A66 120FFA

Outline: PLQP0048KB-A (48P6Q-A)

## Block Diagram

Data input

DA<3:0>    DB<3:0>

INPUT BUFFER

Clock inputs
CKA
CKB

Mode setting input
MODE

MODE CONTROL CIRCUIT

Write control inputs
for A-system
WRESA
WEA

WRITE CONTROL CIRCUIT

WRITE ADDRESS COUNTER

MEMORY ARRAY

256K-word x 16-bit

256K-word x 16-bit

READ ADDRESS COUNTER

READ CONTROL CIRCUIT

Read control inputs
for A-system
RRESA
REA

Write control inputs
for B-system
WRESB
WEB

Read control inputs
for B-system
RRESB
REB

Power on reset input
POR

Test setting input
TEST<2:1>

MODE CONTROL CIRCUIT

Vcc

GND

OUTPUT BUFFER

QA<3:0>    QB<3:0>

Data output

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## Pin Function Description

| Pin name (*1) | Name | Input/ Output | Number of pin(s) | Function |
|---|---|---|---|---|
| CKx | Clock input | Input | 2 | They are clock inputs. |
| WEx | Write enable input | Input | 2 | They are write enable control inputs. When they are "L", a write enable status is provided. |
| WRESx | Write reset input | Input | 2 | They are reset inputs to initialize a write address counter of internal FIFO. When they are "L", a write reset status is provided. |
| REx | Read enable input | Input | 2 | They are read enable control inputs. When they are "L", a read enable status is provided. |
| RRESx | Read reset input | Input | 2 | They are reset inputs to initialize a read address counter of internal FIFO. When they are "L", a read reset status is provided. |
| Dx<3:0> | Data input | Input | 8 | They are data input bus. |
| Qx<3:0> | Data output | Output | 8 | They are data output bus. |
| MODE | Mode setting input | Input | 1 | This is a pin for setting operation mode. MODE should be fixed at "L". |
| TEST<2:1> | Test setting input | Input | 2 | They are pins for test. TEST<2:1> should be fixed at "L". |
| POR | Power on reset input | Input | 1 | This is a power on reset input. |
| Vcc | Power supply pin | - | 9 | They are 3.3 V power supply pins. |
| GND | Ground pin | - | 9 | They are ground pins. |

*Note1: X of the pin name shows A or B. A = A-system, B = B-system.

## Mode pin Setting

In normal operation mode. It should be fixed on "L".

| Pin Name | Operation MODE |
|---|---|
| MODE | |
| L | Normal operation |
| H | Out of a guarantee |

## Operation Description
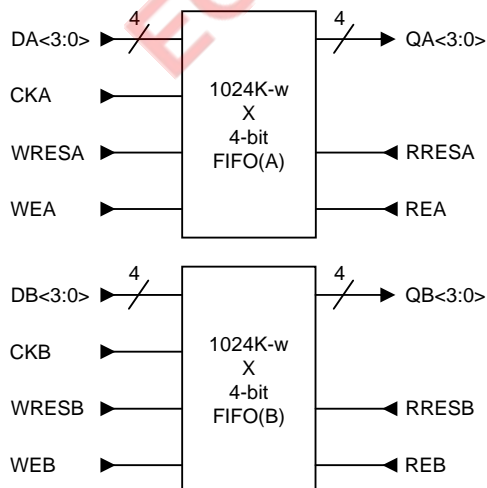


R8A66120FFA can be controlled two pieces of 1024K-word x 4-bit FIFO completely independently. Taking FIFO (A) as an example, the operation of FIFO memory is described as follows. The operation of FIFO (B) is the same as that of FIFO (A).

When write enable input WEA is "L", the contents of data input DA<3:0> are written into FIFO (A) in synchronization with the rising of clock input CKA.
At this time, the write address counter of FIFO (A) is incremented.
When WEA is "H", this IC disable to write data into FIFO (A) and the write address counter of FIFO (A) is not incremented.
When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.

When read enable input REA is "L", the contents of FIFO (A) are outputted to data output QA<3:0> in synchronization with the rising of clock input CKA.
At this time, the read address counter of FIFO (A) is incremented.
When REA is "H", this IC disable to read data from FIFO (A) and the read address counter of FIFO (A) is not incremented.
Also QA<3:0> become high impedance state.
When read reset input RRESA is "L", the read address counter of FIFO (A) is initialized.

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## Electrical Characteristics

### Absolute Maximum Ratings (Ta = 0 ~ 70ºC, unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Vcc | Supply voltage | | -0.3 ~ +3.8 | V |
| VI | Input voltage | A value based on GND | -0.3 ~ Vcc+0.3 | V |
| VO | Output voltage | | -0.3 ~ Vcc+0.3 | V |
| Pd | Maximum power dissipation | Ta = 70°C | 550 | mW |
| Tstg | Storage temperature | | -55 ~ +150 | °C |

### Recommended Operating Conditions

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Vcc | Supply voltage | | 3.0 | 3.3 | 3.6 | V |
| VI | Input voltage | A value based on GND | 0 | | Vcc | V |
| VO | Output voltage | | 0 | | Vcc | V |
| Topr | Operating ambient temperature | | 0 | | 70 | °C |

### DC Characteristics (Ta = 0 ~ 70ºC, Vcc = 3.3 ±0.3V, GND = 0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| VIH | "H" input voltage | A value based on GND | 0.8×Vcc | | | V |
| VIL | "L" input voltage | | | | 0.2 x Vcc | V |
| VOH | "H" output voltage | IOH = -4mA | Vcc−0.4 | | | V |
| VOL | "L" output voltage | IOL = 4mA | | | 0.4 | V |
| IIH | "H" input current | VI = Vcc | | | 10 | uA |
| IIL | "L" input current | VI = GND | | | -10 | uA |
| IOZH | Off state "H" output current | VO = Vcc | | | 10 | uA |
| IOZL | Off state "L" output current | VO = GND | | | -10 | uA |
| Icc | Operating mean current dissipation | Vcc = 3.3 ± 0.3 V  VI : Repeat "H" and "L"  VO : Output open  tCK = 10.0ns (f = 100MHz) | | | 150 | mA |
| CI | Input capacitance | f = 1MHz | | | 10 | pF |
| CO | Off state output capacitance | f = 1MHz | | | 15 | pF |

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### Power On

After power-on this IC, some circuits of internal FIFO should be initialized by the following procedures (1), (2).
Also, when the supply voltage (Vcc) drops below the operation voltage range(3.0 to 3.6V) during operating and so this is powered on again, they should be initialized by the same procedures.

(1)After 1msec or more has passed under the following conditions (i), (ii) and (iii), please input the signal of "L" to "H" to POR pin for power on reset.  After of that, POR pin should be fixed at "H".

                (i)   :Vcc reaches to the operation voltage range.

                (ii)  :The clock signal is inputted to CK pin

                (iii) :POR pin is fixed at "L".

(2)After POR pin is fixed at "H", write reset and read reset operations should be provided with 100 cycles or more respectively.
There is no problem in these reset operations, if total reset cycles reach to 100 or more even if those are discontinuous.

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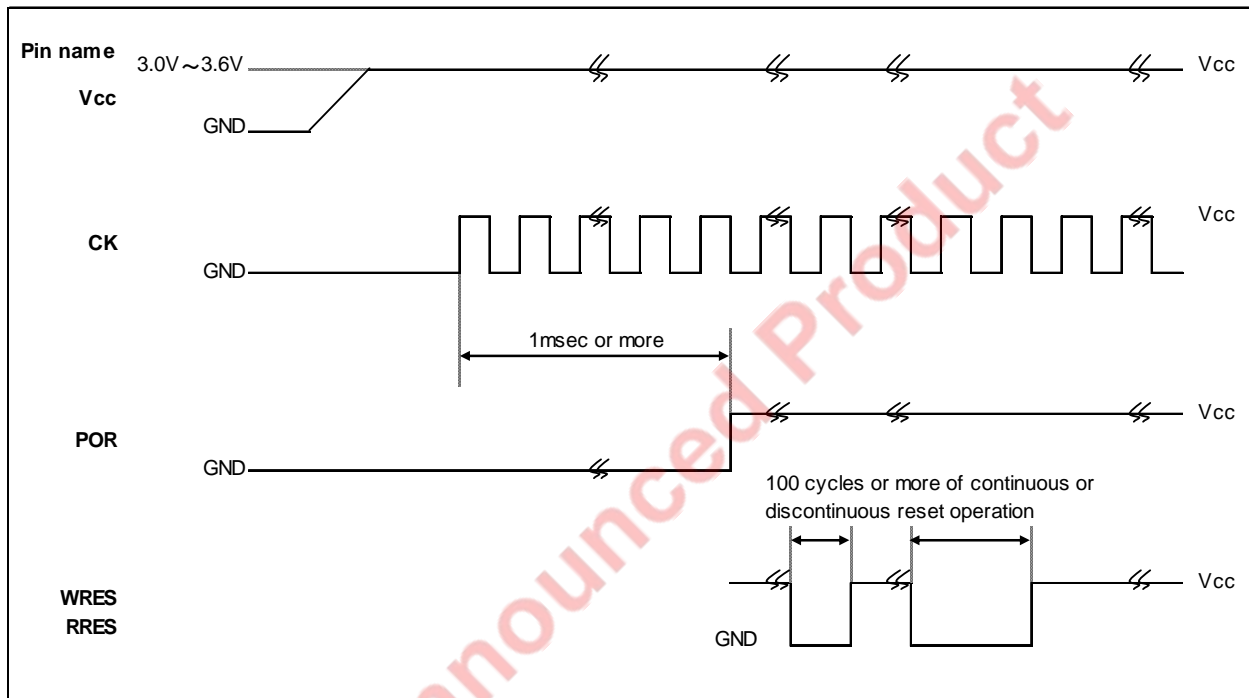
**Timing Requirements (Ta = 0 ~ 70°C,Vcc = 3.3 ± 0.3V, GND = 0V, unless otherwise noted)**

| Symbol | Parameter | Limits | | | Unit |
|--------|-----------|--------|--------|--------|------|
| | | Min. | Typ. | Max. | |
| tCK | Clock (CK) cycle | 10 | | 200 | ns |
| tCKH | CK "H" pulse width | 4 | | | |
| tCKL | CK "L" pulse width | 4 | | | |
| tDS | Input data setup time to CK | 4 | | | |
| tDH | Input data hold time to CK | 0 | | | |
| tWRESS | Write reset setup time to CK | 4 | | | |
| tWRESH | Write reset hold time to CK | 0 | | | |
| tRRESS | Read reset setup time to CK | 4 | | | |
| tRRESH | Read reset hold time to CK | 0 | | | |
| tWES | Write enable setup time to CK | 4 | | | |
| tWEH | Write enable hold time to CK | 0 | | | |
| tRES | Read enable setup time to CK | 4 | | | |
| tREH | Read enable hold time to CK | 0 | | | |
| tr, tf | Input pulse rise / fall time | | | 3 | |

**Switching Characteristics (Ta = 0 ~ 70°C, Vcc = 3.3 ± 0.3V, GND = 0V, unless otherwise noted)**

| Symbol | Parameter | Limits | | | Unit |
|--------|-----------|--------|--------|--------|------|
| | | Min. | Typ. | Max. | |
| tAC | Output access time to CK | | | 6 | ns |
| tOH | Output hold time to CK | 1 | | | |
| tOEN | Output enable time to CK | 1 | | 6 | |
| tODIS | Output disable time to CK | 1 | | 6 | |

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**Switching Characteristics Measurement Circuit**
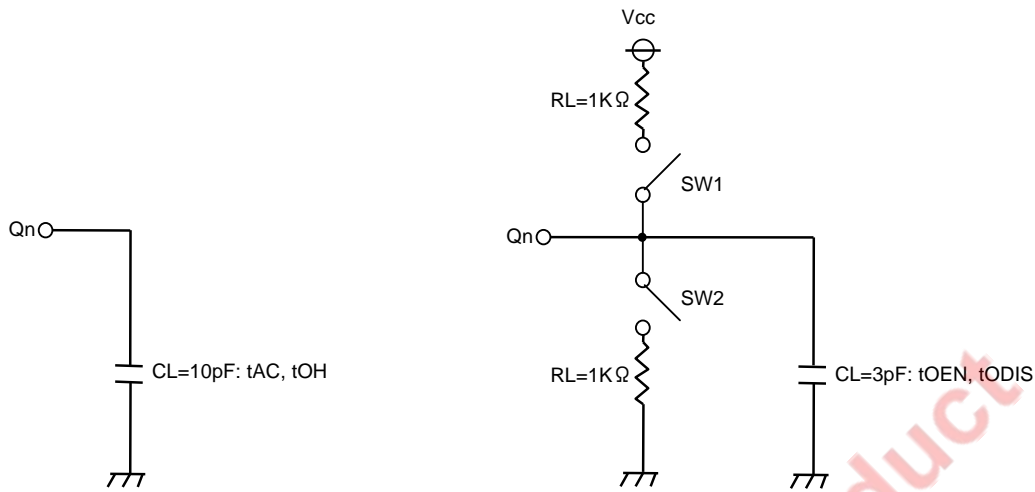


| Parameter | SW1 | SW2 |
|---|---|---|
| tODIS(LZ) | Close | Open |
| tODIS(HZ) | Open | Close |
| tOEN(ZL) | Close | Open |
| tOEN(ZH) | Open | Close |

Input pulse level : 0 ~ Vcc
Input pulse rise/fall time : 1 ns
Decision voltage input : 1/2 Vcc
Decision voltage output : 1/2 Vcc
(However, tODIS(HZ) is judged with 90% of the output amplitude, while tODIS(LZ) is judged with 10% of the output amplitude. )

The load capacitance CL includes the floating capacitance of connections and a input capacitance of a probe.

**tODIS and tOEN Measurement Conditions**

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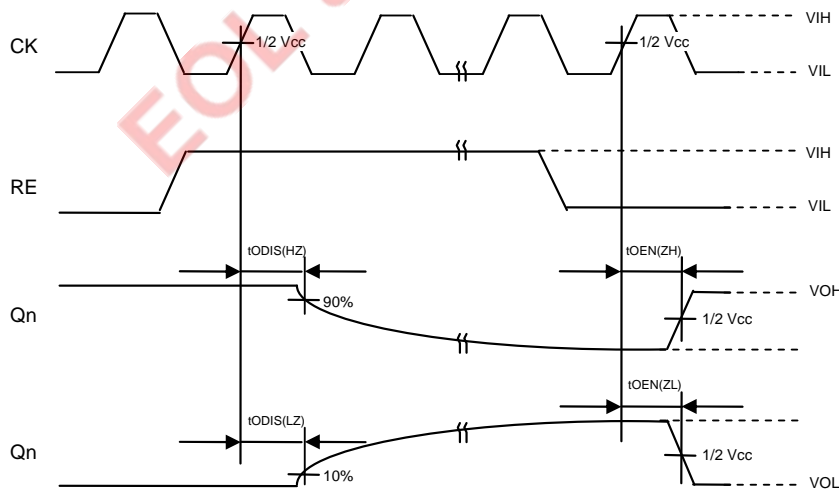
## Operating Timing

### Write Cycle
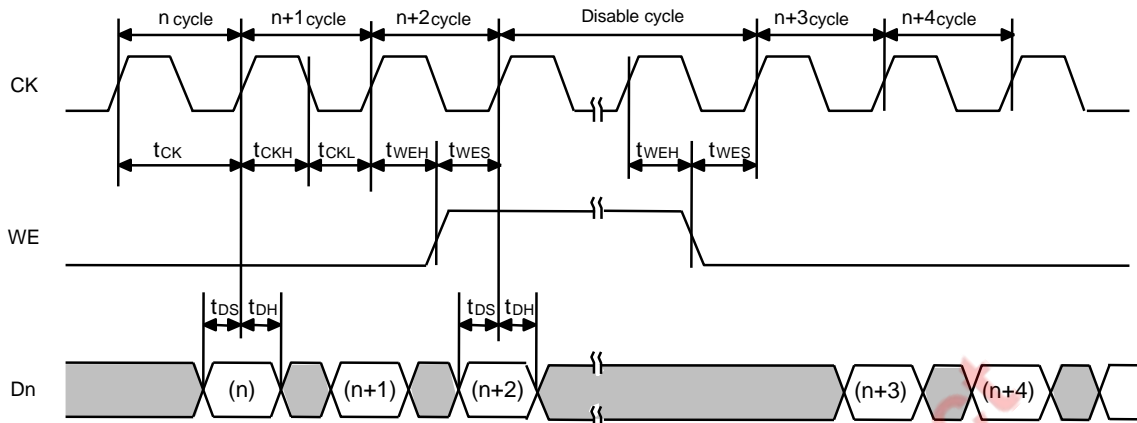


In case of WRES = "H"

### Write Reset Cycle
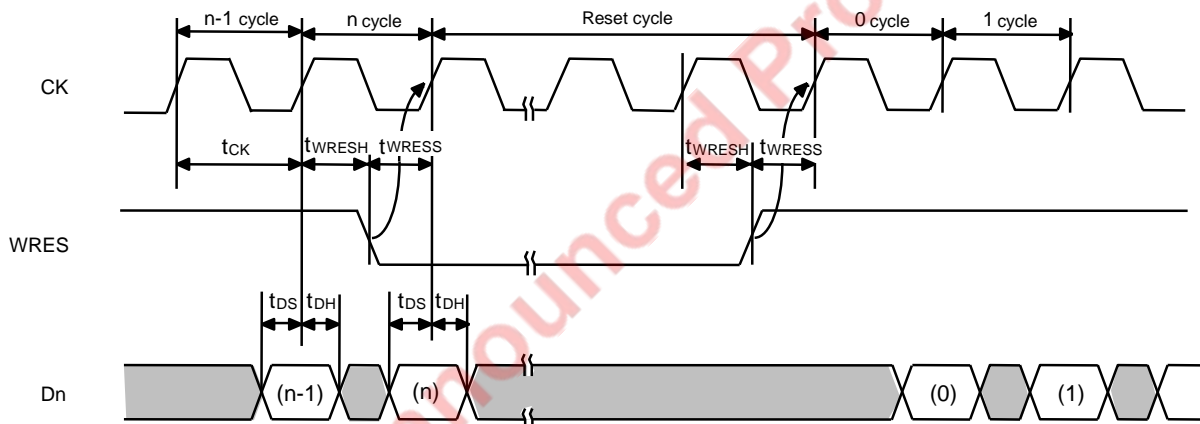


In case of WE = "L"

### Write Reset and Write Enable Combination Cycle
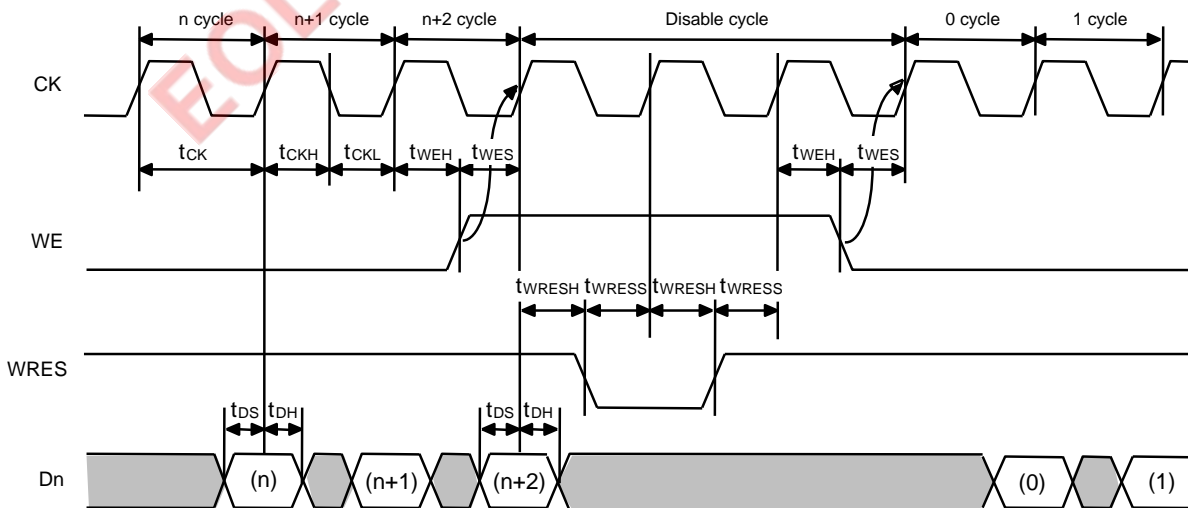


Note: There is no timing restriction of WE to WRES.

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**Read Cycle**



In case of RRES = "H"

**Read Reset Cycle**



In case of RE = "L"
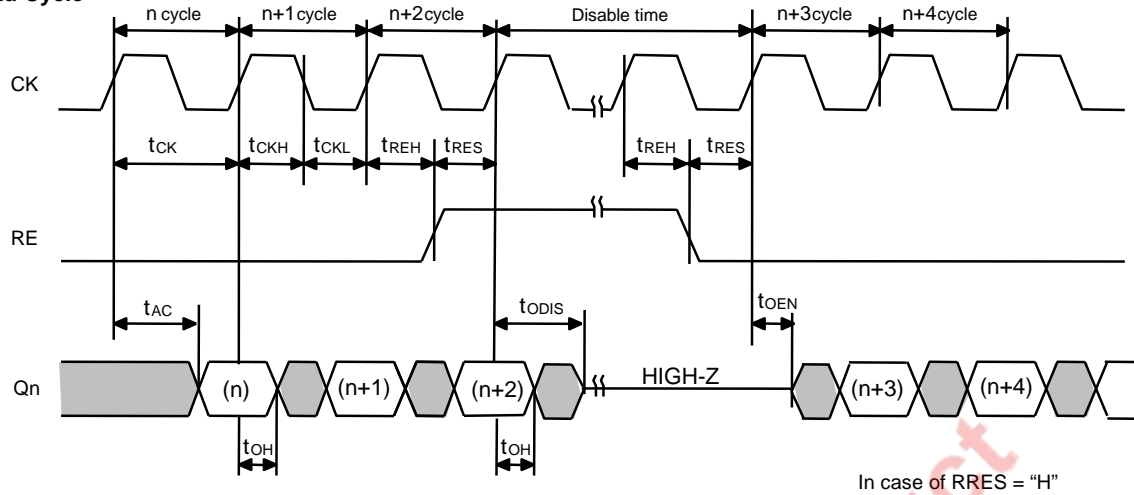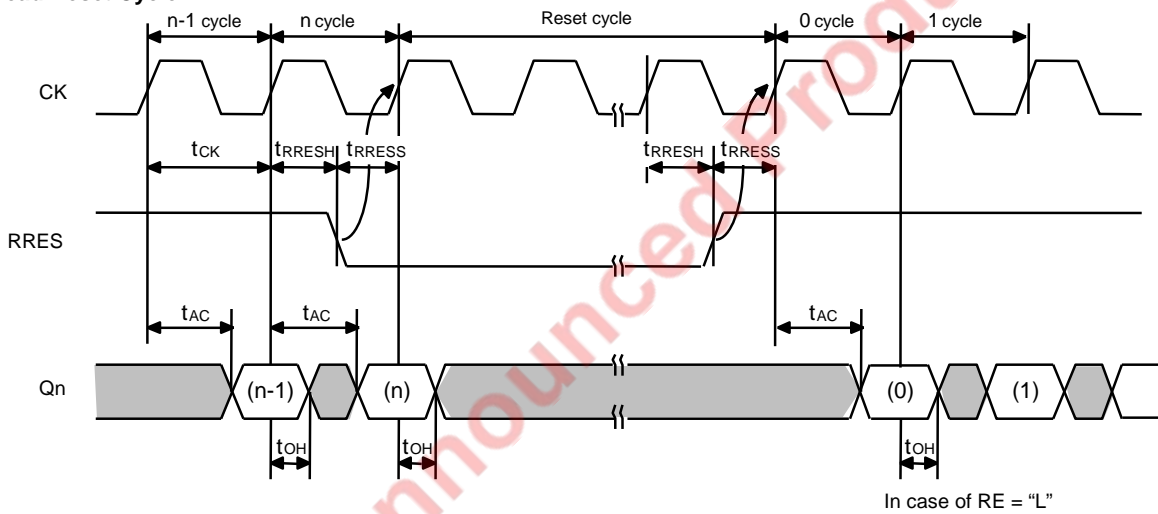
**Read Reset and Read Enable Combination Cycle**
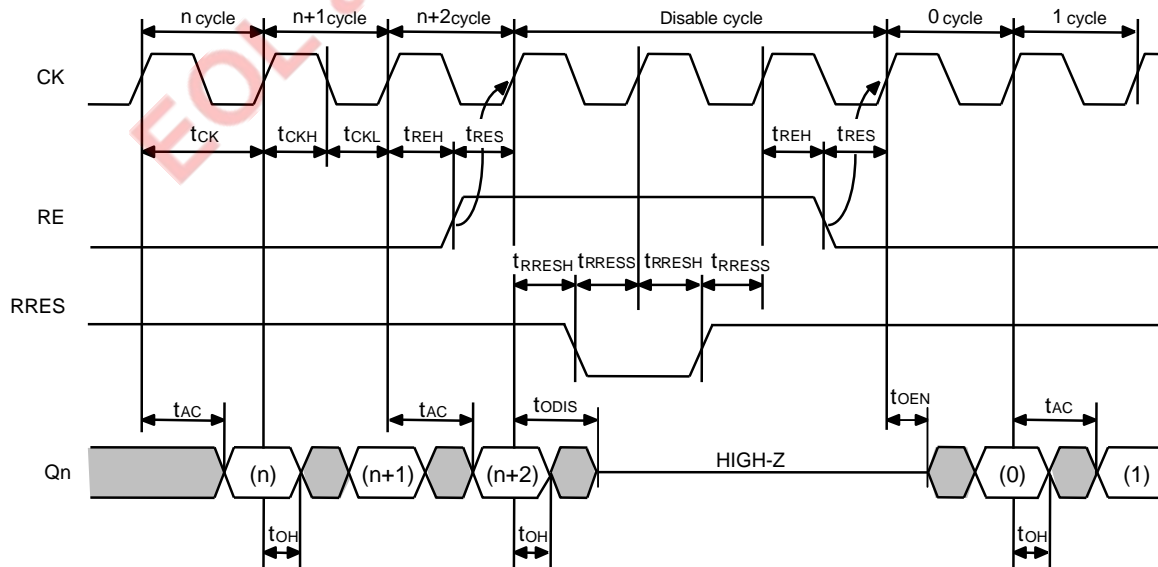


Note: There is no timing restriction of RE to RRES.

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## Caution When Write Cycle and Read Cycle Approach Each Other

The interval m between write cycle and a read cycle should be secured more than 256 cycles when the write cycle goes ahead of the read cycle on the following conditions, that is to say the interval less than 255 cycles is forbidden.

WRES, RRES="H"; WE, RE="L", and
- Both write side and read side are activated continuously.

When once this restriction to the interval isn't fulfilled, writing data is guaranteed, but reading data isn't guaranteed not only for the cycles when it isn't fulfilled but also for the following 256 cycles after it is fulfilled again.
In this 256 cycles, read disable and read reset cycles are not counted.

But the following condition is an exception to the restriction to forbid the intervals less than 255 cycles.
- Either write side or read side is temporarily stopped owing to reset cycles (WRES or RRES="L") or disable cycles (WE or RE ="H").

Note: Also, when the address counter is incremented up to the last cycle of 1-line and then returned to 0 cycle, the interval m between write and read cycles should be secured more than 256 cycles taking account that they are cyclic and serial lines.
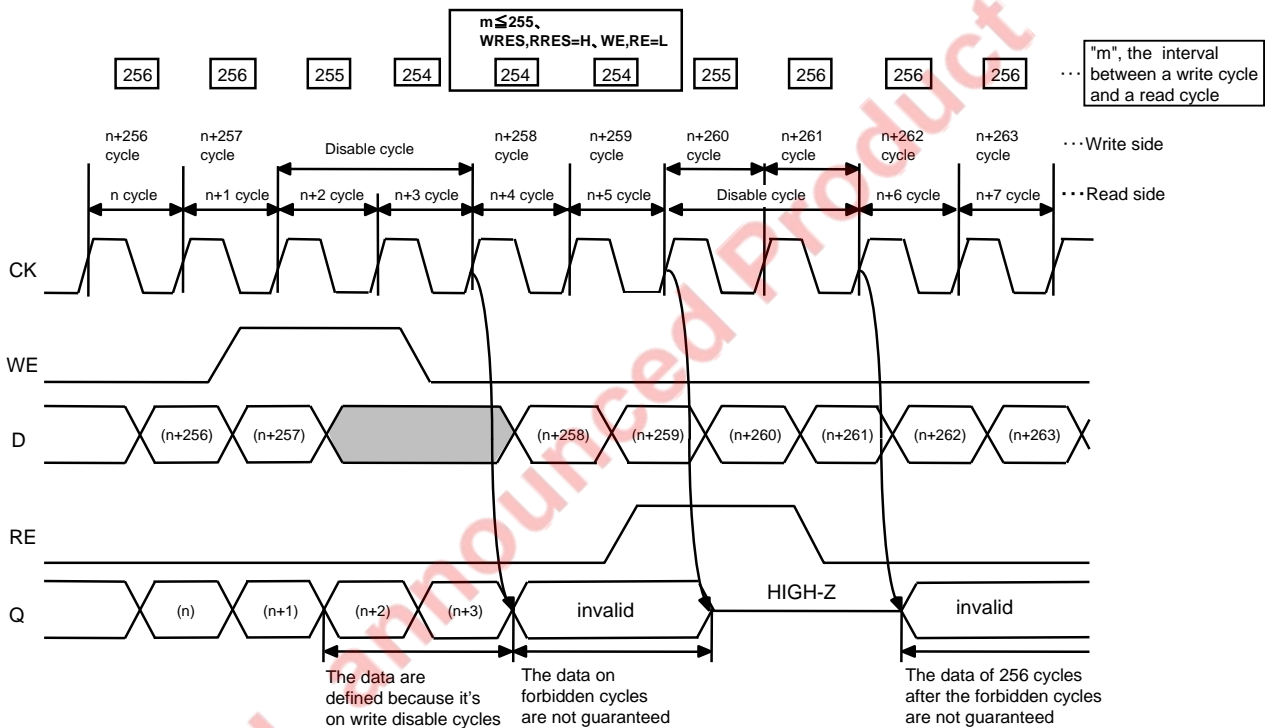


In the case of read cycle goes ahead of the write cycle or write cycle and read cycle are accorded. It's exceptions of the restriction on forbid the intervals less than 255 cycles.

## Caution of The State of Clock Stopping

Stopping of clock signal of this IC is forbidden during operating of it. "Stopping of clock signal" mean that CK is fixed at "L" or "H" for more than tck(Max)(=200ns).
When this restriction to tck isn't fulfilled, all writing data before stopping of clock signal isn't defined.
Once the clock signal stopped, 1 cycle or more of both write reset cycles and read reset cycles should be secured to operate again.

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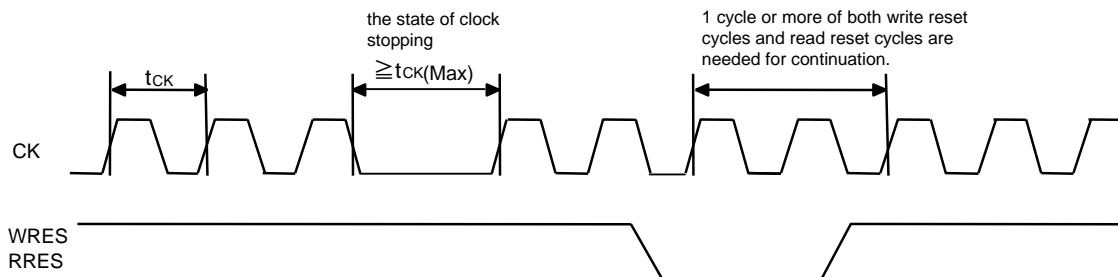
## Variable Length Delay bits

The 1-line length (cycle number) of R8A66120FFA is 1,048,576-cycle.

### 1-line Delay

In read cycles, an output data is read out at the (first) rising edge of CK (i.e. the start of the cycle).
In write cycles, an input data is written at the (second) rising edge of CK (i.e. the end of the cycle).
So 1-line delay can be made easily according to the control method of the following figure.



WE, RE="L"
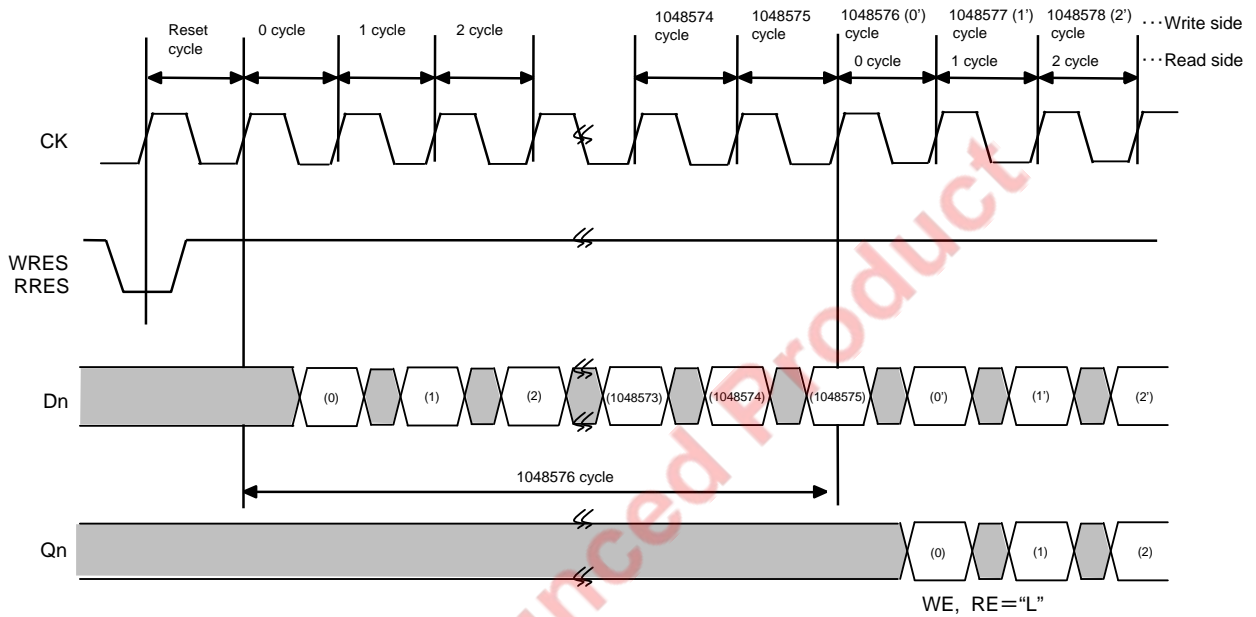
### N-bit Delay 1
### (Reset at cycles corresponding to delay length)



$1048576 \geqq in \geqq 256$
WE, RE="L"
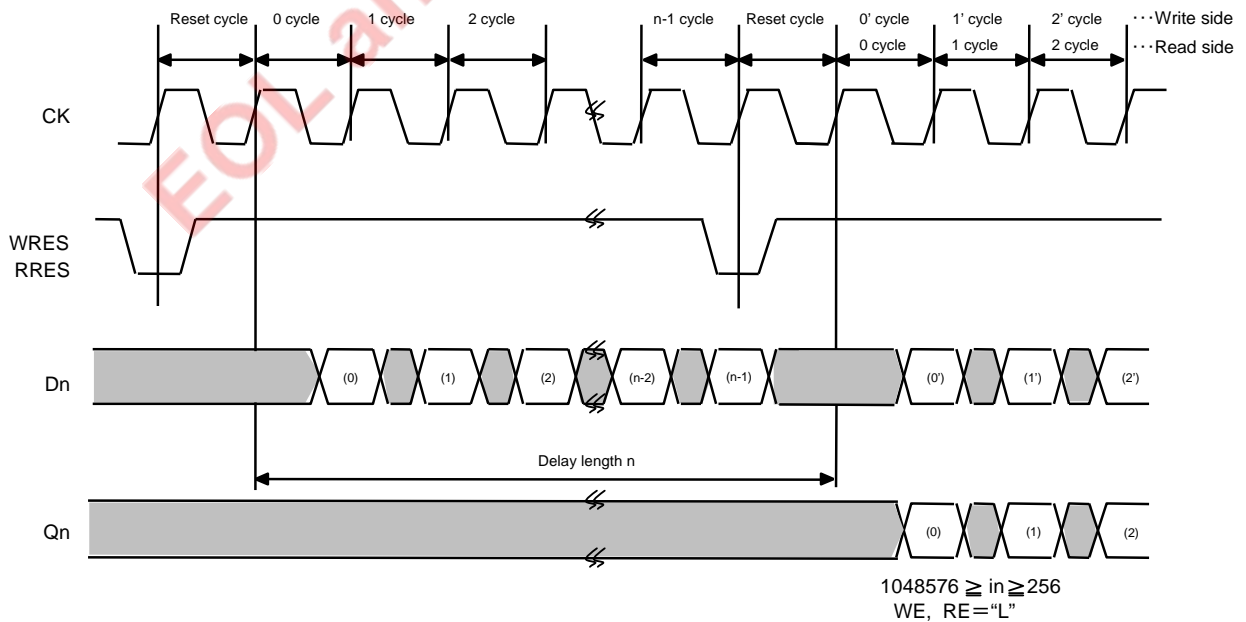
Note: Take care of the restriction to a interval between a write cycle and a read cycle (ref. page10).

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**N-bit Delay 2**
**(Sliding timings of WRES and RRES at cycles corresponding to delay length)**



1048576 ≧ n ≧ 256
WE, RE="L"
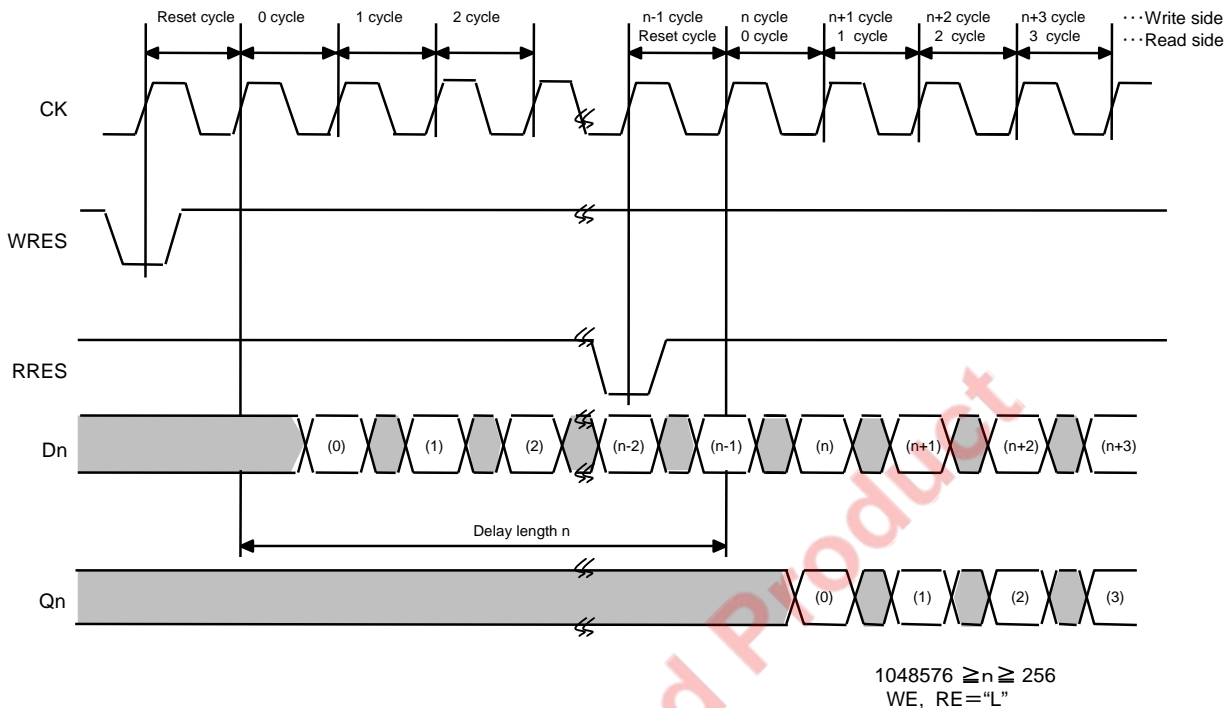
**N-bit Delay 3**
**(Sliding address by disabling RE for cycles corresponding to delay length)**



1048576 ≧ n ≧ 256
WE="L"

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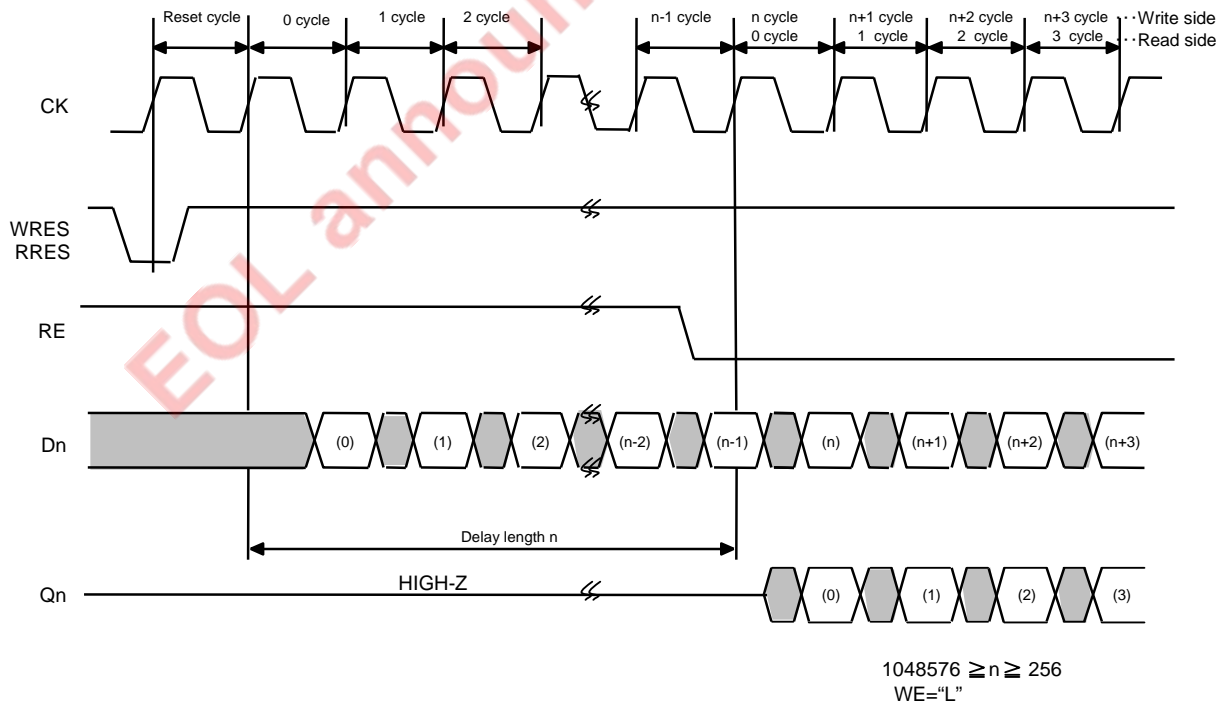
## Reading shortest a data written at n cycle on write-side

In order to read out a written data, CK should be inputted for 256 cycles and more after the data is written.
In following figure, an example is shown of reading out the data written at the rising edge of CK (*1) at n cycle on write-side.
Output data becomes invalid when this restriction isn't fulfilled.
Also, take care of the restriction to the interval between a write cycle and a read cycle (ref. page10).
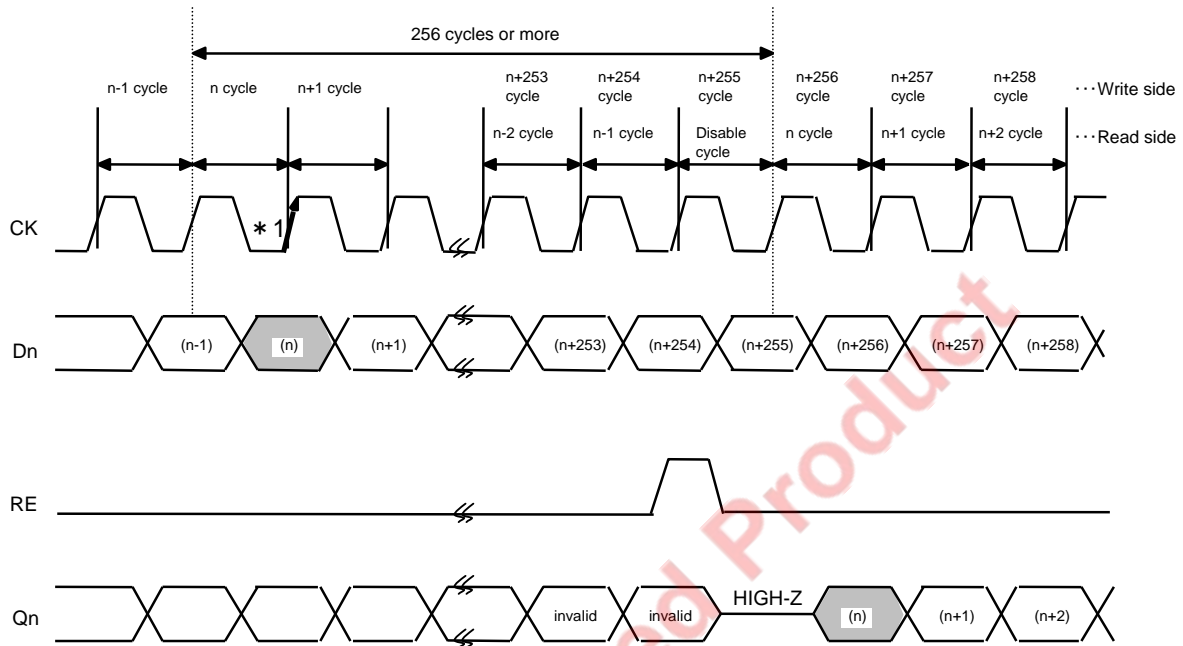


## Reading longest a data written at n cycle on write-side : 1-line Delay

Output Q of n cycle<1>* can be read out until n cycle<1>* on read-side and n cycle<2>* on write-side overlap each other.
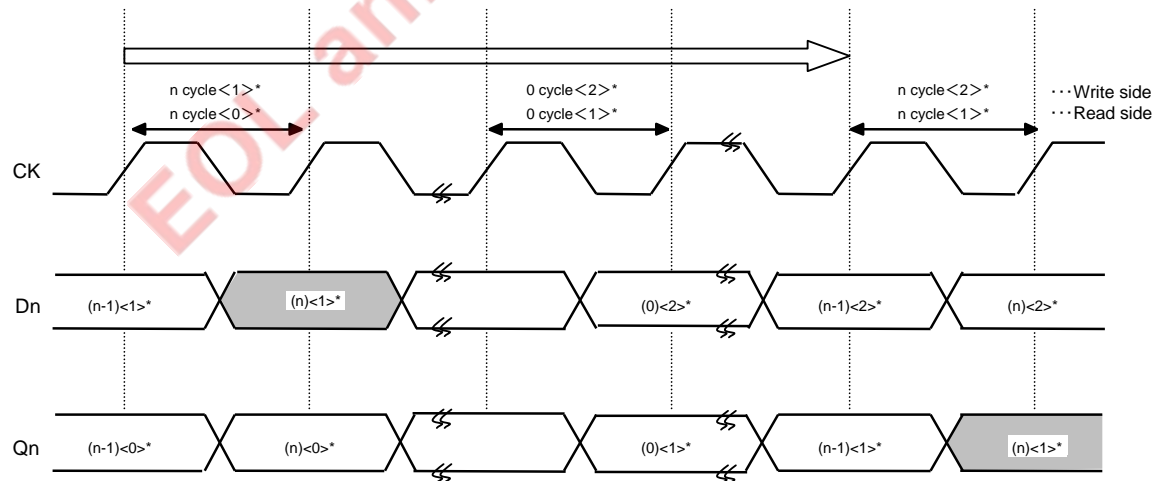


<0>* , <1>* and <2>* indicate a line number.

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## Package Outline

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP48-7x7-0.50 | PLQP0048KB-A | 48P6Q-A | 0.2g |

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Terminal cross section

Detail F

Index mark

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.9 | 7.0 | 7.1 |
| E | 6.9 | 7.0 | 7.1 |
| $A_2$ | —— | 1.4 | —— |
| $H_D$ | 8.8 | 9.0 | 9.2 |
| $H_E$ | 8.8 | 9.0 | 9.2 |
| A | —— | —— | 1.7 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.17 | 0.22 | 0.27 |
| $b_1$ | —— | 0.20 | —— |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | —— | 0.125 | —— |
| $\theta$ | 0° | —— | 8° |
| e | —— | 0.5 | —— |
| x | —— | —— | 0.08 |
| y | —— | —— | 0.10 |
| $Z_D$ | —— | 0.75 | —— |
| $Z_E$ | —— | 0.75 | —— |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | —— | 1.0 | —— |

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