

DESCRIPTION

The R8A66162SP is a semiconductor integrated circuit for LED array driver with 32-bit serial-input, parallel - output shift register, equipped with direct set input and output latches.

The R8A66162SP guarantees sufficient 24mA ($V_{CC}=5.0V$ case) output current to drive anode common LED, allowing 32-bit simultaneous and continuous current output. The parallel outputs are open-drain outputs.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products. Furthermore, pin layout ensures the realization of an easy printed circuit. R8A66162SP is the succession product of M66313FP.

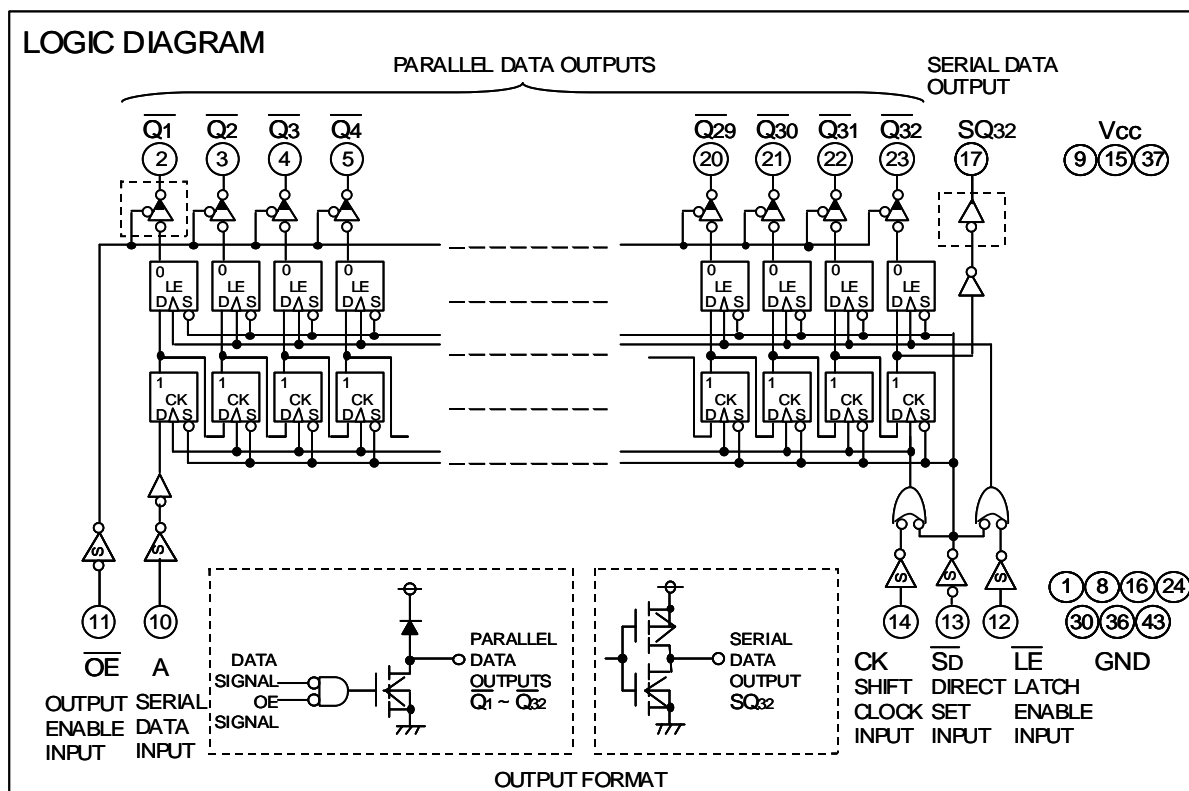
FEATURES

- Anode common LED drive
- V_{CC} 5V or 3.3V single power supply
- High output current: All parallel outputs $\overline{Q_1} \sim \overline{Q_{32}}$ $I_{OL}=24mA$ (at $V_{CC}=5.0V$), $I_{OL}=12mA$ (at $V_{CC}=3.3V$), LEDs can be turned on simultaneously.
- Low power dissipation: 200uW/package (max) ($V_{CC}=5.0V$, $T_a=25^\circ C$, quiescent state)
- High noise margin: Employment of Schmitt-trigger circuit on all inputs allows application with long wiring.
- Direct set input (\overline{SD})
- Open-drain output ($\overline{Q_1} \sim \overline{Q_{32}}$)
- Serial data output for cascading (SQ_{32})
- Wide operating temperature range ($T_a=-40^\circ C \sim +85^\circ C$)
- Pin configuration for easy layout on PCB. (Pin configuration allows easy cascade connection or LED connection)

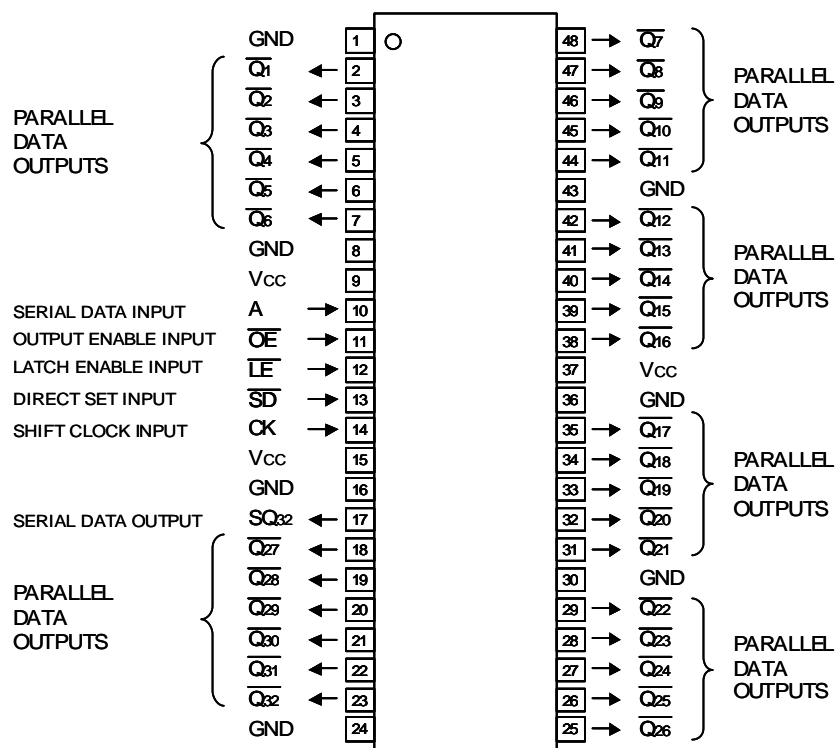
APPLICATION

- LED array drive, The various LED display modules
- PPC, Printer, VCR, Mini-compo, Button-Telephone etc. All of LED display equipments

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



FUNCTIONAL DESCRIPTION

The employment of silicon gate CMOS process of the R8A66162SP guarantees low power dissipation and maintains high noise margin as well as high output current and high speed required to drive LEDs.

Each shift register bit consists of a flip-flop for shifting and an output latch.

The shift operation takes place when the shift clock input CK changes from low-level to high-level.

The serial data input A corresponds to the data input of the first-stage shift register, and the shift register is shifted in sequence when a pulse is applied to CK.

If the latch-enable input \overline{LE} is turned high-level, the content of the shift register at that instant is latched.

The parallel data outputs $\overline{Q_1}$ ~ $\overline{Q_{32}}$ are open-drain outputs.

To expand the number of bits, use the serial data output SQ₃₂ which shows the output of the shift register of the 32nd bit.

If the direct set input \overline{SD} is turned low-level, $\overline{Q_1}$ ~ $\overline{Q_{32}}$ and SQ₃₂ are set. Then shift register and latches are set.

If the high-level input is applied to the output enable input \overline{OE} , $\overline{Q_1}$ ~ $\overline{Q_{32}}$ are set to the high-impedance state, but SQ₃₂ is not set to the high-impedance state. The shift operation is not affected when \overline{OE} is changed.

FUNCTION TABLE (Note: 1)

| OPERATION MODE | INPUT | | | | PARALLEL OUTPUTS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SERIAL OUTPUT SQ ₃₂ | |
|------------------------|-------|----|----|---|------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|--------------------------------------|------------------------------|
| | SD | CK | LE | A | OE | Q ₁ | Q ₂ | Q ₃ | Q ₄ | Q ₅ | Q ₆ | Q ₇ | Q ₈ | Q ₉ | Q ₁₀ | Q ₁₁ | Q ₁₂ | Q ₁₃ | Q ₁₄ | Q ₁₅ | Q ₁₆ | Q ₁₇ | Q ₁₈ | Q ₁₉ | Q ₂₀ | Q ₂₁ | Q ₂₂ | Q ₂₃ | Q ₂₄ | Q ₂₅ | Q ₂₆ | Q ₂₇ | Q ₂₈ | Q ₂₉ | Q ₃₀ | Q ₃₁ | | Q ₃₂ |
| SET | L | X | X | X | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | H |
| SHIFT | H | | L | H | L | L | Q ₁ ⁰ | Q ₂ ⁰ | Q ₃ ⁰ | Q ₄ ⁰ | Q ₅ ⁰ | Q ₆ ⁰ | Q ₇ ⁰ | Q ₈ ⁰ | Q ₉ ⁰ | Q ₁₀ ⁰ | Q ₁₁ ⁰ | Q ₁₂ ⁰ | Q ₁₃ ⁰ | Q ₁₄ ⁰ | Q ₁₅ ⁰ | Q ₁₆ ⁰ | Q ₁₇ ⁰ | Q ₁₈ ⁰ | Q ₁₉ ⁰ | Q ₂₀ ⁰ | Q ₂₁ ⁰ | Q ₂₂ ⁰ | Q ₂₃ ⁰ | Q ₂₄ ⁰ | Q ₂₅ ⁰ | Q ₂₆ ⁰ | Q ₂₇ ⁰ | Q ₂₈ ⁰ | Q ₂₉ ⁰ | Q ₃₀ ⁰ | Q ₃₁ ⁰ | Q ₃₂ ⁰ |
| | H | | L | L | L | Z | Q ₁ ⁰ | Q ₂ ⁰ | Q ₃ ⁰ | Q ₄ ⁰ | Q ₅ ⁰ | Q ₆ ⁰ | Q ₇ ⁰ | Q ₈ ⁰ | Q ₉ ⁰ | Q ₁₀ ⁰ | Q ₁₁ ⁰ | Q ₁₂ ⁰ | Q ₁₃ ⁰ | Q ₁₄ ⁰ | Q ₁₅ ⁰ | Q ₁₆ ⁰ | Q ₁₇ ⁰ | Q ₁₈ ⁰ | Q ₁₉ ⁰ | Q ₂₀ ⁰ | Q ₂₁ ⁰ | Q ₂₂ ⁰ | Q ₂₃ ⁰ | Q ₂₄ ⁰ | Q ₂₅ ⁰ | Q ₂₆ ⁰ | Q ₂₇ ⁰ | Q ₂₈ ⁰ | Q ₂₉ ⁰ | Q ₃₀ ⁰ | Q ₃₁ ⁰ | Q ₃₂ ⁰ |
| LATCH | H | X | H | X | L | Q ₁ ⁰ | Q ₂ ⁰ | Q ₃ ⁰ | Q ₄ ⁰ | Q ₅ ⁰ | Q ₆ ⁰ | Q ₇ ⁰ | Q ₈ ⁰ | Q ₉ ⁰ | Q ₁₀ ⁰ | Q ₁₁ ⁰ | Q ₁₂ ⁰ | Q ₁₃ ⁰ | Q ₁₄ ⁰ | Q ₁₅ ⁰ | Q ₁₆ ⁰ | Q ₁₇ ⁰ | Q ₁₈ ⁰ | Q ₁₉ ⁰ | Q ₂₀ ⁰ | Q ₂₁ ⁰ | Q ₂₂ ⁰ | Q ₂₃ ⁰ | Q ₂₄ ⁰ | Q ₂₅ ⁰ | Q ₂₆ ⁰ | Q ₂₇ ⁰ | Q ₂₈ ⁰ | Q ₂₉ ⁰ | Q ₃₀ ⁰ | Q ₃₁ ⁰ | Q ₃₂ ⁰ | |
| OUTPUT DIS- ABLE | X | X | X | X | H | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | q ₃₂ |

Note 1. $\overline{\text{Q}}^0$: Transition from low-to-high-level
 $\overline{\text{Q}}^0$: Shows the status of output $\overline{\text{Q}}$ before CK input changes
X : Irrelevant
 q^0 : The content of shift register before CK changes
q : The content of shift register
Z : High-impedance state

ABSOLUTE MAXIMUM RATINGS (Ta=-40~85°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|-------------------------------|---|---------------------------|------|
| V _{cc} | Supply voltage | | -0.5~+7.0 | V |
| V _I | Input voltage | | -0.5~V _{cc} +0.5 | V |
| V _O | Output voltage | | -0.5~V _{cc} +0.5 | V |
| I _O | Output current per output pin | $\overline{\text{Q}}_1 \sim \overline{\text{Q}}_{32}$ | 50 | mA |
| | | SQ ₃₂ | ±25 | |
| I _{cc} | Supply/GND current | V _{cc} , GND | -920, +20 | mA |
| P _d | Power dissipation | | 650 | mW |
| T _{stg} | Storage temperature range | | -65~150 | °C |

RECOMMENDED OPERATING CONDITIONS (Ta=-40~85°C, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|------------------|-----------------------------|--------------|--------|------|-----------------|------|
| | | | Min. | Typ. | Max. | |
| V _{cc} | Supply voltage | 5.0V support | 4.5 | 5.0 | 5.5 | V |
| | | 3.3V support | 3.0 | 3.3 | 3.6 | V |
| V _I | Input voltage | | 0 | | V _{cc} | V |
| V _O | Output voltage | | 0 | | V _{cc} | V |
| T _{opr} | Operating temperature range | | -40 | | 85 | °C |

ELECTRICAL CHARACTERISTICS

■ 5.0V version support specifications (Ta=-40~85°C, Vcc=4.5V~5.5V, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|-----------------|----------------------------------|---------------------------------|---|---|-----------------|------|--------------|------|
| | | | | | Min. | Typ. | Max. | |
| V _{T+} | Positive going threshold voltage | | | | 0.35xVcc | | 0.70xVcc | V |
| V _{T-} | Negative going threshold voltage | | | | 0.20xVcc | | 0.55xVcc | V |
| V _{OH} | High level output voltage | SQ ₃₂ | V _I =V _{T+} , V _{T-} Vcc=4.5V | I _{OH} =-20uA I _{OH} =-4mA | Vcc-0.1 3.66 | | | V |
| V _{OL} | Low level output voltage | Q ₁ ~Q ₃₂ | V _I =V _{T+} , V _{T-} Vcc=4.5V | I _{OL} =20uA | | | 0.10 | V |
| | | | | I _{OL} =24mA | | | 0.50 | |
| | | | | I _{OL} =28mA | | | 0.55(Notes2) | |
| | | | | I _{OL} =20uA | | | 0.10 | |
| | | I _{OL} =4mA | | | | 0.53 | | |
| | | SQ ₃₂ | | | | | | |
| I _{IH} | High level input current | | V _I =Vcc | Vcc=5.5V | | | 5 | uA |
| I _{IL} | Low level input current | | V _I =GND | Vcc=5.5V | | | -5 | uA |
| I _O | Maximum output leakage current | Q ₁ ~Q ₃₂ | V _I =V _{T+} , V _{T-} Vcc=5.5V | V _O =Vcc | | | 10 | uA |
| | | | | V _O =GND | | | -10 | |
| I _{cc} | Quiescent supply current | | V _I =Vcc, GND | Vcc=5.5V | | | 400 | uA |

Note2 : Ta = -40~70°C

■ 3.3V version support specifications (Ta=-40~85°C, Vcc=3.0V~3.6V, unless otherwise noted)

| Symbol | Parameter | | Test conditions | | Limits | | | Unit |
|-----------------|----------------------------------|---------------------------------|---|---|-----------------|------|----------|------|
| | | | | | Min. | Typ. | Max. | |
| V _{T+} | Positive going threshold voltage | | | | 0.35xVcc | | 0.70xVcc | V |
| V _{T-} | Negative going threshold voltage | | | | 0.20xVcc | | 0.55xVcc | V |
| V _{OH} | High level output voltage | SQ ₃₂ | V _I =V _{T+} , V _{T-} Vcc=3.0V | I _{OH} =-20uA I _{OH} =-2mA | Vcc-0.1 2.60 | | | V |
| V _{OL} | Low level output voltage | Q ₁ ~Q ₃₂ | V _I =V _{T+} , V _{T-} Vcc=3.0V | I _{OL} =20uA | | | 0.10 | V |
| | | | | I _{OL} =12mA | | | 0.54 | |
| | | SQ ₃₂ | | I _{OL} =20uA | | | 0.10 | |
| | | | | I _{OL} =2mA | | | 0.40 | |
| I _{IH} | High level input current | | V _I =Vcc | Vcc=3.6V | | | 5 | uA |
| I _{IL} | Low level input current | | V _I =GND | Vcc=3.6V | | | -5 | uA |
| I _O | Maximum output leakage current | Q ₁ ~Q ₃₂ | V _I =V _{T+} , V _{T-} Vcc=3.6V | V _O =Vcc | | | 10 | uA |
| | | | | V _O =GND | | | -10 | |
| I _{cc} | Quiescent supply current | | V _I =Vcc, GND | Vcc=3.6V | | | 400 | uA |

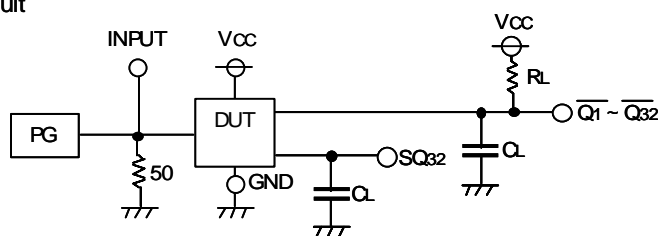
SWITCHING CHARACTERISTICS (Ta=-40~85°C, Vcc=5.0V or 3.3V, unless otherwise noted)

| Symbol | Parameter | Test conditions | 5.0V specification | | | 3.3V specification | | | Unit |
|----------------|---|---|--------------------|------|------|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| f_{max} | Maximum clock frequency | | | | 4 | | | 3.3 | MHz |
| tPZL | Output "Z-L" and "L-Z" propagation time | CK- $\overline{Q_1} \sim \overline{Q_{32}}$ (Turned on) | | | 200 | | | 220 | ns |
| tPLZ | | CK- $\overline{Q_1} \sim \overline{Q_{32}}$ (Turned off) | | | 250 | | | 270 | ns |
| tPLH | Output "L-H" and "H-L" propagation time | CK-SQ ₃₂ | | | 125 | | | 150 | ns |
| tPHL | | | | | 125 | | | 150 | ns |
| tPZL | Output "Z-L" propagation time | $\overline{S_D} - \overline{Q_1} \sim \overline{Q_{32}}$ (Turned on) | | | 200 | | | 220 | ns |
| tPLH | Output "L-H" propagation time | $\overline{S_D} - \overline{Q_{32}}$ | | | 125 | | | 150 | ns |
| tPZL | Output "Z-L" and "L-Z" propagation time | $\overline{LE} - \overline{Q_1} \sim \overline{Q_{32}}$ (Turned on) | | | 125 | | | 150 | ns |
| tPLZ | | $\overline{LE} - \overline{Q_1} \sim \overline{Q_{32}}$ (Turned off) | | | 200 | | | 220 | ns |
| tPZL | Output "Z-L" and "L-Z" propagation time | $\overline{OE} - \overline{Q_1} \sim \overline{Q_{32}}$ (Turned on) | | | 125 | | | 150 | ns |
| tPLZ | | $\overline{OE} - \overline{Q_1} \sim \overline{Q_{32}}$ (Turned off) | | | 200 | | | 220 | ns |
| C _i | Input capacitance | | | | 10 | | | 10 | pF |
| C _o | Output capacitance | $\overline{OE} = V_{cc}$ | | | 15 | | | 15 | pF |

TIMING REQUIREMENTS (Ta=-40~85°C, Vcc=5.0V or 3.3V, unless otherwise noted)

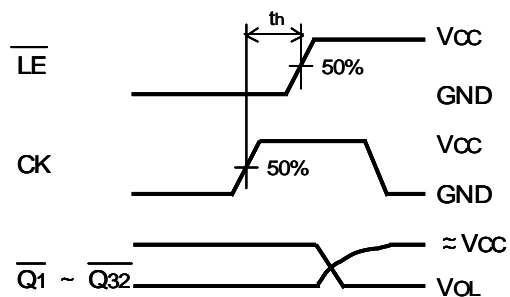
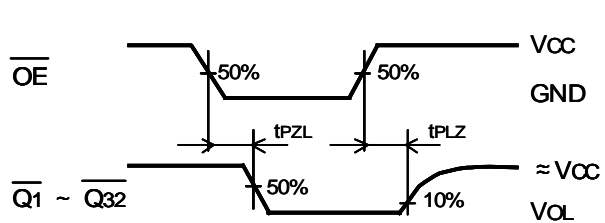
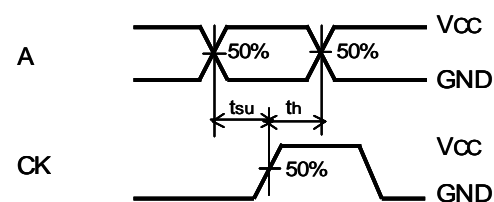
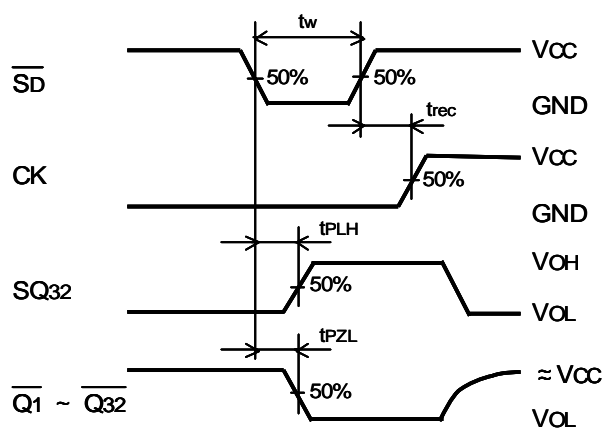
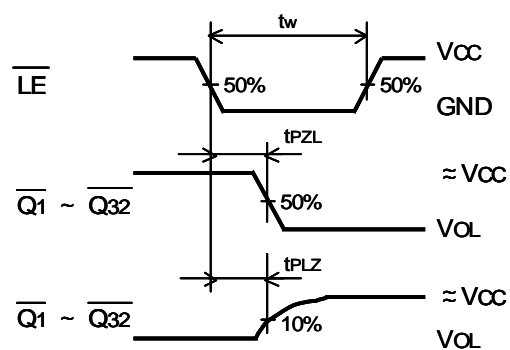
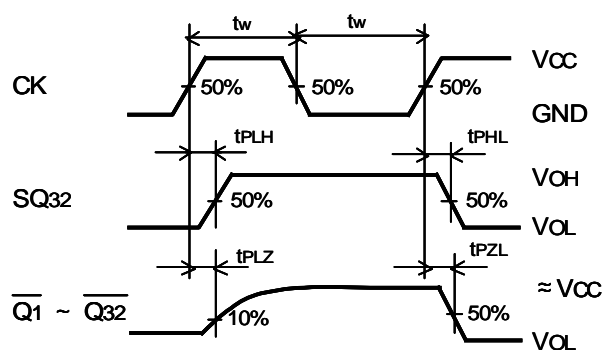
| Symbol | Parameter | Test conditions | 5.0V specification | | | 3.3V specification | | | Unit |
|------------------|--|-----------------|--------------------|------|------|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| t _w | CK, \overline{LE} , $\overline{S_D}$ pulse width | (Note3) | 125 | | | 150 | | | ns |
| t _{su} | Setup time A to CK | | 125 | | | 150 | | | ns |
| t _h | Hold time A to CK | | 15 | | | 20 | | | ns |
| | Hold time \overline{LE} to CK | | 70 | | | 80 | | | ns |
| t _{rec} | Recovery time CK to $\overline{S_D}$ | | 70 | | | 80 | | | ns |

Note3. Test circuit



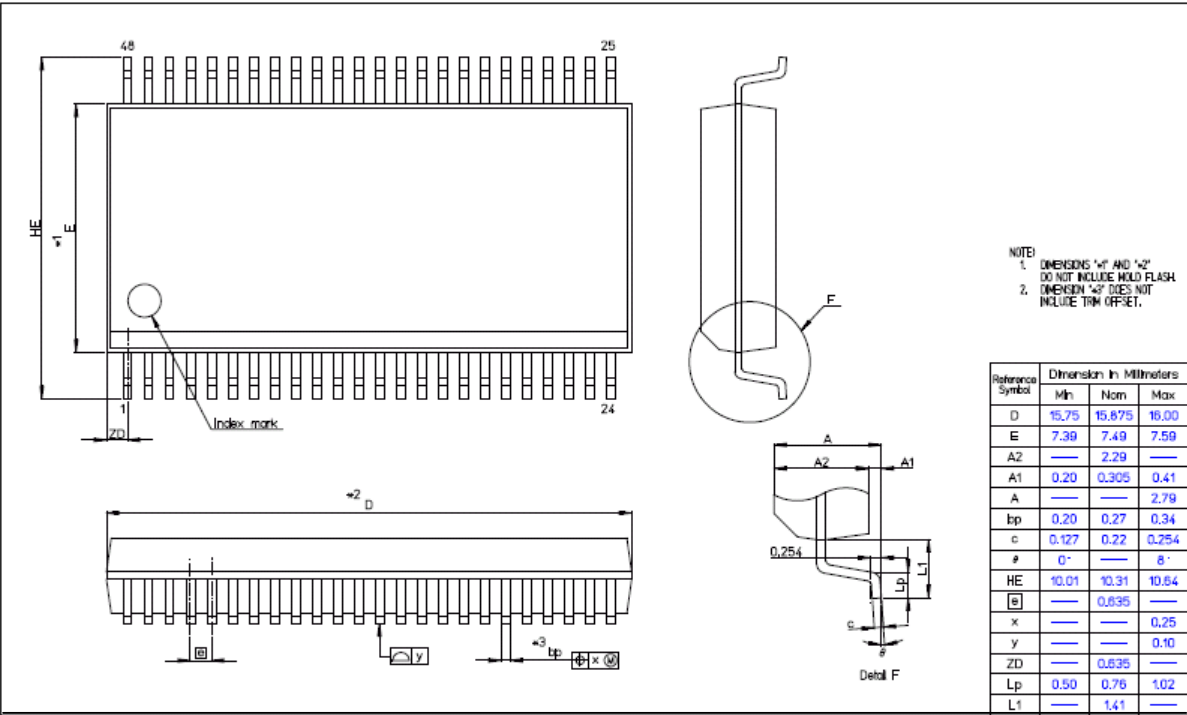
- (1) The pulse generator(PG) has the following characteristics(10%~90%):tr=6ns,tf=6ns
 (2) The capacitance CL includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



PACKAGE OUTLINE

| | | |
|------------|--------------|---------------|
| Package | RENESAS Code | Previous Code |
| 48pin SSOP | PRSP0048ZB-A | 48P2X-A |



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Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
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Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510