Description

The MK3720D and MK3720B are drop-in replacements for the MK3720S and MK3720A devices. Compared to these earlier devices the MK3720D and MK3720B offer a wider operating frequency range and improved power supply noise rejection.

The MK3720 is a low cost, low jitter, high performance 3.3 Volt VCXO designed to replace expensive 13.5, 27, or 54 MHz VCXOs. The patented on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by ±100 ppm. Using ICS' patented VCXO and analog/digital Phase-Locked Loop (PLL) techniques, the device uses an inexpensive external pullable crystal input to produce output clocks of 13.5 MHz, 27 MHz, and 54 MHz.

The MK3720D exhibits a moderate VCXO gain of 120ppm/V typical, when used with a high quality external pullable quartz crystal. The MK3720B offers a higher VCXO gain of 150ppm/V, similar to the earlier MK3720A. The higher intrinsic VCXO gain of the MK3720B may help compensate for the reduced pullability of a low quality crystal used in some applications. However, higher VCXO gain may also increase clock output phase noise.

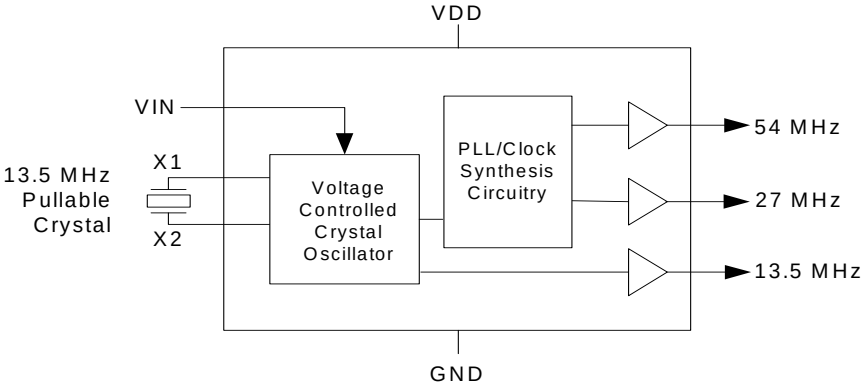
The frequency of the on-chip VCXO is adjusted by an external control voltage input into pin VIN. Because VIN is a high impedance input, it can be driven directly from an PWM RC integrator circuit.

Features

- MK3720D and MK3720B are drop-in upgrades to the earlier MK3720S and MK3720A devices
- Packaged in 8 pin SOIC
- Operating voltage of 3.3 V (±5%)
- Output clocks of 54, 27, and 13.5 MHz
- Uses an inexpensive 13.500 MHz external crystal
- On-chip VCXO (patented) with pull range of 200ppm (minimum)
- VCXO tuning voltage of 0 to 3.3V
- 12mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process

MK3720D is Recommended for New Designs

Block Diagram



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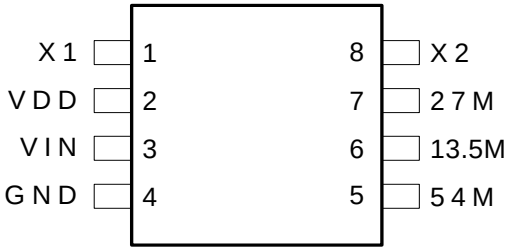
Pin Assignment



MK3720B
MK3720D

8 Pin (150 mil) SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI	Input	Crystal connection. Connect to the external pullable crystal.
2	VDD	Power	Connect to +3.3 V (0.01uf decoupling capacitor recommended).
3	VIN	Input	Voltage input to VCXO. Zero to 3.3 V analog input which controls the oscillation frequency of the VCXO.
4	GND	Power	Connect to ground.
5	54M	Output	54 MHz VCXO clock output.
6	13.5	Output	13.5 MHz VCXO clock output.
7	27	Output	27 MHz VCXO clock output.
8	X2	Input	Crystal connection. Connect to the external pullable crystal.

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External Component Selection

The MK3720 requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD (pin 2) and GND (pin 4), as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output (CLK, pin 5) and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Quartz Crystal

The MK3720 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section shown must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The MK3720 incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the MK3720 is designed to have zero frequency error when the total of on-chip + stray capacitance is 14pF.

Recommended Crystal Parameters:

See application note MAN05 for crystal information. MAN05 is available on the internet at www.icst.com/pdf/man05.pdf.

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the MK3720. There should be no via’s between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

To determine the need for and value of the crystal adjustment capacitors, you will need a PC board of your final layout, a frequency counter capable of about 1 ppm resolution and accuracy, two power supplies, and some samples of the crystals which you plan to use in production, along with measured initial accuracy for each crystal at the specified crystal load capacitance, CL.

To determine the value of the crystal capacitors:

1. Connect VDD of the MK3720 to 3.3V. Connect pin 3 of the MK3720 to the second power supply. Adjust the voltage on pin 3 to 0V. Measure and record the frequency of the CLK output.

2. Adjust the voltage on pin 3 to 3.3V. Measure and record the frequency of the same output.

To calculate the centering error:

$$Error = 10^6 x\left[\frac{(f_{3.0V} - f_{target}) + (f_{0V} - f_{target})}{f_{target}}\right] - error_{xtal}$$

Where:

f_{target} = nominal crystal frequency

$error_{xtal}$ =actual initial accuracy (in ppm) of the crystal being measured

If the centering error is less than ±25 ppm, no adjustment is needed. If the centering error is more than 25ppm negative, the PC board has excessive stray capacitance and a new PCB layout should be considered to reduce stray capacitance. (Alternately, the crystal may be re-specified to a higher load capacitance. Contact ICS MicroClock for details.) If the centering error is more than 25ppm positive, add

identical fixed centering capacitors from each crystal pin to ground. The value for each of these caps (in pF) is given by:

External Capacitor =

2 x (centering error)/(trim sensitivity)

Trim sensitivity is a parameter which can be supplied by your crystal vendor. If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the measurement to verify that the remaining error is acceptably low (typically less than ±25ppm).

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3720. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0	–	+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V
Reference crystal parameters	Refer to page 3			

DC Electrical Characteristics

VDD=3.3V ±5% , Ambient temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No load		13		mA
Short Circuit Current	I_{OS}			±50		mA
VIN, VCXO Control Voltage	V_{IA}		0		3.3	V

AC Electrical Characteristics

VDD = 3.3V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Units
Crystal Pullability		F_P	0V≤ VIN ≤ 3.3V, Note 1	± 115			ppm
VCXO Gain							
	MK3720D, Note 3		VIN = VDD/2 ± 1V, Note 1		120		ppm/V
	MK3720B, Note 3		VIN = VDD/2 ± 1V, Note 1		150		ppm/V
Output Rise Time		t_{OR}	0.8 to 2.0V, C_L=15pF			1.5	ns
Output Fall Time		t_{OF}	2.0 to 0.8V, C_L=15pF			1.5	ns
Output Clock Duty Cycle		t_D	Measured at 1.4V, C_L=15pF	45	50	55	%
Maximum Output Jitter, short term		t_J	C_L=15pF, 13.5M CLK		80		ps
			C_L=15pF, 27M and 54M CLK		150		ps

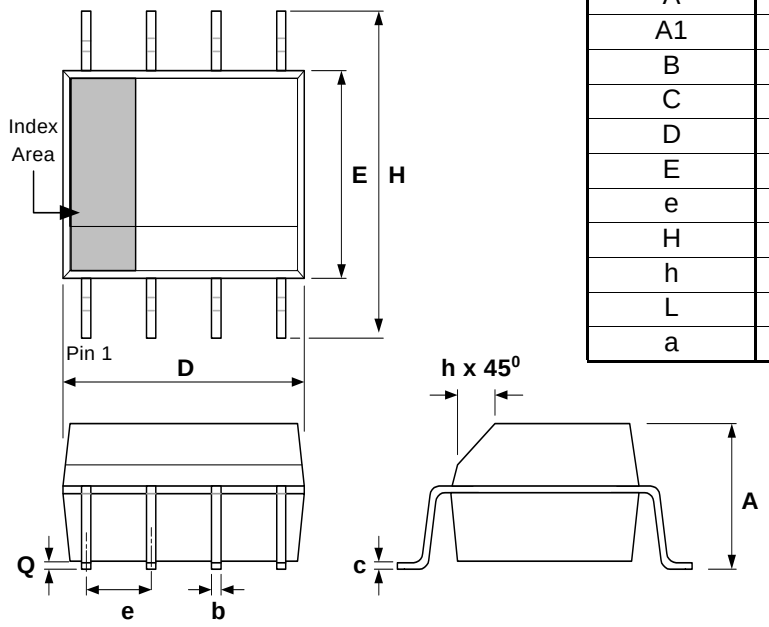
Note 1: External crystal device must conform with Pullable Crystal Specifications listed on page 3.

Note 2: Original MK3720S and MK3720A provided ± 100 ppm crystal pullability.

Note 3: Original MK3720S and MK3720A provided 100 and 170 ppm/V respectively.

Package Outline and Package Dimensions (8 pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	0.0532	0.0688
A1	1.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	0.1497	0.1574
e	1.27 Basic		0.050 Basic	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
a	0°	8°	0°	8°

Ordering Information

Part / Order Number (Note 1)	Marking	Shipping packaging	Package	Temperature
MK3720D	MK3720D	Tubes	8 pin SOIC	0 to +70° C
MK3720DTR	MK3720D	Tape and Reel	8 pin SOIC	0 to +70° C
MK3720B	MK3720B	Tubes	8 pin SOIC	0 to +70° C
MK3720BTR	MK3720B	Tape and Reel	8 pin SOIC	0 to +70° C

Note 1: MK3720D is recommended for new designs. Call factory for information on MK3720A and MK3720S.