

### Advanced Information

- 1 048 576 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast Page Mode Operation
- Performance:

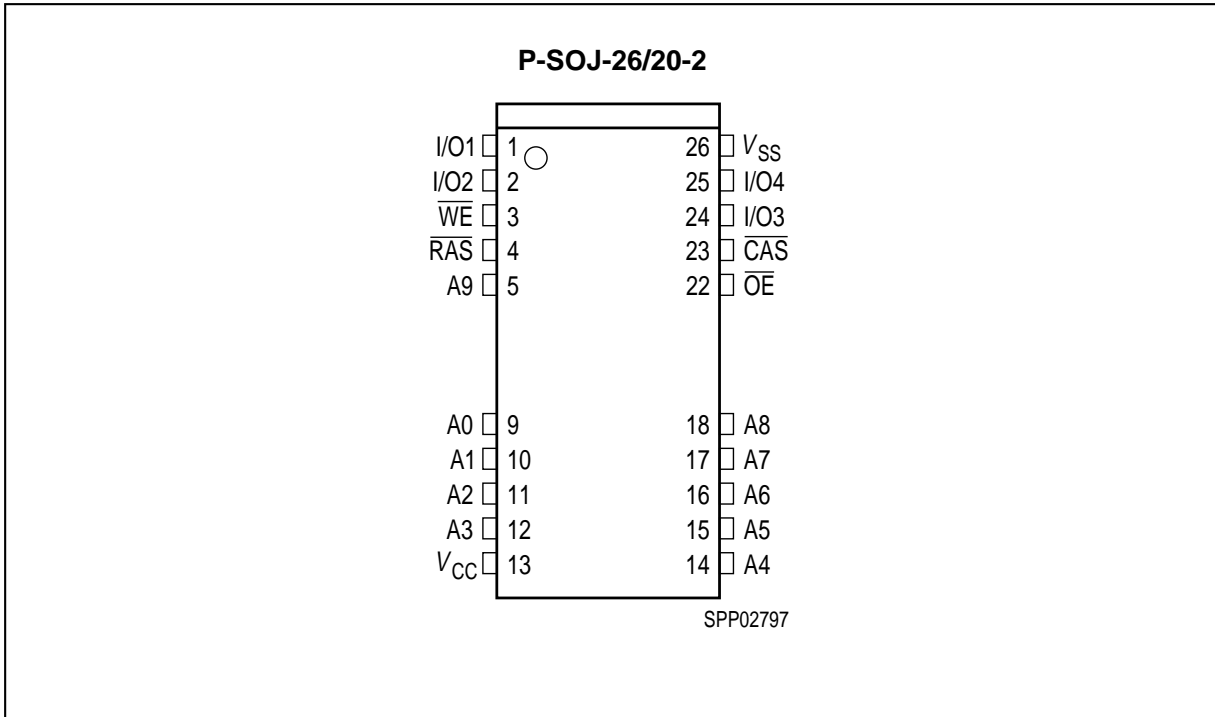
		-50	-60	
$t_{RAC}$	$\overline{RAS}$ access time	50	60	ns
$t_{CAC}$	$\overline{CAS}$ access time	13	15	ns
$t_{AA}$	Access time from address	25	30	ns
$t_{RC}$	Read/Write cycle time	95	110	ns
$t_{PC}$	Fast page mode cycle time	35	40	ns

- Single + 5 V ( $\pm 10\%$ ) supply with a built-in VBB generator
- Low power dissipation  
max. 660 mW active (-50 version)  
max. 605 mW active (-60 version)
- Standby power dissipation:  
11 mW max. standby (TTL)  
5.5 mW max. standby (CMOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify write,  $\overline{CAS}$ -before- $\overline{RAS}$  refresh,  $\overline{RAS}$ -only refresh, hidden refresh and test mode capability
- All inputs and outputs TTL-compatible
- 1024 refresh cycles / 16 ms
- Plastic Packages: P-SOJ-26/20-2 with 300 mil width

The HYB 514400BJ/BJL is the new generation dynamic RAM organized as 1 048 576 words by 4-bit. The HYB 514400BJ/BJL utilizes CMOS silicon gate process as well as advances circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514400BJ/BJL to be packed in a standard plastic P-SOJ-26/20 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 5 V ( $\pm 10\%$ ) power supply, direct interfacing with high performance logic device families such as Schottky TTL.

**Ordering Information**

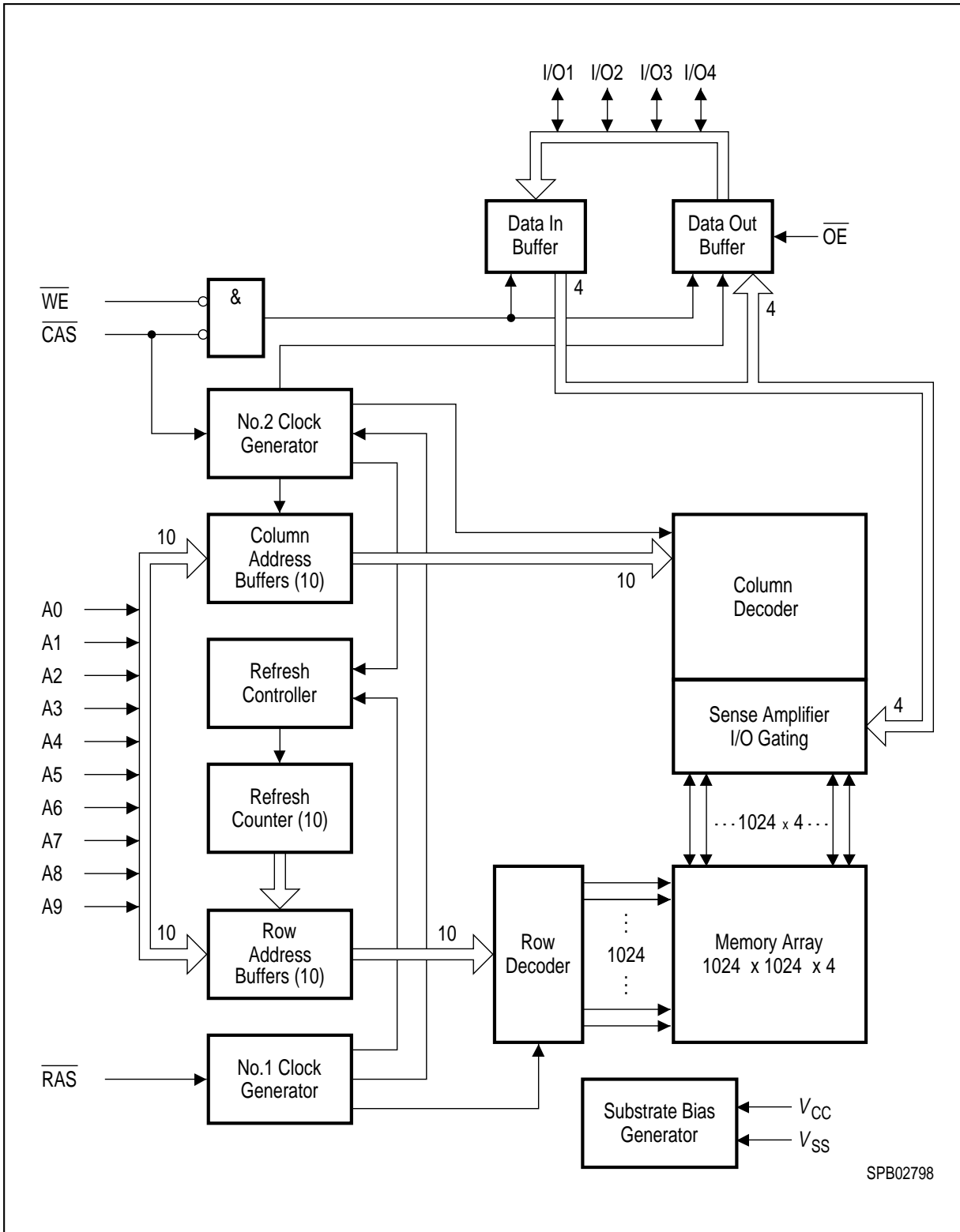
Type	Ordering Code	Package	Descriptions
HYB 514400BJ-50	Q67100-Q973	P-SOJ-26/20-2 300 mil	DRAM (access time 50 ns)
HYB 514400BJ-60	Q67100-Q756	P-SOJ-26/20-2 300 mil	DRAM (access time 60 ns)



**Pin Configuration**

**Pin Names**

A0 - A9	Address Input
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read/Write Input
OE	Output Enable
I/O1 - I/O4	Data Input/Output
V <sub>CC</sub>	Power Supply (+ 5 V)
V <sub>SS</sub>	Ground (0 V)
N.C.	No Connection



SPB02798

Block Diagram

### Absolute Maximum Ratings

Operating temperature range .....	0 to 70 °C
Storage temperature range.....	- 55 to + 150 °C
Input/output voltage .....	- 1 to + 7 V
Power Supply voltage .....	- 1 to + 7 V
Data out current (short circuit) .....	50 mA

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### DC Characteristics

$T_A = 0$  to 70 °C,  $V_{SS} = 0$  V,  $V_{CC} = 5$  V ± 10 %,  $t_T = 5$  ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	$V_{IH}$	2.4	$V_{CC} + 0.5$	V	1
Input low voltage	$V_{IL}$	- 1.0	0.8	V	1
Output high voltage ( $I_{OUT} = - 5$ mA)	$V_{OH}$	2.4	-	V	1
Output low voltage ( $I_{OUT} = 4.2$ mA)	$V_{OL}$	-	0.4	V	1
Input leakage current, any input ( $0$ V < $V_{IN} < 7$ , all other input = 0 V)	$I_{I(L)}$	- 10	10	μA	1
Output leakage current (DO is disabled, $0 < V_{OUT} < V_{CC}$ )	$I_{O(L)}$	- 10	10	μA	1
Average $V_{CC}$ supply current -50 version -60 version	$I_{CC1}$	-	120 110	mA	2, 3, 4
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = \overline{WE} = V_{IH}$ )	$I_{CC2}$	-	2	mA	
Average $V_{CC}$ supply current during $\overline{RAS}$ -only refresh cycles -50 version -60 version	$I_{CC3}$	-	120 110	mA	2, 4
Average $V_{CC}$ supply current during fast page mode operation -50 version -60 version	$I_{CC4}$	-	80 70	mA	2, 3, 4
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = \overline{WE} = V_{CC} - 0.2$ V)	$I_{CC5}$	-	1	mA	1
Average $V_{CC}$ supply current during $\overline{CAS}$ -before- $\overline{RAS}$ refresh mode -50 version -60 version	$I_{CC6}$	-	120 110	mA	2, 4

#### Capacitance

$T_A = 0$  to  $70$  °C;  $V_{CC} = 5$  V ± 10 %;  $f = 1$  MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9)	$C_{I1}$	–	5	pF
Input capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{OE}$ )	$C_{I2}$	–	7	pF
Output capacitance (IO1 to IO4)	$C_{IO}$	–	7	pF

#### AC Characteristics <sup>5,6</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V ± 10 %,  $t_T = 5$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

#### Common Parameters

Random read or write cycle time	$t_{RC}$	95	–	110	–	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	35	–	40	–	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	50	10k	60	10k	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	13	10k	15	10k	ns	
Row address setup time	$t_{ASR}$	0	–	0	–	ns	
Row address hold time	$t_{RAH}$	8	–	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	0	–	ns	
Column address hold time	$t_{CAH}$	10	–	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	18	37	20	45		
$\overline{RAS}$ to column address delay time	$t_{RAD}$	13	25	15	30	ns	
$\overline{RAS}$ hold time	$t_{RSH}$	13	–	15	–	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	50	–	60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	–	5	–	ns	
Transition time (rise and fall)	$t_T$	3	50	3	50	ns	<sup>7</sup>
Refresh period	$t_{REF}$	–	16	–	16	ms	

#### Read Cycle

Access time from $\overline{RAS}$	$t_{RAC}$	–	50	–	60	ns	8,9
Access time from $\overline{CAS}$	$t_{CAC}$	–	13	–	15	ns	8,9
Access time from column address	$t_{AA}$	–	25	–	30	ns	8,10
$\overline{OE}$ access time	$t_{OEA}$	–	13	–	15	ns	

**AC Characteristics (cont'd)** <sup>5, 6</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 5$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	25	–	30	–	ns	
Read command setup time	$t_{\text{RCS}}$	0	–	0	–	ns	
Read command hold time	$t_{\text{RCH}}$	0	–	0	–	ns	11
Read command hold time referenced to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	–	0	–	ns	11
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	0	–	0	–	ns	8
Output buffer turn-off delay	$t_{\text{OFF}}$	0	13	0	15	ns	12
Output buffer turn-off delay from $\overline{\text{OE}}$	$t_{\text{OEZ}}$	0	13	0	15	ns	12
Data to $\overline{\text{CAS}}$ low delay	$t_{\text{DZC}}$	0	–	0	–	ns	13
Data to $\overline{\text{OE}}$ low delay	$t_{\text{DZO}}$	0	–	0	–	ns	13
$\overline{\text{CAS}}$ high to data delay	$t_{\text{CDD}}$	13	–	15	–	ns	14
$\overline{\text{OE}}$ high to data delay	$t_{\text{ODD}}$	13	–	15	–	ns	14

**Write Cycle**

Write command hold time	$t_{\text{WCH}}$	8	–	10	–	ns	
Write command pulse width	$t_{\text{WP}}$	8	–	10	–	ns	
Write command setup time	$t_{\text{WCS}}$	0	–	0	–	ns	15
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	13	–	15	–	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	13	–	15	–	ns	
Data setup time	$t_{\text{DS}}$	0	–	0	–	ns	16
Data hold time	$t_{\text{DH}}$	10	–	10	–	ns	16

**Read-Modify-Write Cycle**

Read-write cycle time	$t_{\text{RWC}}$	131	–	150	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	$t_{\text{RWD}}$	68	–	80	–	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	$t_{\text{CWD}}$	31	–	35	–	ns	15
Column address to $\overline{\text{WE}}$ delay time	$t_{\text{AWD}}$	43	–	50	–	ns	15
$\overline{\text{OE}}$ command hold time	$t_{\text{OEH}}$	13	–	15	–	ns	

**Fast Page Mode Cycle**

Fast page mode cycle time	$t_{\text{PC}}$	35	–	40	–	ns	
$\overline{\text{CAS}}$ precharge time	$t_{\text{CP}}$	10	–	10	–	ns	

**AC Characteristics (cont'd)** <sup>5, 6</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V ± 10 %,  $t_T = 5$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Access time from $\overline{\text{CAS}}$ precharge	$t_{\text{CPA}}$	–	30	–	35	ns	<sup>7</sup>
$\overline{\text{RAS}}$ pulse width	$t_{\text{RAS}}$	50	200k	60	200k	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ delay	$t_{\text{RHCP}}$	30	–	35	–	ns	

**Fast Page Mode Read-Modify-Write Cycle**

Fast page mode read-write cycle time	$t_{\text{PRWC}}$	71	–	80	–	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$	$t_{\text{CPWD}}$	48	–	55	–	ns	

**$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Cycle**

$\overline{\text{CAS}}$ setup time	$t_{\text{CSR}}$	10	–	10	–	ns	
$\overline{\text{CAS}}$ hold time	$t_{\text{CHR}}$	10	–	10	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	$t_{\text{RPC}}$	5	–	5	–	ns	
Write to $\overline{\text{RAS}}$ precharge time	$t_{\text{WRP}}$	10	–	10	–	ns	
Write hold time referenced to $\overline{\text{RAS}}$	$t_{\text{WRH}}$	10	–	10	–	ns	

**$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Counter Test Cycle**

$\overline{\text{CAS}}$ precharge time	$t_{\text{CPT}}$	35	–	40	–	ns	
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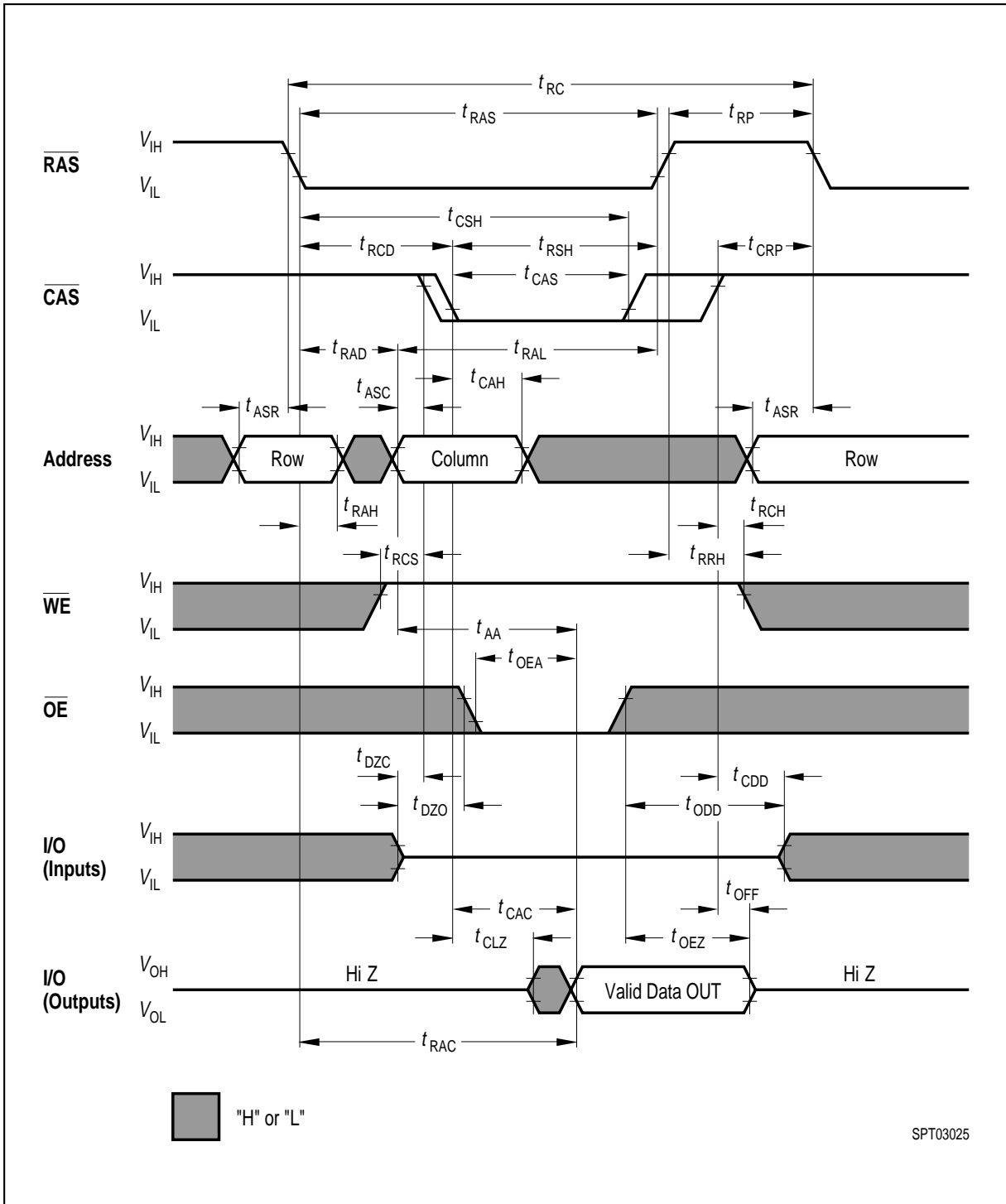
**Test Mode**

Write command setup time	$t_{\text{WTS}}$	10	–	10	–	ns	
Write command hold time	$t_{\text{WTH}}$	10	–	10	–	ns	

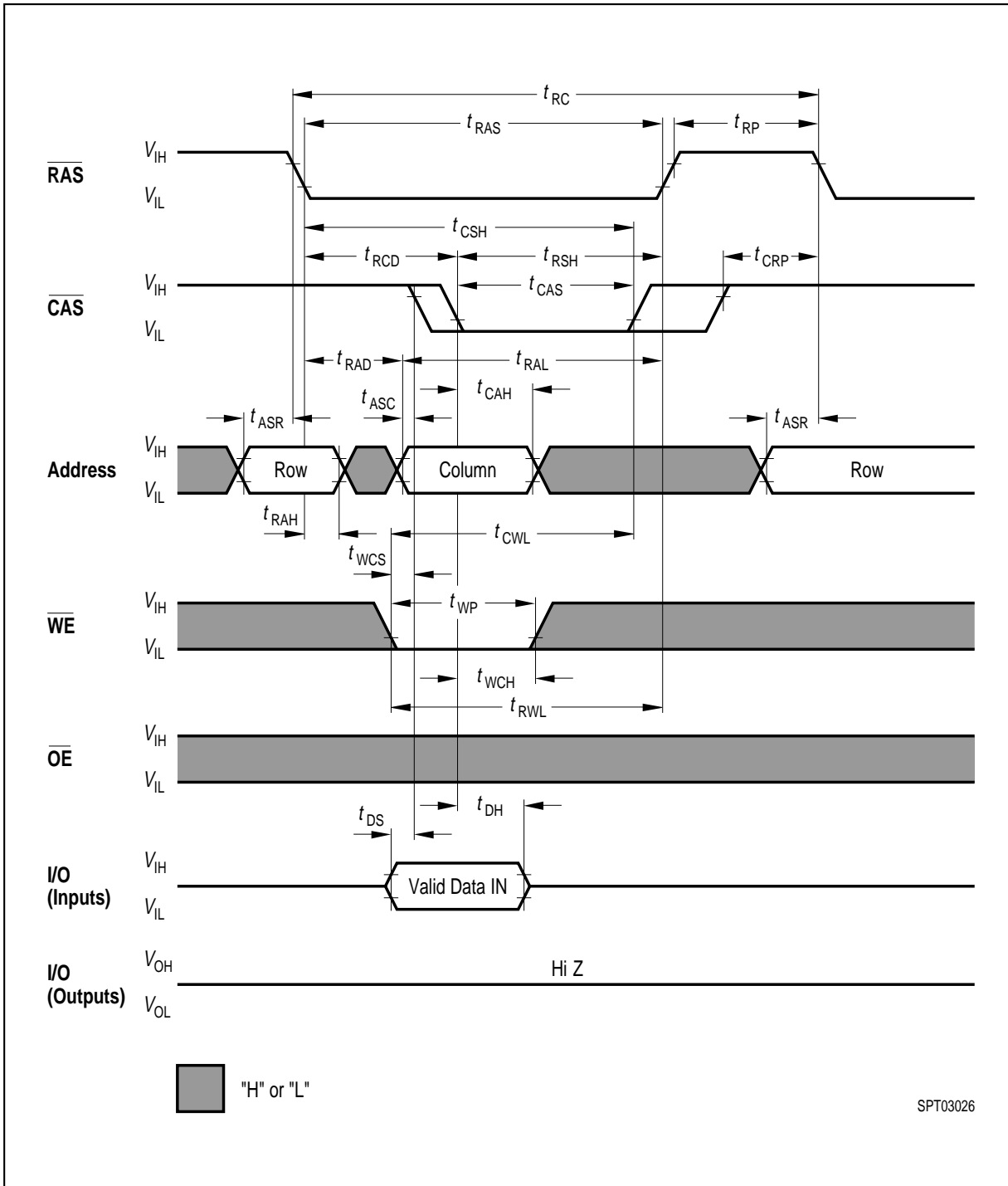


**Notes:**

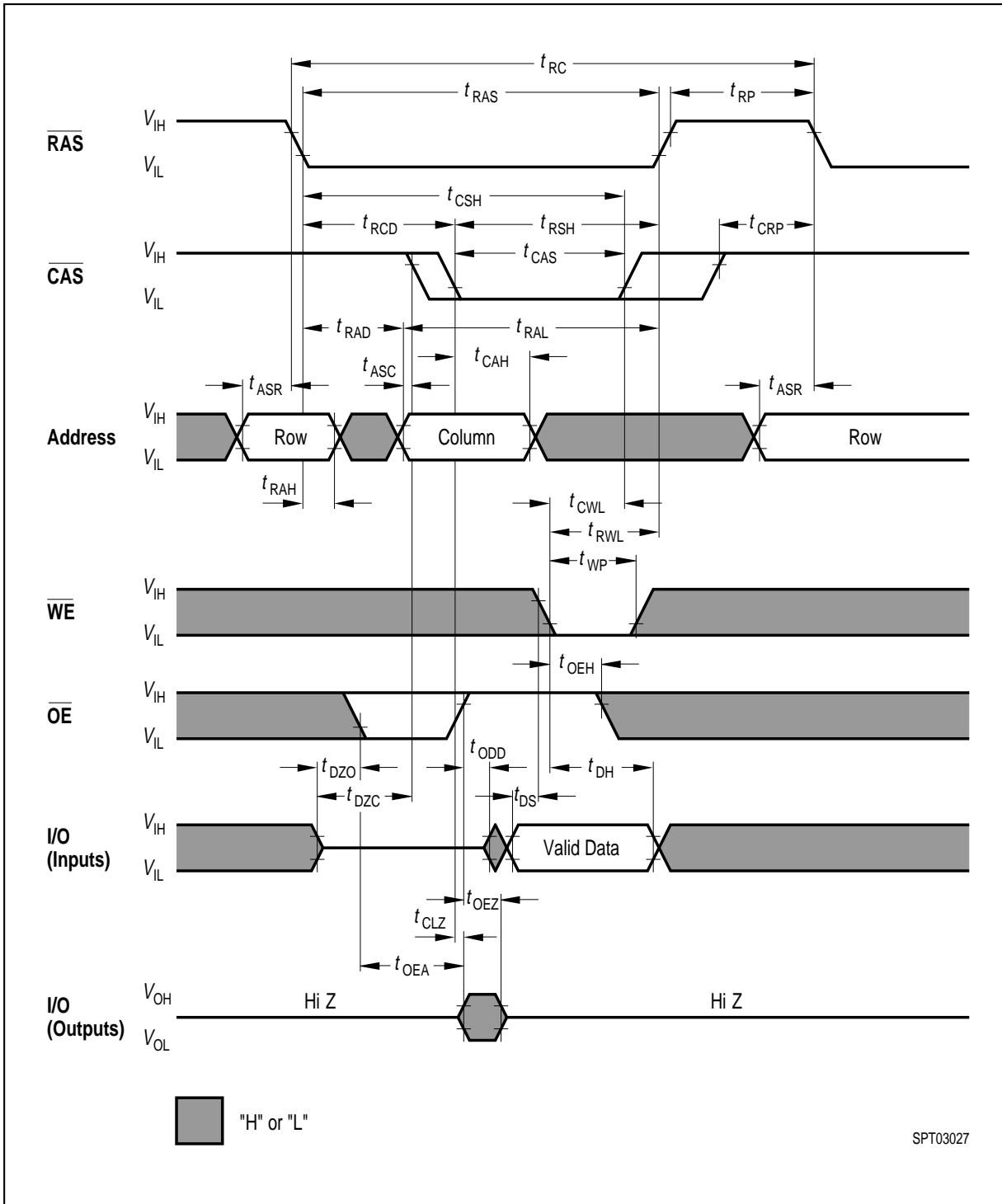
1. All voltages are referenced to  $V_{SS}$ .
2.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.
3.  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are measured with the output open.
4. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ . In the case of  $I_{CC4}$  it can be changed once or less during a fast page mode cycle ( $t_{PC}$ ).
5. An initial pause of 200  $\mu s$  is required after power-up followed by 8  $\overline{RAS}$  cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6. AC measurements assume  $t_T = 5$  ns.
7.  $V_{IH(MIN)}$  and  $V_{IL(MAX)}$  are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
8. Measured with a load equivalent to 2 TTL loads and 100 pF.
9. Operation within the  $t_{RCD(MAX)}$  limit ensures that  $t_{RAC(MAX)}$  can be met.  $t_{RCD(MAX)}$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD(MAX)}$  limit, then access time is controlled by  $t_{CAC}$ .
10. Operation within the  $t_{RAD(MAX)}$  limit ensures that  $t_{RAC(MAX)}$  can be met.  $t_{RAD(MAX)}$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD(MAX)}$  limit, then access time is controlled by  $t_{AA}$ .
11. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
12.  $t_{OFF(MAX)}$  and  $t_{OEZ(MAX)}$  define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
13. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
14. Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.
15.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} > t_{WCS(MIN)}$ , the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if  $t_{RWD} > t_{RWD(MIN)}$ ,  $t_{CWD} > t_{CWD(MIN)}$ ,  $t_{AWD} > t_{AWD(MIN)}$  and  $t_{CPWD} > t_{CPWD(MIN)}$ , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
16. These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles and to the  $\overline{WE}$  leading edge in read-write cycles.



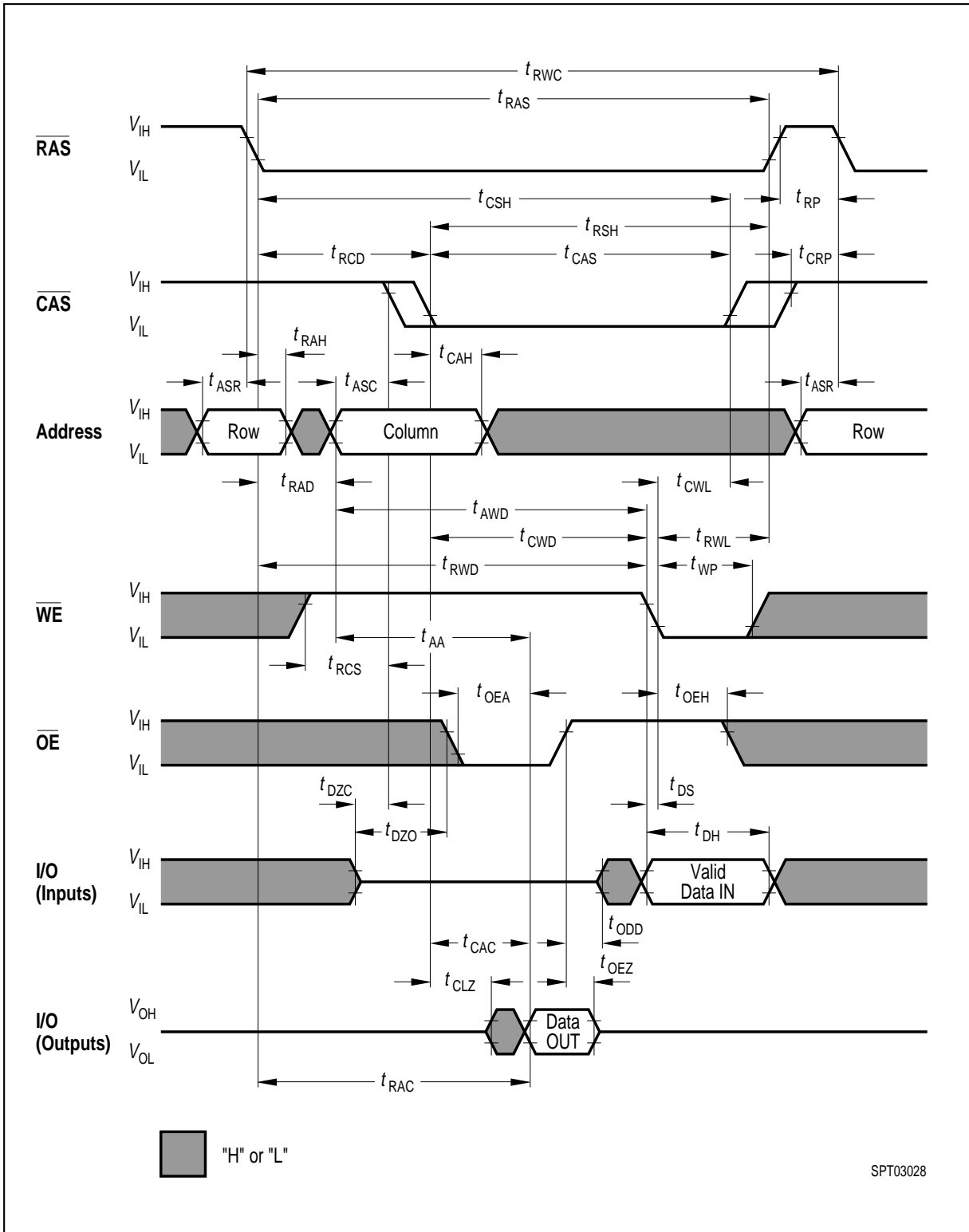
Read Cycle



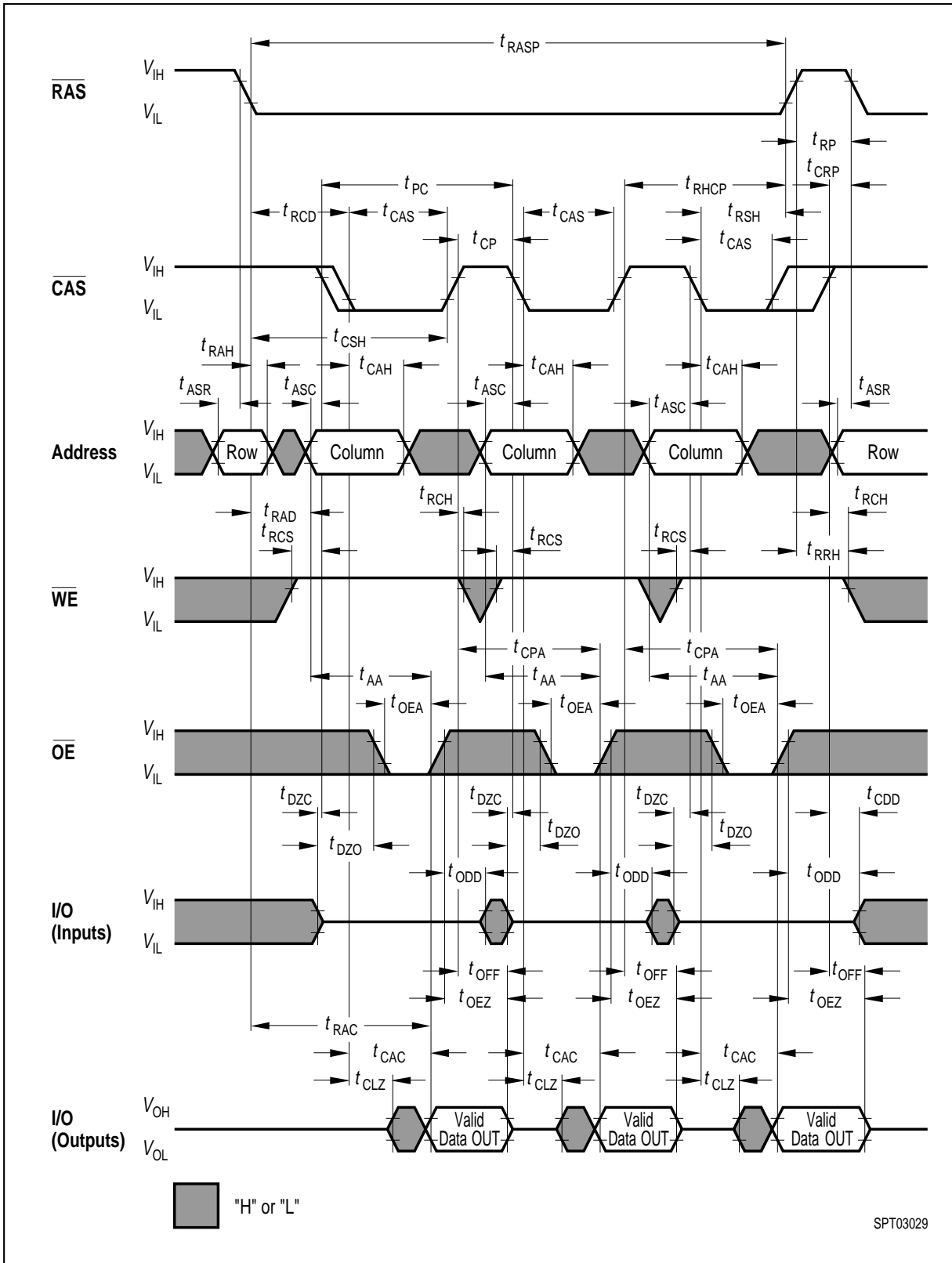
Write Cycle (Early Write)



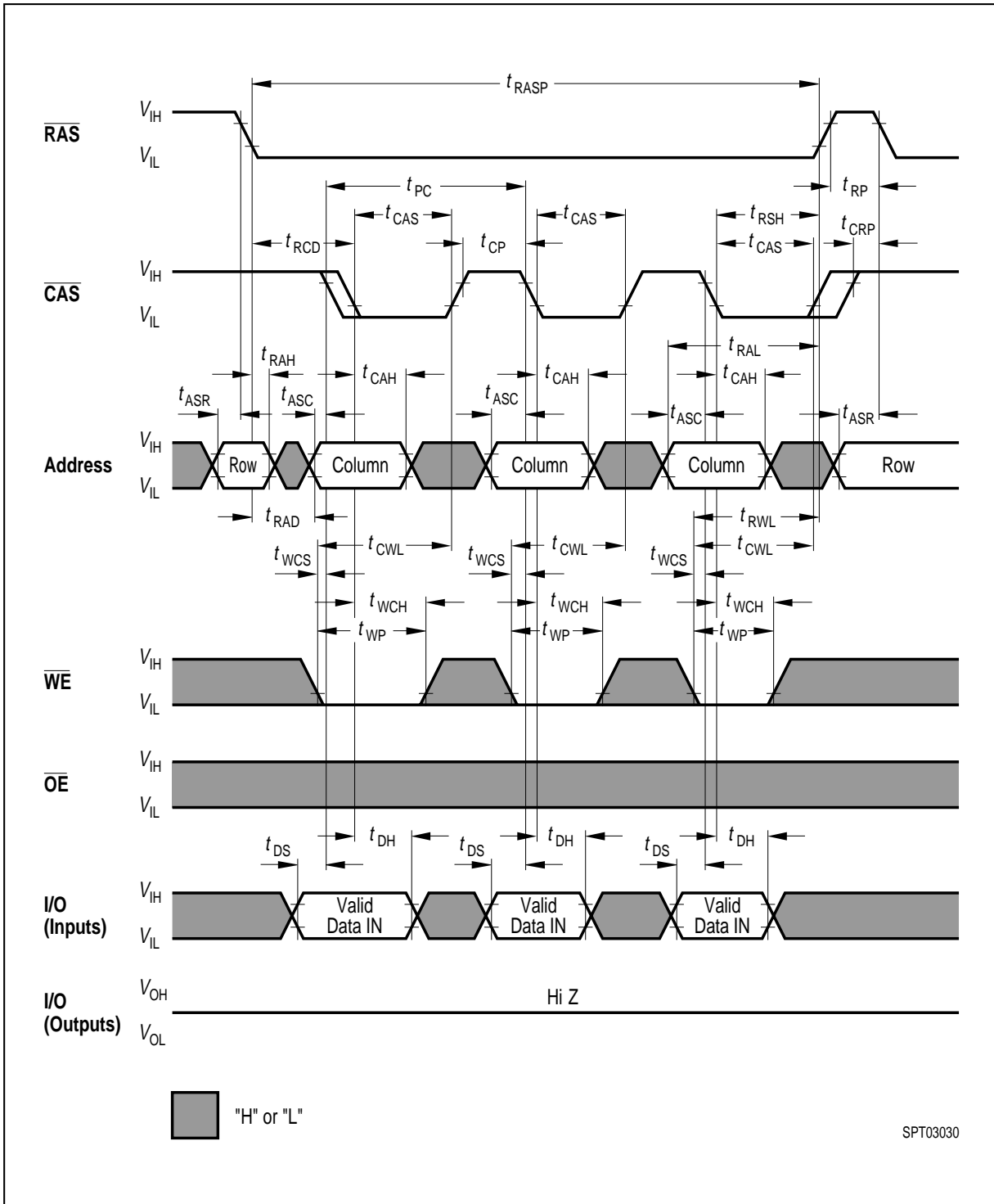
Write Cycle ( $\overline{OE}$  Controlled Write)



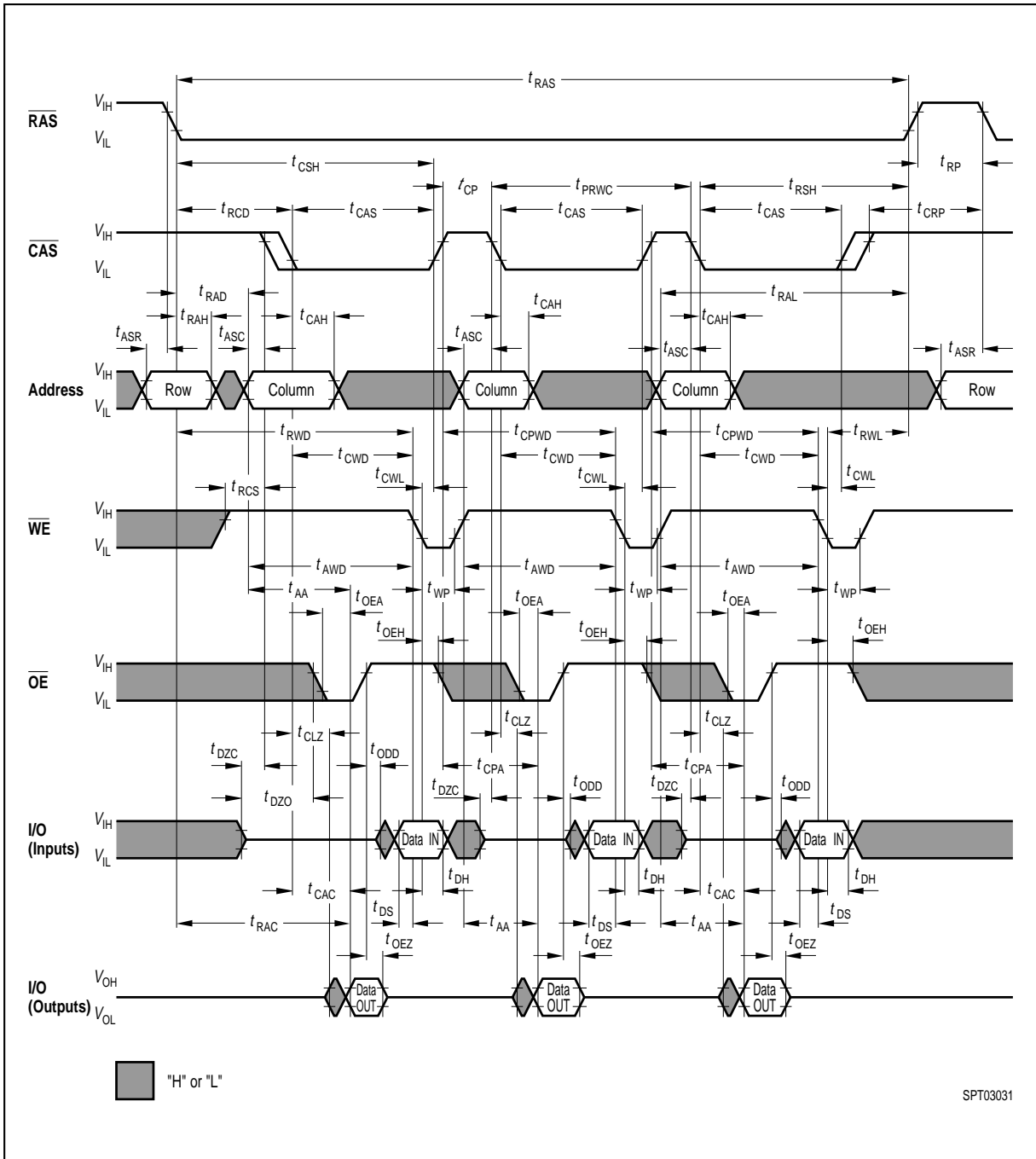
Read-Write (Read-Modify-Write) Cycle



Fast Page Mode Read Cycle

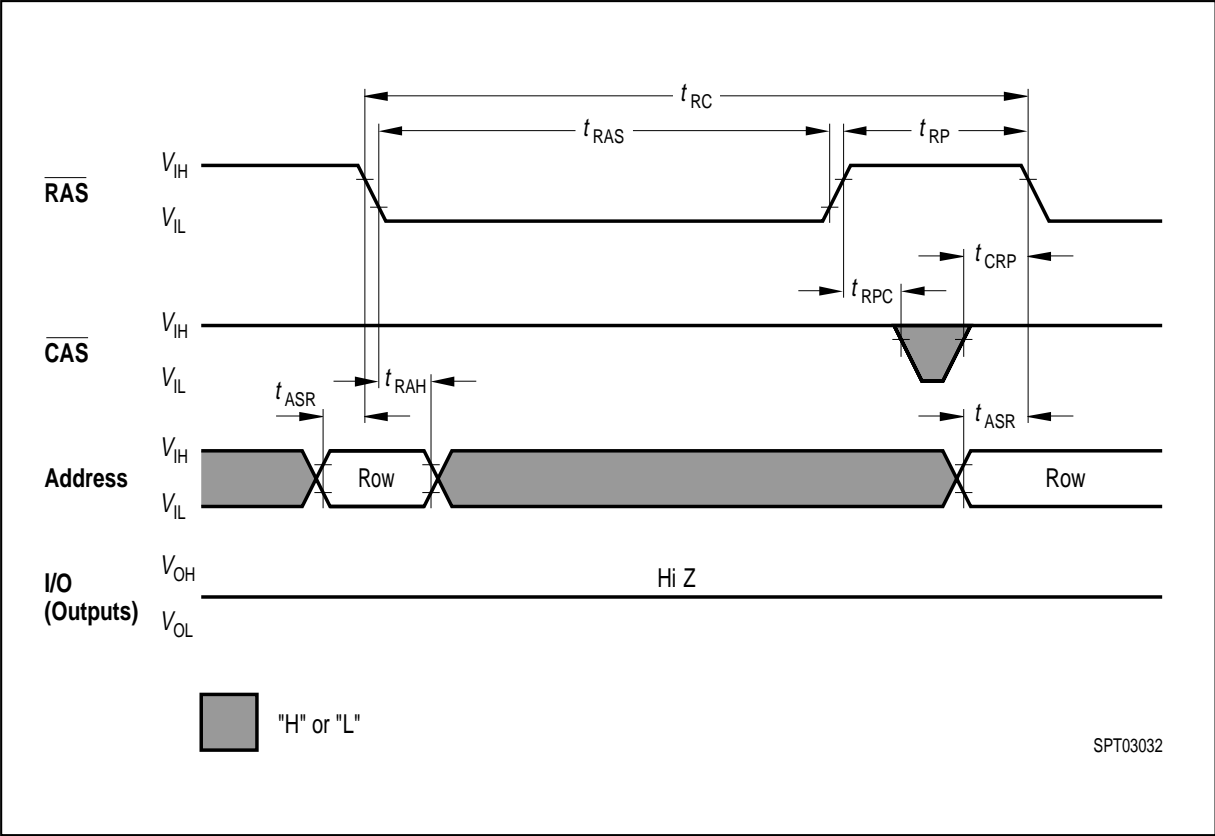


Fast Page Mode Early Write Cycle

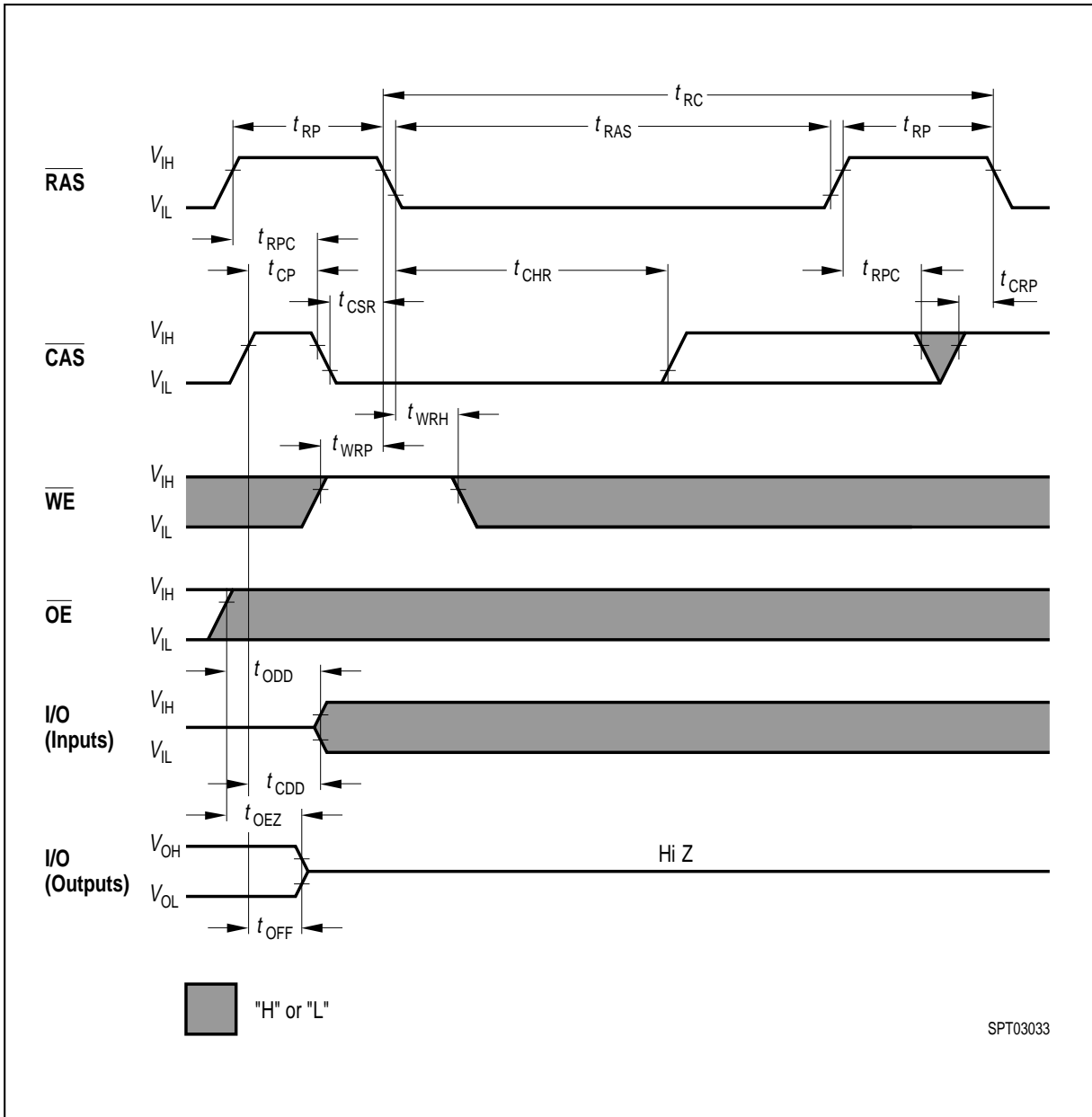


Fast Page Mode Read-Modify-Write Cycle

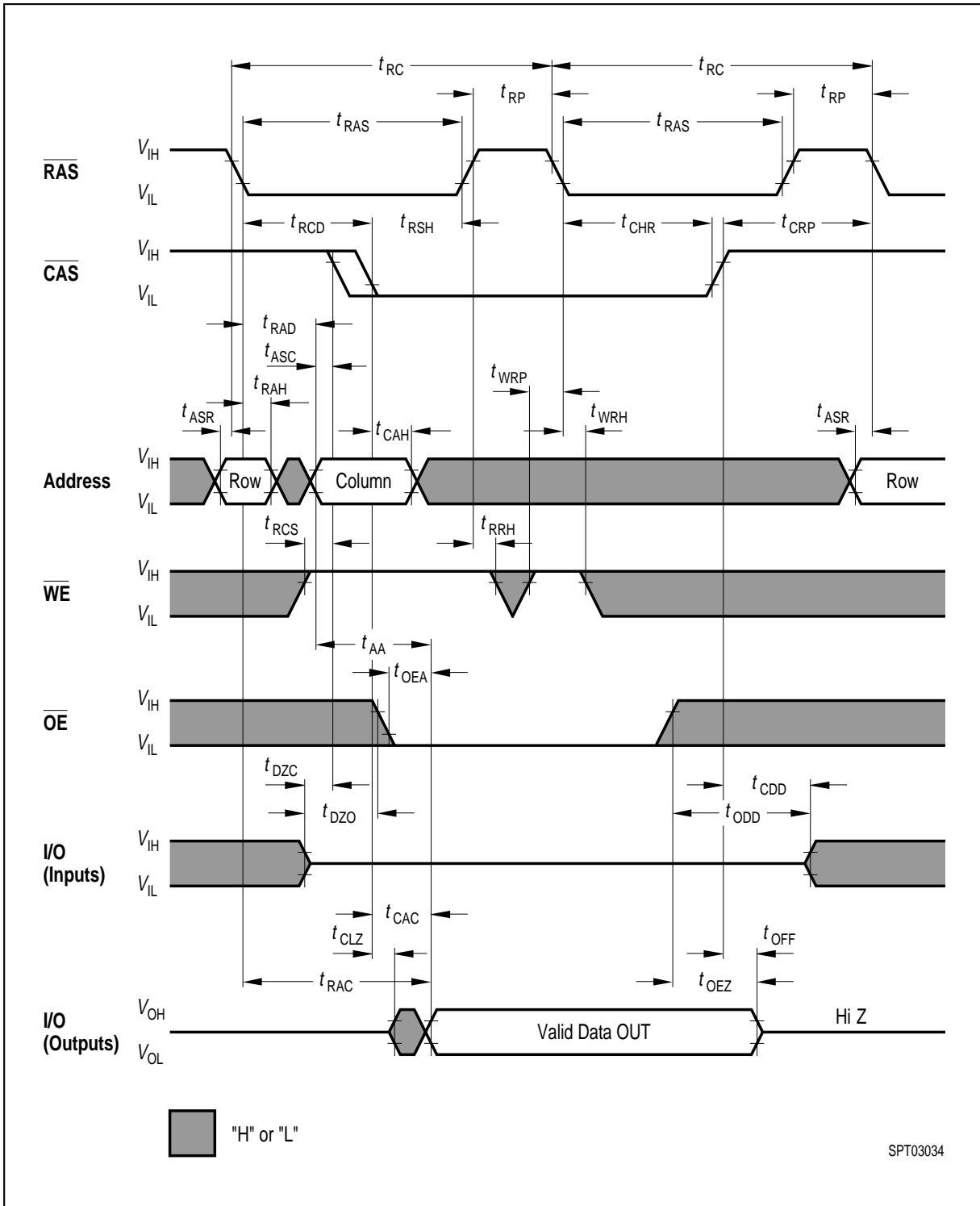




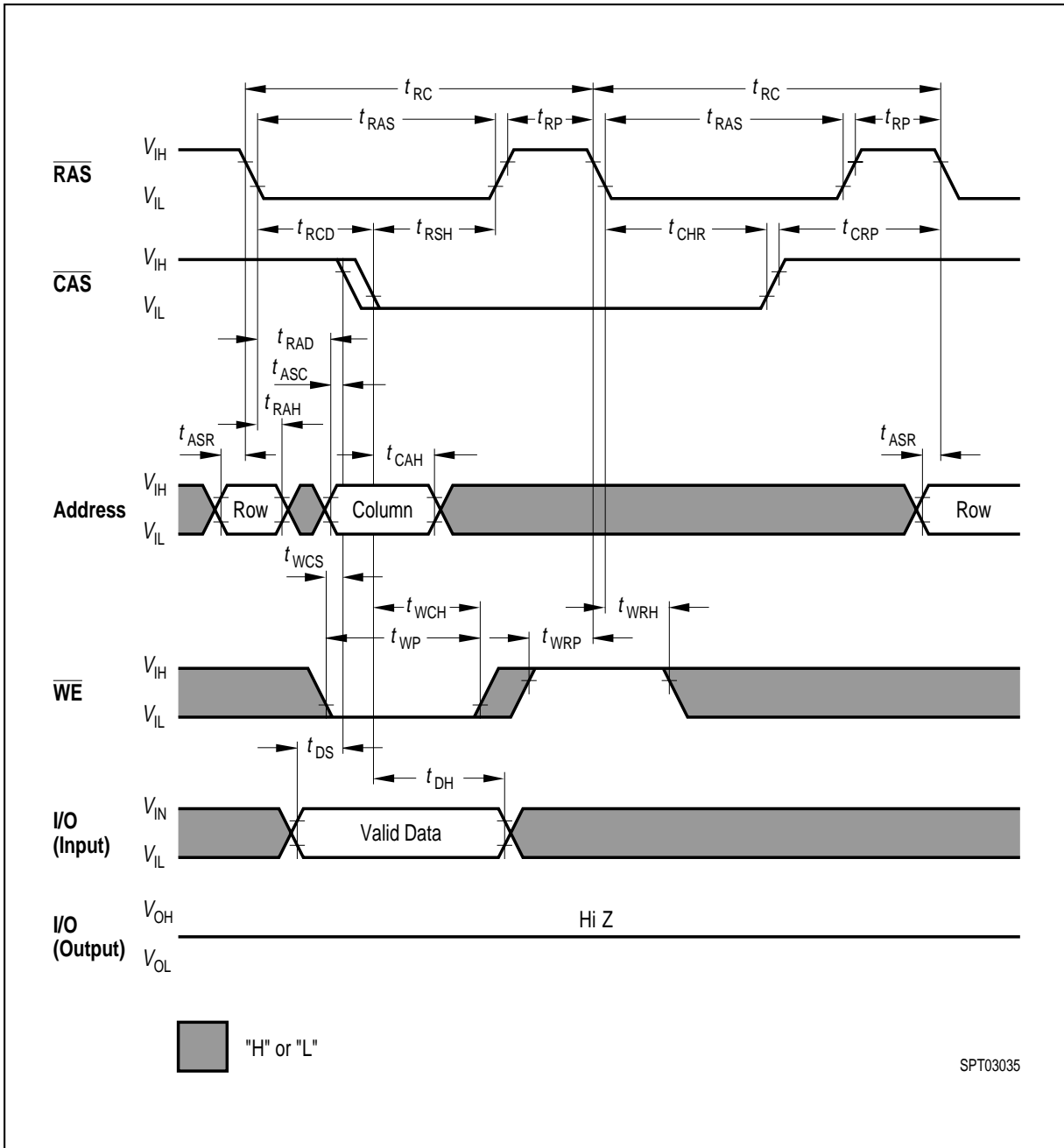
RAS-Only Refresh Cycle



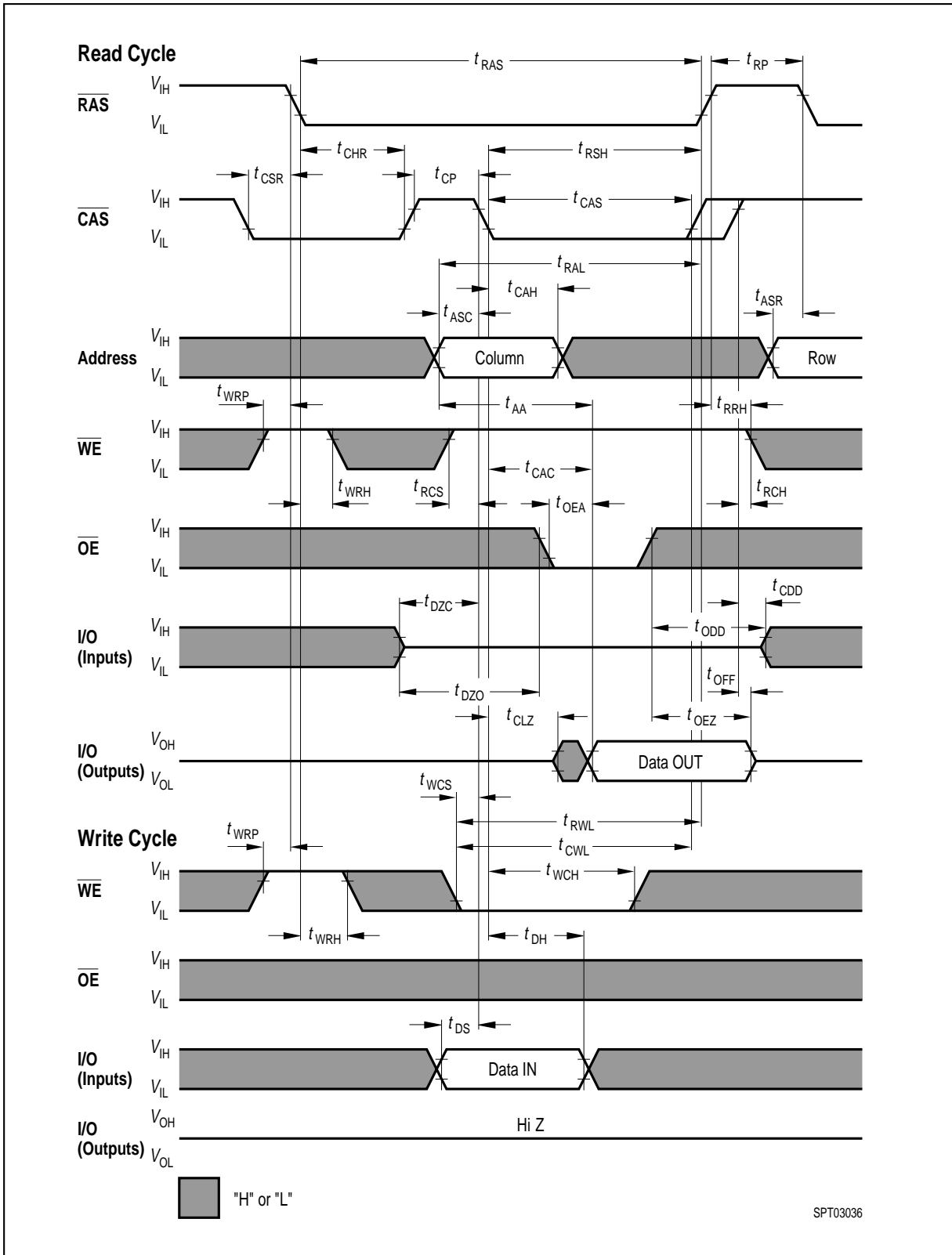
CAS-Before-RAS Refresh Cycle



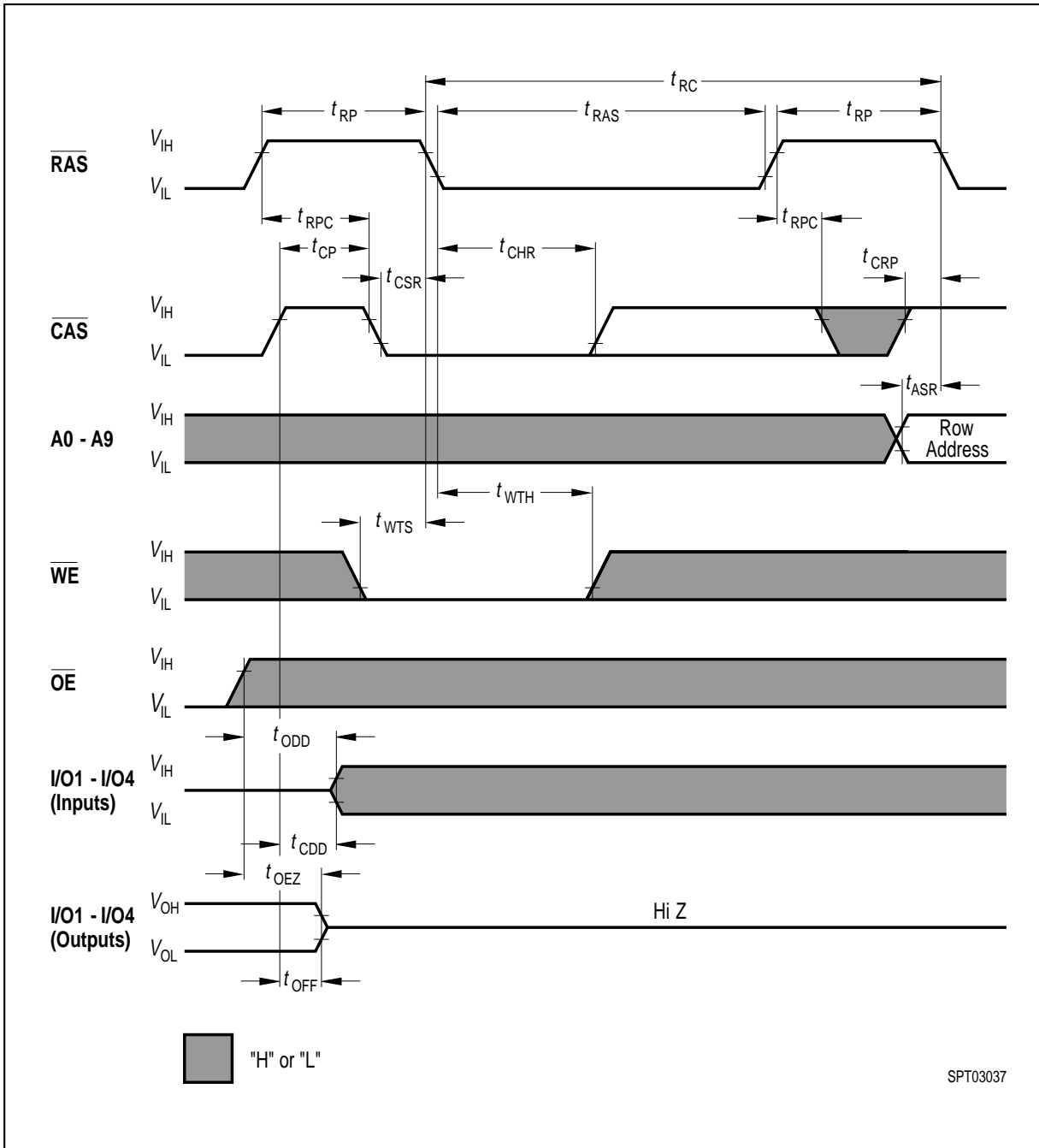
Hidden Refresh Cycle (Read)



**Hidden Refresh Cycle (Early Write)**



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

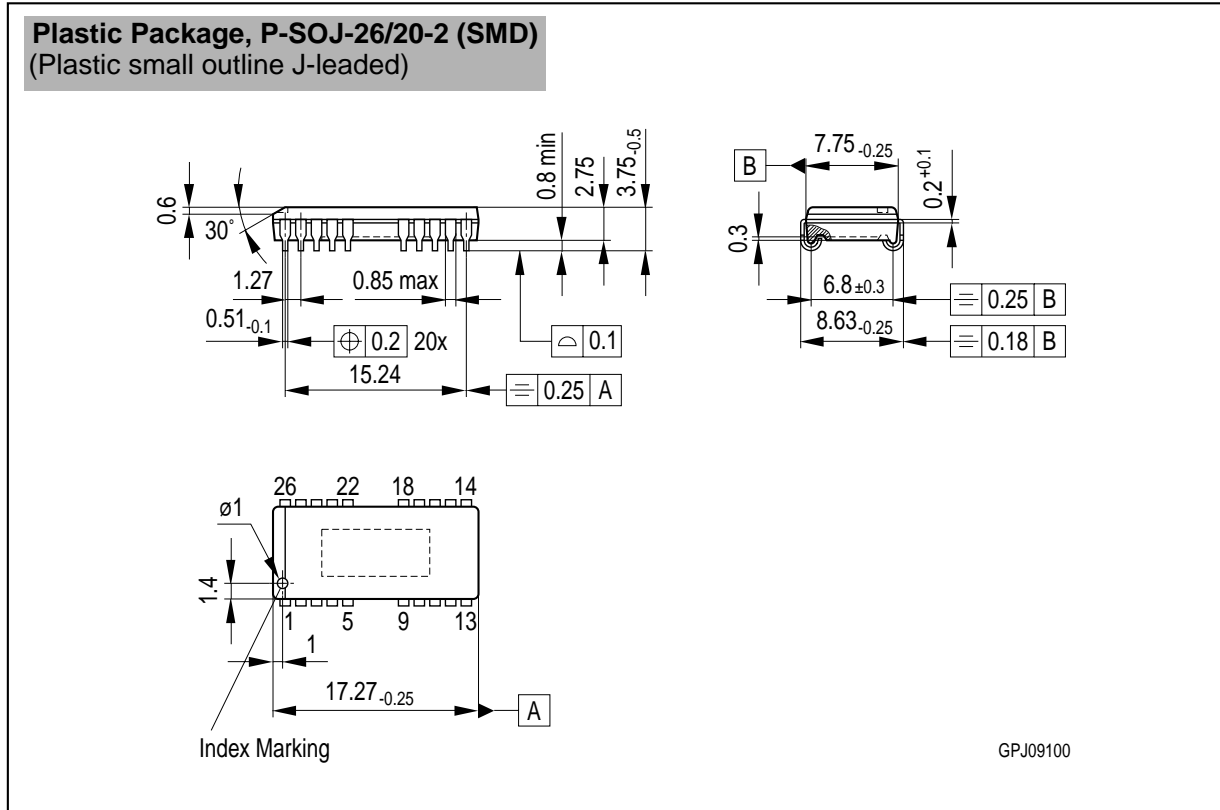
**Test Mode**

As the HYB 514400BJ is organized internally as 512k × 8-bits, a test mode cycle using 8:1 compression can be used to improve test time. Note that in the 1M × 4 version the test time is reduced by 1/2 for a linear test pattern.

In a test mode "write" the data from each I/O1 pin is written into eight bits simultaneously (all "1" or all "0"). The I/O2 - I/O4 inputs are not used for writing in test mode. In test mode "read" each I/O output is used for indicating the test mode result. If the internal eight bits are equal, the I/O would indicate a "1". If they were not equal, the I/O would indicate a "0". Note that in test mode „read“ I/O1-I/O3 are always driven to "ones", i.e. all outputs will be "1" for a test mode "pass". The WCBR cycle ( $\overline{WE}$ ,  $\overline{CAS}$ -before- $\overline{RAS}$ ) puts the device into test mode. To exit from test mode, a " $\overline{CAS}$ -before- $\overline{RAS}$  refresh", " $\overline{RAS}$ -only refresh" or "Hidden refresh" can be used.

Addresses A10R, A10C and A0C are don't care during test mode.

**Package Outlines**



**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm