

## 512Kx8 Static RAM Module

### Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**  
— Access time of 20 ns
- **Low active power**  
— 1.93W (max.)
- **JEDEC-compatible pinout**
- **32-pin, 0.6-inch-wide DIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**  
— Max. height of 0.34 inches

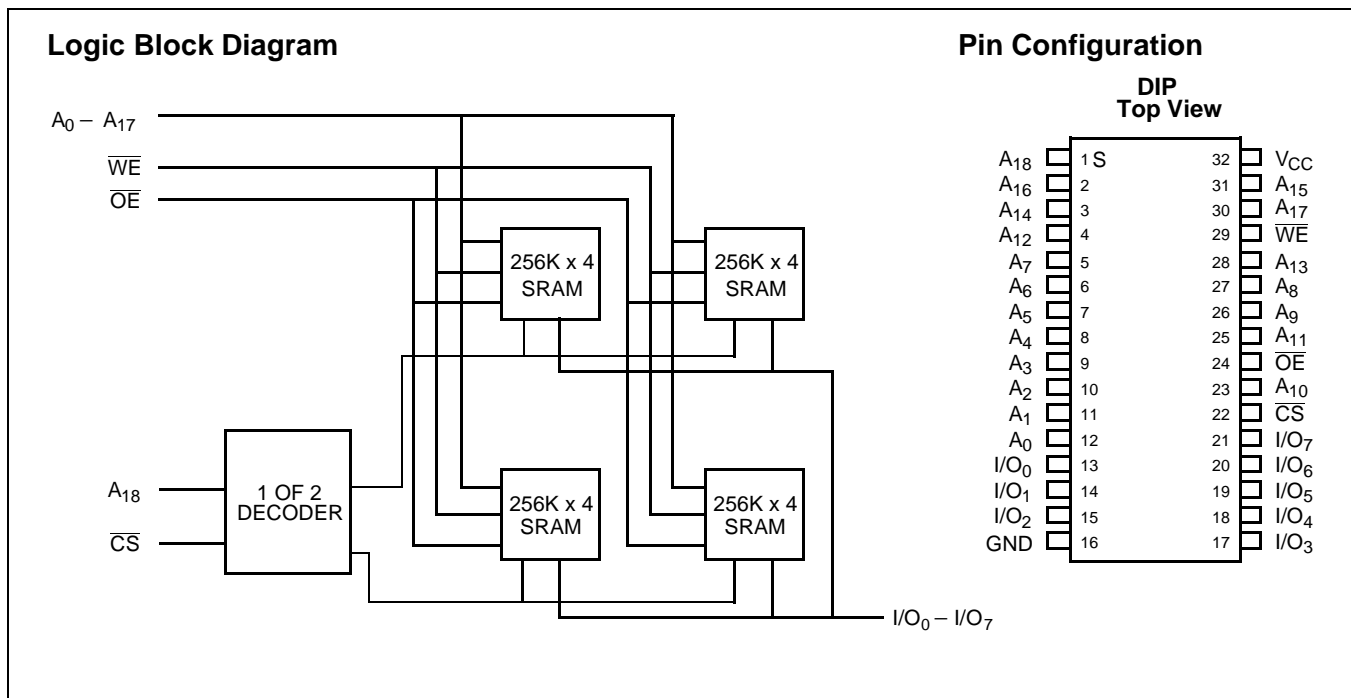
### Functional Description

The CYM1464 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is

constructed using four 256K x 4 static RAMs in SOJ packages mounted on an epoxy laminate substrate with pins.

Writing to the module is accomplished when the chip select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the eight input/output pins ( $I/O_0$  through  $I/O_7$ ) of the device is written into the memory location specified on the address pins ( $A_0$  through  $A_{18}$ ). Reading the device is accomplished by taking chip select and output enable ( $\overline{OE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins ( $A_0$  through  $A_{18}$ ) will appear on the eight appropriate data input/output pins ( $I/O_0$  through  $I/O_7$ ).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.



### Selection Guide

	1464-20	1464-22	1464-25	1464-30	1464-35	1464-45	1464-55
Maximum Access Time (ns)	20	22	25	30	35	45	55
Maximum Operating Current (mA)	350	350		300		300	
Maximum Standby Current (mA)	240	240		240		240	

### Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... -55°C to +125°C  
 Ambient Temperature with  
 Power Applied..... -10°C to +85°C  
 Supply Voltage to Ground Potential ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V  
 DC Input Voltage ..... -0.5V to +7.0V

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%

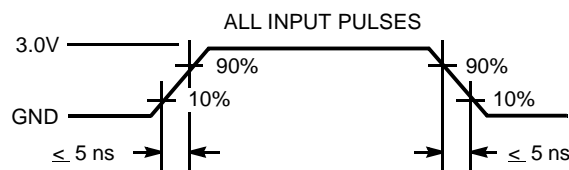
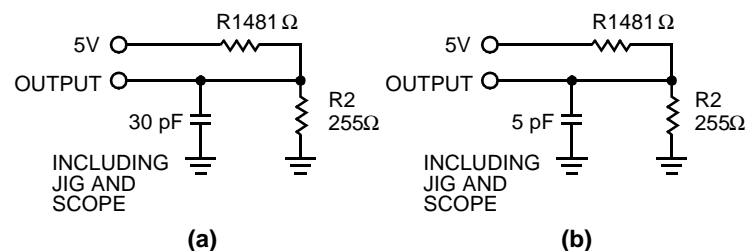
### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1464-20, 22, 25		1464-30, 35, 45, 55		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> +0.3	2.2	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-10	+10	-10	+10	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, CS ≤ V <sub>IL</sub>		350		300	mA
I <sub>SB1</sub>	Automatic CS Power-Down Current	V <sub>CC</sub> = Max., CS ≥ V <sub>IH</sub> , Min. Duty Cycle = 100%		240		240	mA
I <sub>SB2</sub>	Automatic CS Power-Down Current	V <sub>CC</sub> = Max., CS ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V		60		60	mA

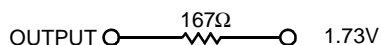
### Capacitance<sup>[2]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	40	pF
C <sub>OUT</sub>	Output Capacitance		30	pF

### AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



#### Notes:

- V<sub>IL</sub> (min.) = -3.0V for pulse widths less than 20 ns.
- Tested on a sample basis.

**Switching Characteristics** Over the Operating Range<sup>[3]</sup>

Parameter	Description	1464-20		1464-22		1464-25		1464-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
t <sub>RC</sub>	Read Cycle Time	20		22		25		30		ns
t <sub>AA</sub>	Address to Data Valid		20		22		25		30	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		5		5		5		ns
t <sub>ACS</sub>	$\overline{\text{CS}}$ LOW to Data Valid		20		22		25		30	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid		13		13		15		15	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to Low Z	0		0		0		0		ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High Z	0	10	0	10	0	10	0	10	ns
t <sub>LZCS</sub>	$\overline{\text{CS}}$ LOW to Low Z	5		5		5		10		ns
t <sub>HZCS</sub>	$\overline{\text{CS}}$ HIGH to High Z <sup>[4]</sup>	0	15	0	15	0	15	0	20	ns
<b>WRITE CYCLE<sup>[5]</sup></b>										
t <sub>WC</sub>	Write Cycle Time	20		22		25		30		ns
t <sub>SCS</sub>	$\overline{\text{CS}}$ LOW to Write End	15		17		20		25		ns
t <sub>AW</sub>	Address Set-Up to Write End	15		15		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	3		3		3		3		ns
t <sub>SA</sub>	Address Set-Up to Write Start	5		5		5		5		ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	15		15		15		20		ns
t <sub>SD</sub>	Data Set-Up to Write End	12		12		15		15		ns
t <sub>HD</sub>	Data Hold from Write End	2		2		2		2		ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low Z	0		0		0		0		ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High Z <sup>[4]</sup>		15		15		15		15	ns

**Switching Characteristics** Over the Operating Range <sup>[3]</sup>

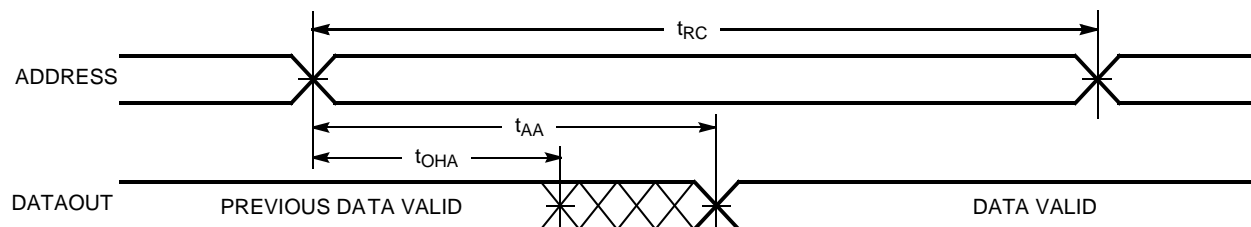
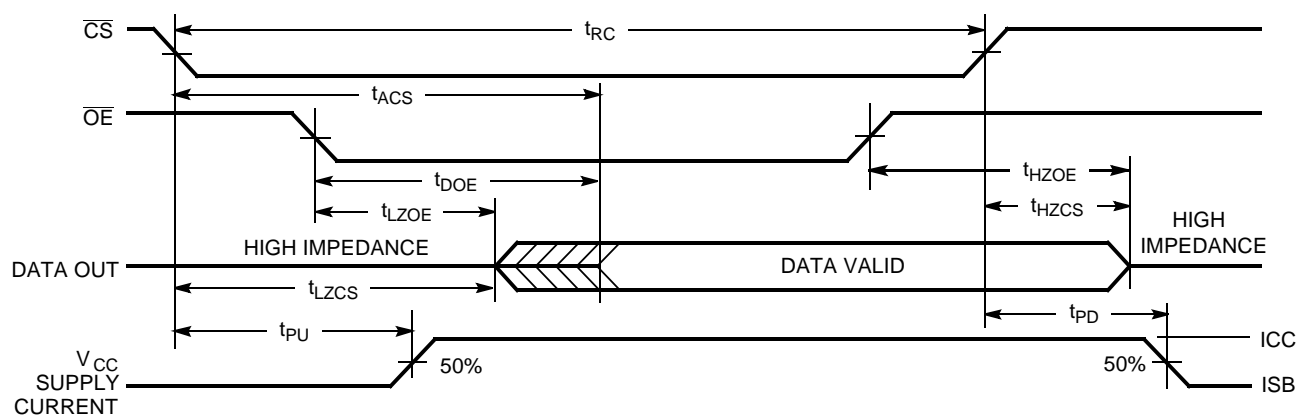
Parameter	Description	1464-35		1464-45		1464-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	35		45		55		ns
t <sub>AA</sub>	Address to Data Valid		35		45		55	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		5		5		ns
t <sub>ACS</sub>	$\overline{\text{CS}}$ LOW to Data Valid		35		45		55	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid		20		25		30	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to Low Z	0		0		0		ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High Z	0	15	0	15	0	15	ns
t <sub>LZCS</sub>	$\overline{\text{CS}}$ LOW to Low Z	10		10		10		ns
t <sub>HZCS</sub>	$\overline{\text{CS}}$ HIGH to High Z <sup>[4]</sup>	0	20	0	20	0	20	ns

**Notes:**

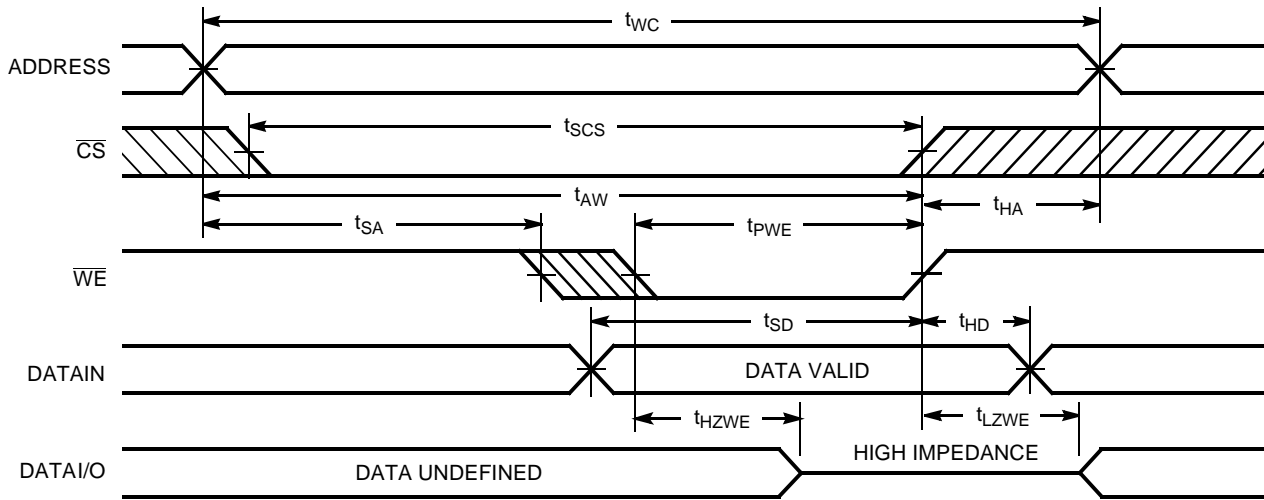
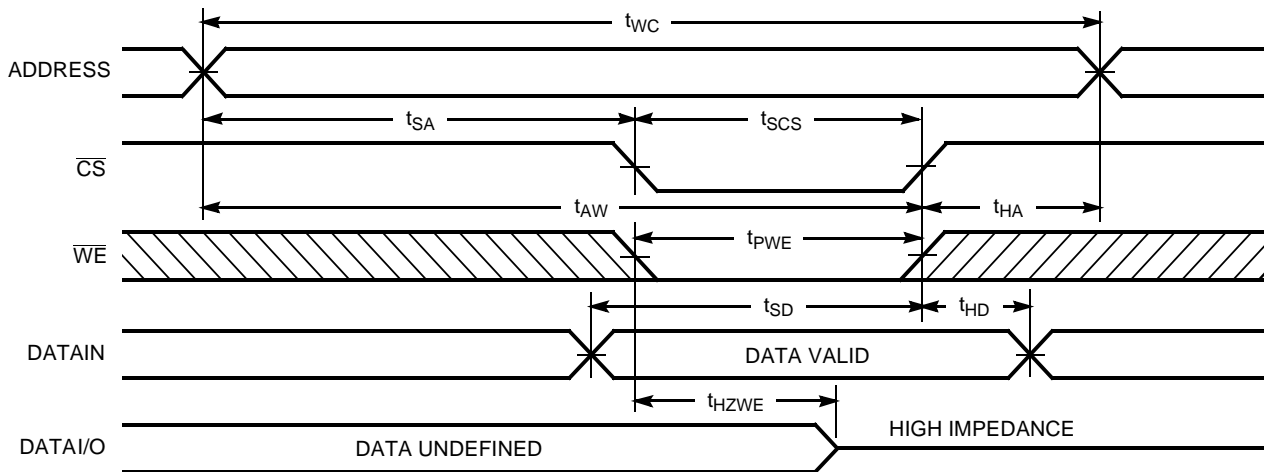
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CS}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

**Switching Characteristics** Over the Operating Range (continued)<sup>[3]</sup>

Parameter	Description	1464-35		1464-45		1464-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE<sup>[5]</sup></b>								
$t_{WC}$	Write Cycle Time	35		45		55		ns
$t_{SCS}$	$\overline{CS}$ LOW to Write End	30		40		50		ns
$t_{AW}$	Address Set-Up to Write End	30		40		50		ns
$t_{HA}$	Address Hold from Write End	3		3		3		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	25		35		40		ns
$t_{SD}$	Data Set-Up to Write End	20		25		35		ns
$t_{HD}$	Data Hold from Write End	2		3		3		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[4]</sup>		15		15		20	ns

**Switching Waveforms**
**Read Cycle No. 1<sup>[6,7]</sup>**

**Read Cycle No. 2<sup>[6,8]</sup>**

**Notes:**

6.  $\overline{WE}$  is HIGH for read cycle.
7. Device is continuously selected,  $\overline{CS} = V_{LL}$ .
8. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[5]</sup>**

**Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[5,9]</sup>**

**Note:**

9. If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Truth Table**

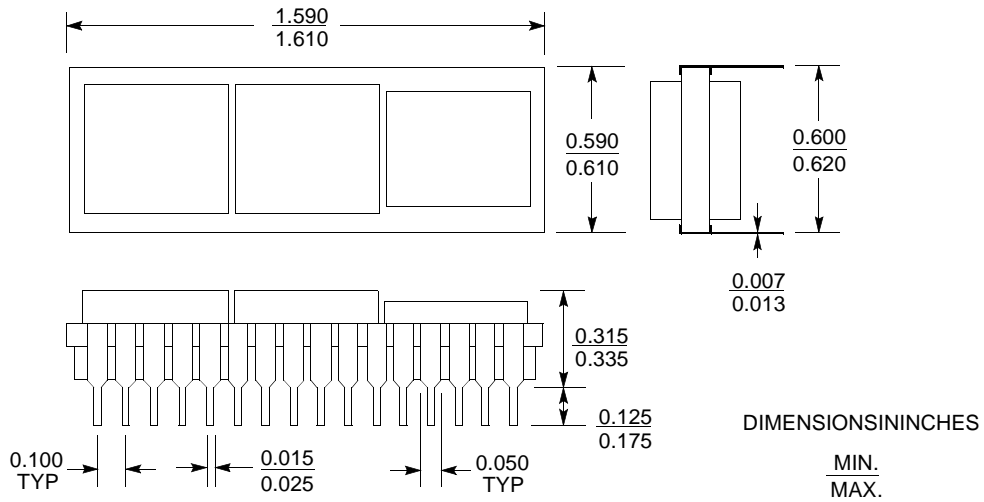
CS	WE	OE	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

**Ordering Information**

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CYM1464PD-20C	PD02	32-Pin DIP Module	Commercial
22	CYM1464PD-22C	PD02	32-Pin DIP Module	Commercial
25	CYM1464PD-25C	PD02	32-Pin DIP Module	Commercial
30	CYM1464PD-30C	PD02	32-Pin DIP Module	Commercial
35	CYM1464PD-35C	PD02	32-Pin DIP Module	Commercial
45	CYM1464PD-45C	PD02	32-Pin DIP Module	Commercial
55	CYM1464PD-55C	PD02	32-Pin DIP Module	Commercial

Package Diagrams

32-Pin DIP Module PD02



<b>Document Title: CYM1464 512K x 8 Static RAM Module</b> <b>Document Number: 38-05272</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	114173	3/19/02	DSG	Change from Spec number: 38-M-00030 to 38-05272