



# CYM1846

## 512K x 32 Static RAM Module

### Features

- High-density 16-megabit SRAM module
- 32-bit standard footprint supports from 16Kx32 through 1Mx32
- High-speed SRAMs
  - Access time of 12 ns
- Low active power
  - 4.4W (max.) at 12 ns
- Compatible with CYM1821, CYM1831, CYM1836, CYM1841, and CYM1851 JEDEC modules
- Available in 72-pin ZIP or SIMM/Angled SIMM

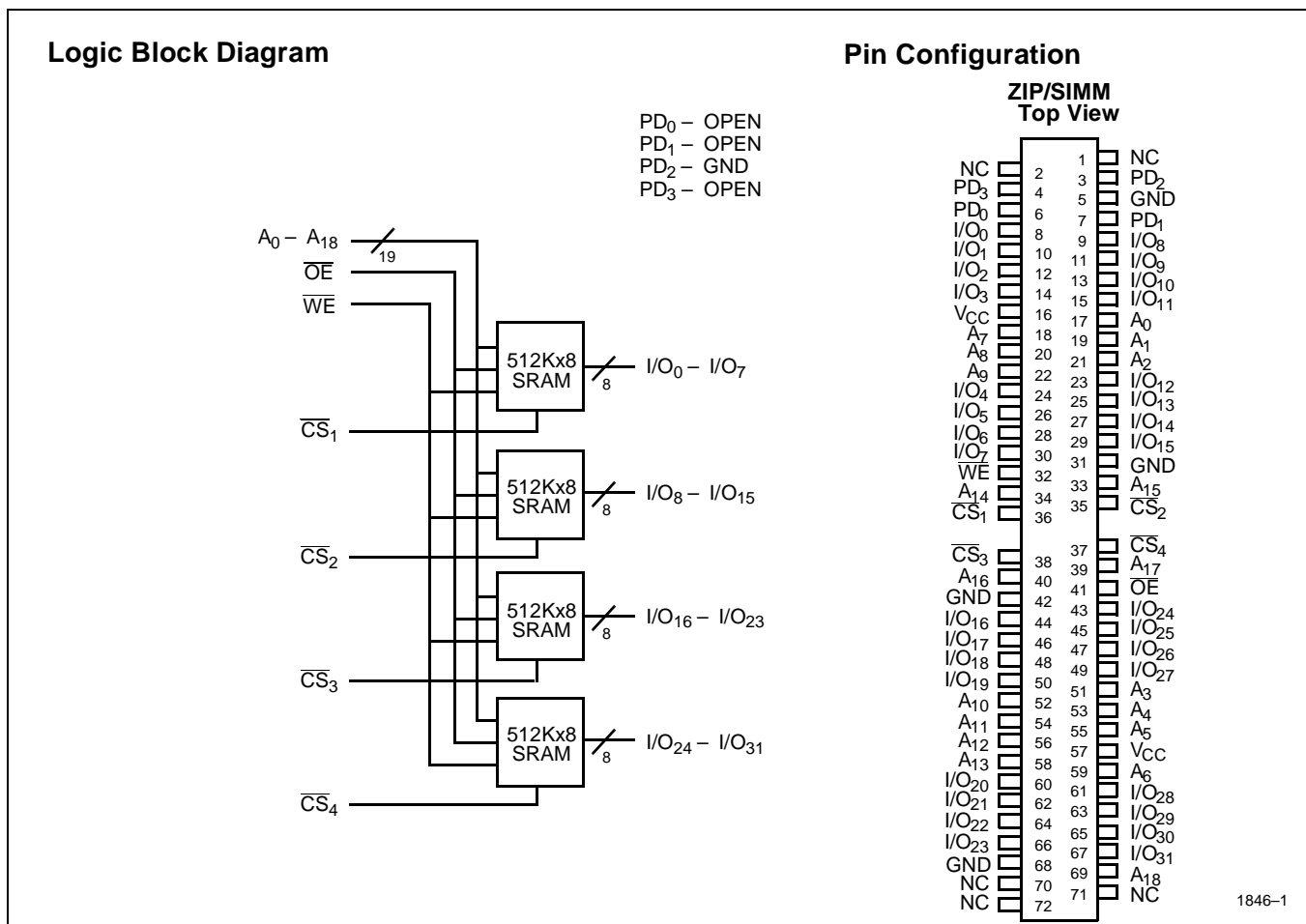
### Functional Description

The CYM1846 is a high-performance 16-megabit static RAM module organized as 512K words by 32 bits. This module is

constructed from four 512K x 8 SRAMs in SOJ packages mounted on an epoxy laminate substrate. Four chip selects are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of the chip selects.

The CYM1846 is designed for use with standard 72-pin SIMM socket and ZIP footprint. The pinout is compatible with the 64-pin JEDEC ZIP/SIMM module family (CYM1821, CYM1831, CYM1836, and CYM1841) and the 72-pin CYM1851. Thus, a single motherboard design can be used to accommodate memory depth ranging from 16K words (CYM1821) to 1024K words (CYM1851). The standard SIMM can be used in Angled SIMM sockets and is available with either tin-lead or 10 micro-inches of gold flash on the edge contacts.

Presence detect pins (PD<sub>0</sub> – PD<sub>3</sub>) are used to identify module memory density in applications where modules with alternate word depths can be interchanged.



**Selection Guide**

	1846-12	1846-15	1846-20	1846-25	1846-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	800	800	800	800	800
Maximum Standby Current (mA)	240	240	240	240	240

Shaded area contains preliminary information.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -55°C to +125°C

Ambient Temperature with Power Applied ..... -10°C to +85°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... -0.5V to +V<sub>CC</sub>

DC Input Voltage ..... -0.5V to +7.0V

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

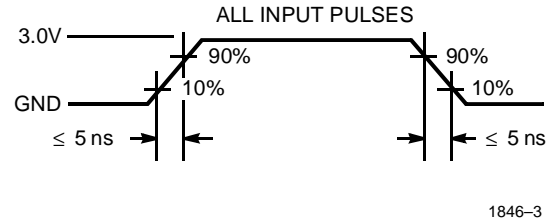
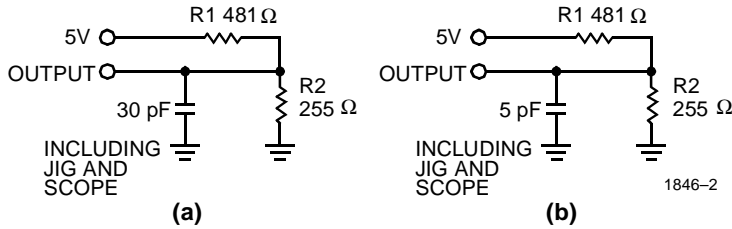
Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-10	+10	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, $\overline{CS}_N \leq V_{IL}$		800	mA
I <sub>SB1</sub>	Automatic $\overline{CS}$ Power-Down Current <sup>[1]</sup>	Max. V <sub>CC</sub> , $\overline{CS} \geq V_{IH}$ , Min. Duty Cycle = 100%		240	mA
I <sub>SB2</sub>	Automatic $\overline{CS}$ Power-Down Current <sup>[1]</sup>	Max. V <sub>CC</sub> , $\overline{CS} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V	-20, -25, 35	40	mA
			-12, -15	120	mA

**Capacitance<sup>[2]</sup>**

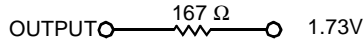
Parameter	Description	Test Conditions	Max.	Unit
C <sub>INA</sub>	Input Capacitance ( $\overline{WE}$ , $\overline{OE}$ , A <sub>0-18</sub> )	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	40	pF
C <sub>INB</sub>	Input Capacitance ( $\overline{CS}$ )		20	pF
C <sub>OUT</sub>	Output Capacitance		20	pF

**Note:**

1. A pull-up resistor to V<sub>CC</sub> on the  $\overline{CS}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
2. Tested on a sample basis.

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT


**Switching Characteristics** Over the Operating Range<sup>[3]</sup>

Parameter	Description	1846-12		1846-15		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	12		15		ns
$t_{AA}$	Address to Data Valid		12		15	ns
$t_{OHA}$	Data Hold from Address Change	3		3		ns
$t_{ACS}$	$\overline{CS}$ LOW to Data Valid		12		15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		7		8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z		7		8	ns
$t_{LZCS}$	$\overline{CS}$ LOW to Low Z <sup>[4]</sup>	3		3		ns
$t_{HZCS}$	$\overline{CS}$ HIGH to High Z <sup>[4, 5]</sup>		7		8	ns
$t_{PD}$	$\overline{CS}$ HIGH to Power-Down		12		15	ns
<b>WRITE CYCLE<sup>[6]</sup></b>						
$t_{WC}$	Write Cycle Time	12		15		ns
$t_{SCS}$	$\overline{CS}$ LOW to Write End	9		10		ns
$t_{AW}$	Address Set-Up to Write End	9		10		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	1		1		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10		12		ns
$t_{SD}$	Data Set-Up to Write End	7		8		ns
$t_{HD}$	Data Hold from Write End	1		1		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z	3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[5]</sup>	0	7	0	8	ns

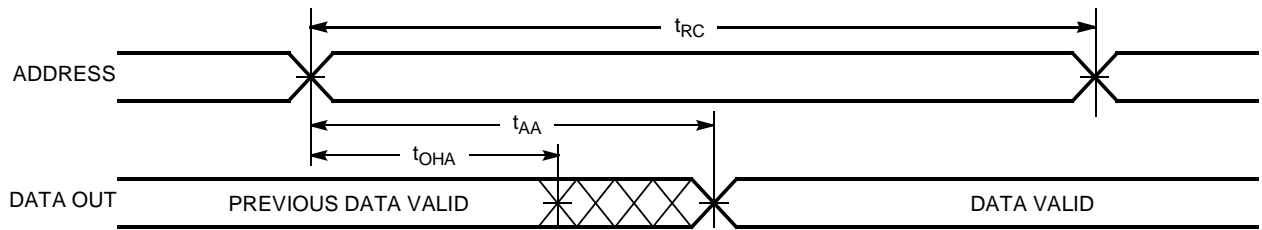
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**Switching Characteristics** Over the Operating Range<sup>[3]</sup> (continued)

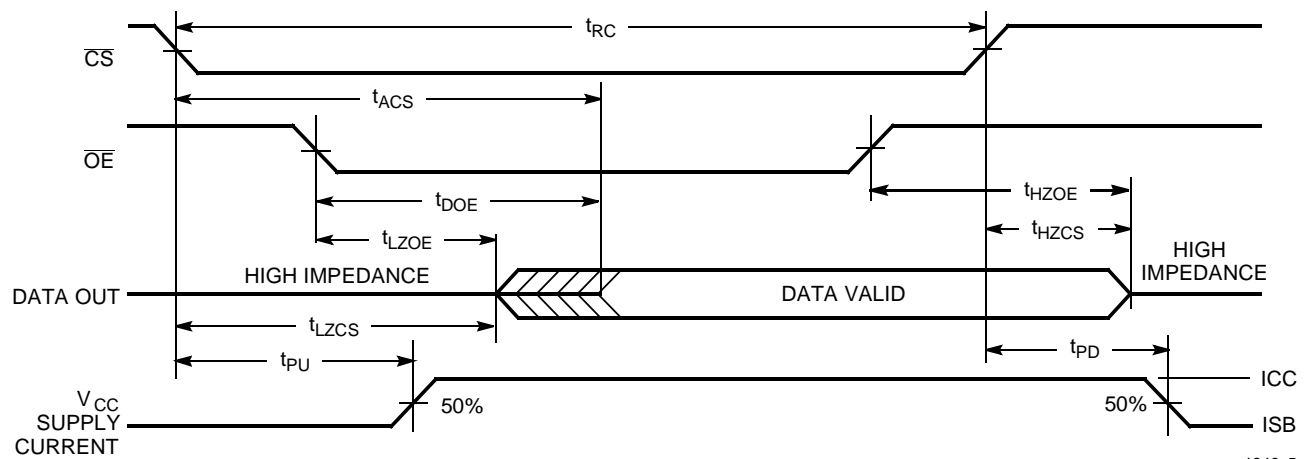
Parameter	Description	1846–20		1846–25		1846–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	20		25		35		ns
t <sub>AA</sub>	Address to Data Valid		20		25		35	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		ns
t <sub>ACS</sub>	$\overline{CS}$ LOW to Data Valid		20		25		35	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		10		15		25	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z		10		12		12	ns
t <sub>LZCS</sub>	$\overline{CS}$ LOW to Low Z <sup>[4]</sup>	3		3		3		ns
t <sub>HZCS</sub>	$\overline{CS}$ HIGH to High Z <sup>[4, 5]</sup>		10		12		12	ns
t <sub>PD</sub>	$\overline{CS}$ HIGH to Power-Down		20		25		35	ns
<b>WRITE CYCLE<sup>[6]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	20		25		35		ns
t <sub>SCS</sub>	$\overline{CS}$ LOW to Write End	15		20		30		ns
t <sub>AW</sub>	Address Set-Up to Write End	15		20		30		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	1		2		2		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	15		20		30		ns
t <sub>SD</sub>	Data Set-Up to Write End	10		15		20		ns
t <sub>HD</sub>	Data Hold from Write End	1		2		2		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z	3		4		5		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6]</sup>	0	10	0	12	0	12	ns

**Notes:**

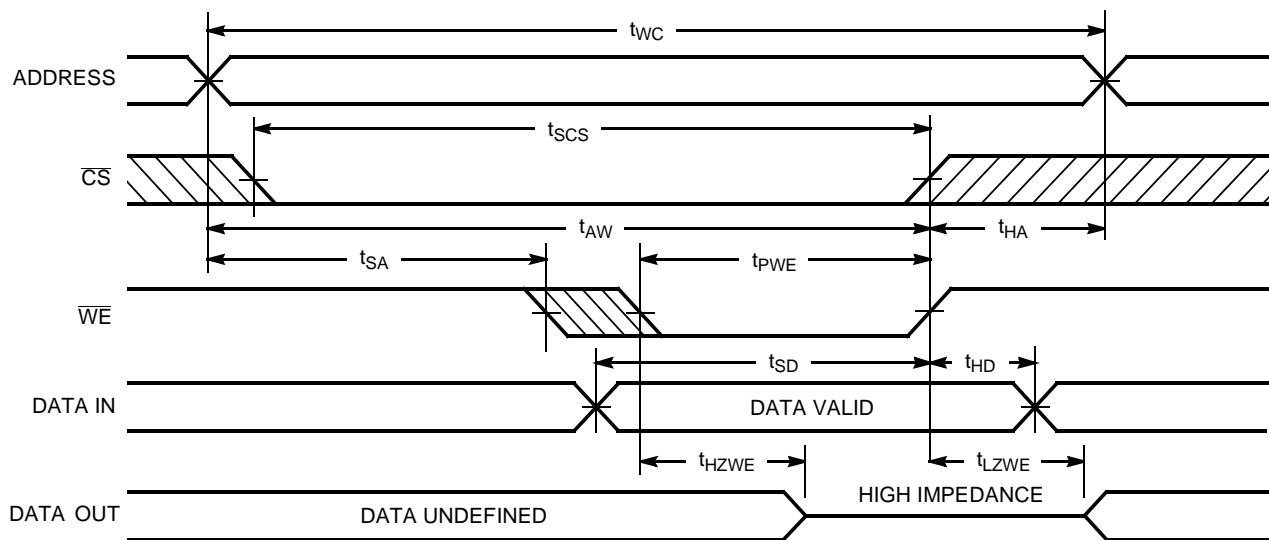
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

**Switching Waveforms**
**Read Cycle No. 1 [7, 8]**


1846-4

**Read Cycle No. 2 [7, 9]**


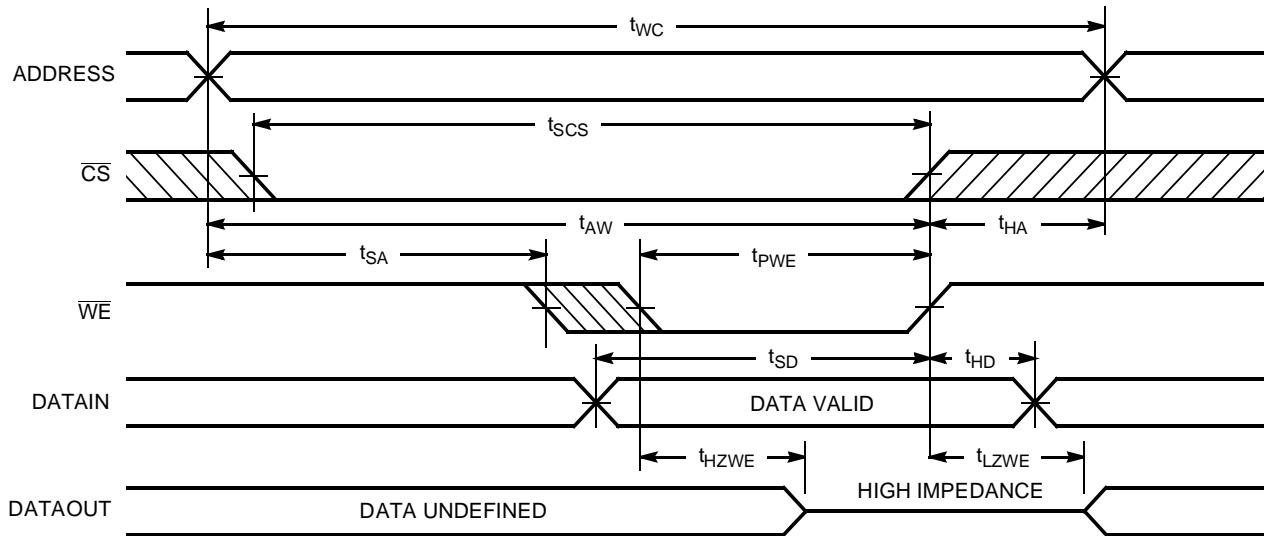
1846-5

**Write Cycle No. 1 (WE Controlled) [6]**


1846-6

**Notes:**

7. WE is HIGH for read cycle.
8. Device is continuously selected,  $\overline{CS} = V_{IL}$ , and  $\overline{OE} = V_{IL}$ .
9. Address valid prior to or coincident with CS transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{CS}$  Controlled) [6, 10]**

**Note:**

10. If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Truth Table**

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Inputs/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

**Ordering Information**

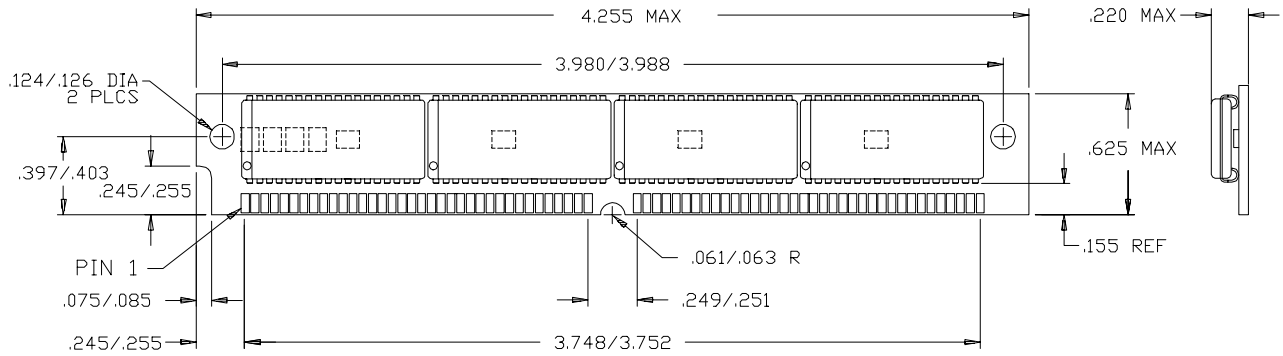
Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
12	CYM1846PM-12C	PM21	72-Pin Plastic SIMM Module	Commercial
	CYM1846P8-12C	PM21	72-Pin Plastic SIMM Module (gold contacts)	
	CYM1846PZ-12C	PZ11	72-Pin Plastic ZIP Module	
15	CYM1846PM-15C	PM21	72-Pin Plastic SIMM Module	Commercial
	CYM1846P8-15C	PM21	72-Pin Plastic SIMM Module (gold contacts)	
	CYM1846PZ-15C	PZ11	72-Pin Plastic ZIP Module	
20	CYM1846PM-20C	PM21	72-Pin Plastic SIMM Module	Commercial
	CYM1846P8-20C	PM21	72-Pin Plastic SIMM Module (gold contacts)	
	CYM1846PZ-20C	PZ11	72-Pin Plastic ZIP Module	
25	CYM1846PM-25C	PM21	72-Pin Plastic SIMM Module	Commercial
	CYM1846P8-25C	PM21	72-Pin Plastic SIMM Module (gold contacts)	
	CYM1846PZ-25C	PZ11	72-Pin Plastic ZIP Module	
35	CYM1846PM-35C	PM21	72-Pin Plastic SIMM Module	Commercial
	CYM1846P8-35C	PM21	72-Pin Plastic SIMM Module (gold contacts)	
	CYM1846PZ-35C	PZ11	72-Pin Plastic ZIP Module	

Shaded area contains preliminary information.

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Package Diagrams

72-Pin Plastic SIMM Module PM21



72-Pin Plastic ZIP Module PZ11

