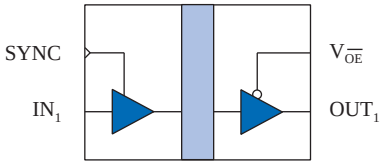
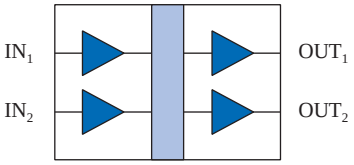
2 Mbps DC-Correct Digital Isolators

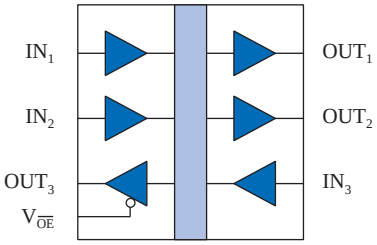
Functional Diagrams



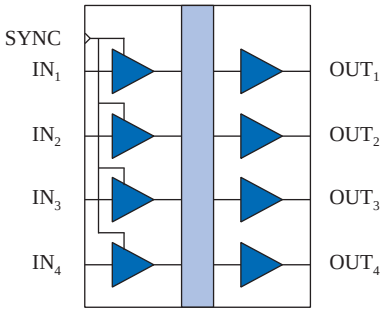
IL510



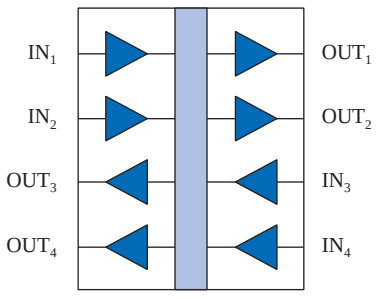
IL511



IL514



IL515



IL516

Features

- +5 V / +3.3 V CMOS/TTL Compatible
- 2 Mbps Maximum Speed
- DC-Correct
- External Clocking Option (IL510 and IL515)
- Very Low EMC
- 2500 V_{RMS} Isolation (1 min.)
- 10 ns Pulse Width Distortion
- 25 ns Propagation Delay
- 30 kV/µs Typical Common Mode Rejection
- 8-pin MSOP; 0.3" and 0.15" 8-pin and 16-pin SOIC Packages
- UL 1577 Approved; IEC 61010-2001 Approval Pending

Applications

- ADCs and DACs
- Digital Fieldbus
- RS-485 and RS-422
- Multiplexed Data Transmission
- Data Interfaces
- Board-to-Board Communication
- Hi-Fi Audio
- Digital Noise Reduction
- Ground Loop Elimination
- Peripheral Interfaces
- Parallel Bus
- Logic Level Shifting

Description

NVE's IL500-Series isolators are CMOS devices manufactured with NVE's patented* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology.

Compared to the industry-standard IL700-Series isolators, which have speeds up to 150 Mbps, IL500-Series isolators are more cost effective, offer a DC-correct design, and have an external clocking option on some models.

All IL500-Series isolator channels operate at 2 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a propagation delay of 25 ns and a pulse width distortion of 10 ns.

REV. C

Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	−55		150	°C	
Ambient Operating Temperature[1]	T_A	−55		150	°C	
Supply Voltage	V_{DD1}, V_{DD2}	−0.5		7	V	
Input Voltage	V_I	−0.5		V_{DD}+0.5	V	
Output Voltage	V_O	−0.5		V_{DD}+0.5	V	
Output Current Drive	I_O			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	T_A	−40		85	°C	
Supply Voltage	V_{DD1}, V_{DD2}	3.0		5.5	V	
Logic High Input Voltage	V_{IH}	2.4		V_{DD}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times[10]	t_{IR}, t_{IF}	DC-Correct				

Insulation Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance						
MSOP		3.0			mm	
0.15" SOIC (8-pin or 16-pin)		4.0			mm	
0.3" SOIC		8.1			mm	
Leakage Current			0.2		µA	240 V_{RMS}, 60 Hz
Barrier Impedance			$>10^{14}\|\|3$		Ω || pF	

Package Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Capacitance (Input–Output)[5]	C_{I-O}		4		pF	f = 1 MHz
Thermal Resistance						
MSOP	θ_{JC}		168		°C/W	Thermocouple at center underside of package
0.15" 8-pin SOIC	θ_{JC}		144		°C/W	
0.15" 16-pin SOIC	θ_{JC}		41		°C/W	
0.3" 16-pin SOIC	θ_{JC}		28		°C/W	
Package Power Dissipation	P_{PD}			150	mW	f = 1 MHz, V_{DD} = 5 V

Safety and Approvals

IEC61010-1

TUV Certificate Numbers: **N1502812, N1502812-101 pending**

Classification as Reinforced Insulation

Model	Package	Pollution Degree	Material Group	Max. Working Voltage
IL5xx-1 (pending)	MSOP	II	III	150 V_{RMS}
IL5xx-3	8-pin and 16-pin 0.15" SOIC	II	III	150 V_{RMS}
IL5xx	0.3" SOIC	II	III	300 V_{RMS}

UL 1577

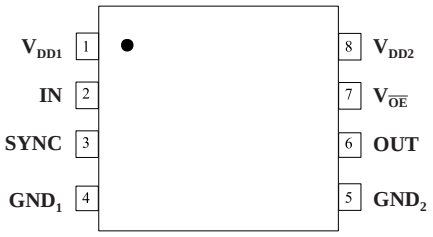
Component Recognition Program File Number: E207481
Rated 2500V_{RMS} for 1 minute

Soldering Profile

Per JEDEC J-STD-020C, MSL=2

IL510 Pin Connections

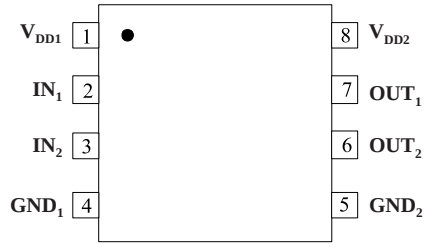
1	V_{DD1}	Supply voltage
2	IN	Data In
3	SYNC	External clock
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	OUT	Data Out
7	$V_{\overline{OE}}$	Output enable (internally held low with 100 kΩ)
8	V_{DD2}	Supply voltage



IL510

IL511 Pin Connections

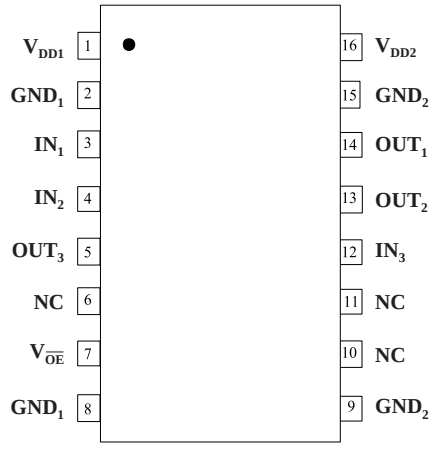
1	V_{DD1}	Supply voltage
2	IN_1	Data in, channel 1
3	IN_2	Data in, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	OUT_2	Data out, channel 2
7	OUT_1	Data out, channel 1
8	V_{DD2}	Supply voltage



IL511

IL514 Pin Connections

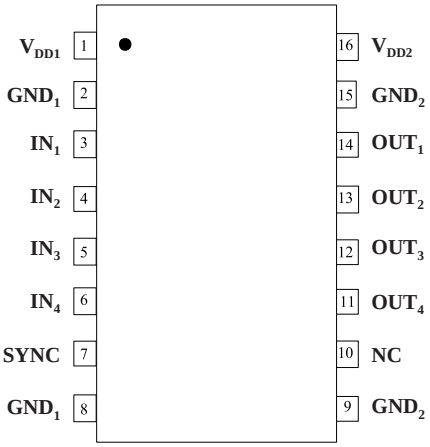
1	V_{DD1}	Supply Voltage 1
2	GND_1	Ground return for V_{DD1} (internally connected to pin 8)
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	OUT_3	Data out, channel 3
6	NC	No connection
7	$V_{\overline{OE}}$	Output enable, channel 3 (internally held low with 100 kΩ)
8	GND_1	Ground return for V_{DD1} (internally connected to pin 2)
9	GND_2	Ground return for V_{DD2} (internally connected to pin 15)
10	NC	No Connection
11	NC	No Connection
12	IN_3	Data in, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground return for V_{DD2} (internally connected to pin 9)
16	V_{DD2}	Supply voltage



IL514

IL515 Pin Connections

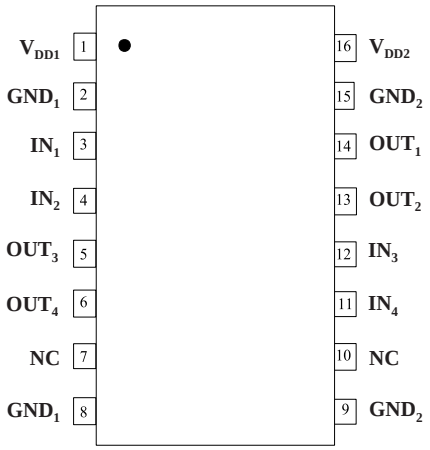
1	V_{DD1}	Supply voltage
2	GND_1	Ground return for V_{DD1}
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	IN_3	Data in, channel 3
6	IN_4	Data in, channel 4
7	SYNC	External clock
8	GND_1	Ground return for V_{DD1}
9	GND_2	Ground return for V_{DD2}
10	NC	No connection
11	OUT_4	Data out, channel 4
12	OUT_3	Data out, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground return for V_{DD2}
16	V_{DD2}	Supply voltage



IL515

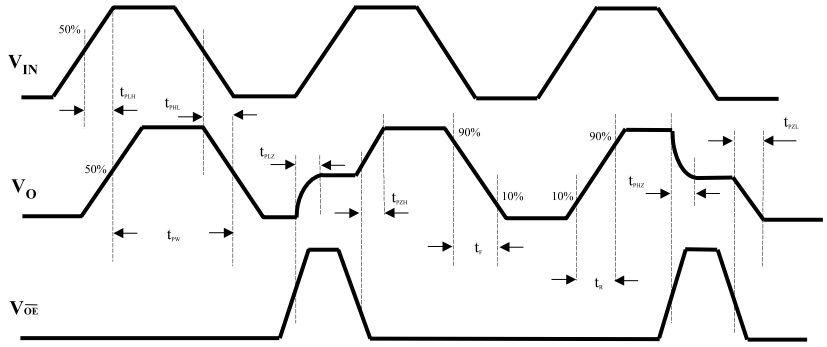
IL516 Pin Connections

1	V_{DD1}	Supply voltage
2	GND_1	Ground Return for V_{DD1}
3	IN_1	Data in, channel 1
4	IN_2	Data in, channel 2
5	OUT_3	Data out, channel 3
6	OUT_4	Data out, channel 4
7	NC	No connection
8	GND_1	Ground Return for V_{DD1}
9	GND_2	Ground Return for V_{DD2}
10	NC	No connection
11	IN_4	Data in, channel 4
12	IN_3	Data in, channel 3
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND_2	Ground Return for V_{DD2}
16	V_{DD2}	Supply voltage



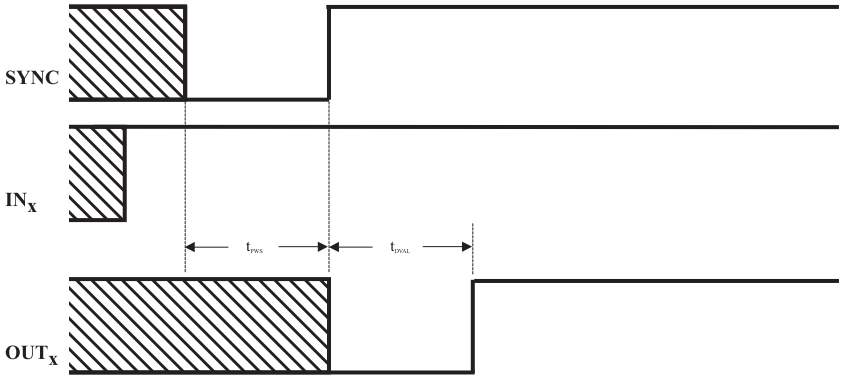
IL516

Timing Diagrams



Legend

t_{PLH}	Propagation Delay, Low to High
t_{PHL}	Propagation Delay, High to Low
t_{PW}	Minimum Pulse Width
t_{PLZ}	Propagation Delay, Low to High Impedance
t_{PZH}	Propagation Delay, High Impedance to High
t_{PHZ}	Propagation Delay, High to High Impedance
t_{PZL}	Propagation Delay, High Impedance to Low
t_R	Rise Time
t_F	Fall Time



Legend

t_{PWS}	SYNC Pulse Width
t_{DVAL}	Time Until Data Valid

Truth Tables

Output Enable

V_I	$V_{\overline{OE}}$	V_O
L	L	L
H	L	H
L	H	Z
H	H	Z

SYNC

SYNC	Function
0	Internal Refresh On
1	Internal Refresh Off
⎍	Input Data Latched to Output

Note: SYNC should be connected to GND to enable internal refresh, V_{DD} to disable internal refresh, or to an external clock. The SYNC pin should not be left unconnected.

3.3 Volt Electrical Specifications

Electrical specifications are T_{min} to T_{max} unless otherwise stated.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
DC Specifications						
Input Quiescent Supply Current						
IL510, IL511, IL515	I_{DD1}		15	30	µA	
IL514			1.7	2	mA	
IL516			3.3	4	mA	
Output Quiescent Supply Current						
IL510	I_{DD2}		1.7	2	mA	
IL511, IL514, IL516			3.3	4	mA	
IL515			6.6	8	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} − 0.1	V_{DD}		V	I_O = −20 µA, V_I = V_{IH}
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.5	0.8		I_O = 4 mA, V_I = V_{IL}
Switching Specifications						
Maximum Data Rate		2			Mbps	C_L = 15 pF
Pulse Width[7]	PW	20			ns	V_O 50% points; SYNC=0
		25			ns	V_O 50% points; SYNC=1
Propagation Delay Input to Output (High to Low)	t_{PHL}			25	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}			25	ns	C_L = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t_{PHZ}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t_{PLZ}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t_{PZH}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t_{PZL}			5	ns	C_L = 15 pF
Pulse Width Distortion[2]	PWD			10	ns	C_L = 15 pF
Propagation Delay Skew[3]	t_{PSK}			10	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		1	3	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)[4]	$\|CM_H\|$,$\|CM_L\|$	20	30		kV/µs	V_{CM} = 300 V
Channel-to-Channel Skew	t_{CSK}		3	5	ns	C_L = 15 pF
SYNC Timing						
SYNC Time Until Data Valid	t_{DVAL}			9	µs	
Internal Clock Off Time[11]	t_{OFF}			5	ns	
SYNC Pulse Width	t_{PWS}	10			µs	
Internal Clock Pulse Width	t_{PWI}	3.5		5	ns	
Dynamic Power Consumption[6]			140	240	µA/MHz	per channel
Magnetic Field Immunity[8] (V_{DD2}= 3V, 3V<V_{DD1}<5.5V)						
Power Frequency Magnetic Immunity	H_{PF}	1000	1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}	1800	2000		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}	1800	2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier[9]	K_X		2.5			

5 Volt Electrical Specifications

Electrical specifications are T_{min} to T_{max} unless otherwise stated.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
DC Specifications						
Input Quiescent Supply Current						
IL510, IL511, IL515	I_{DD1}		24	40	µA	
IL514			2	3	mA	
IL516			5	6	mA	
Output Quiescent Supply Current						
IL510	I_{DD2}		2	3	mA	
IL511, IL514, IL516			4	6	mA	
IL515			9	12	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} − 0.1	V_{DD}		V	I_O = −20 µA, V_I = V_{IH}
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.5	0.8		I_O = 4 mA, V_I = V_{IL}
Switching Specifications						
Maximum Data Rate		2			Mbps	C_L = 15 pF
Pulse Width[7]	PW	20			ns	V_O 50% points; SYNC=0
		25			ns	V_O 50% points; SYNC=1
Propagation Delay Input to Output (High to Low)	t_{PHL}			25	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}			25	ns	C_L = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t_{PHZ}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t_{PLZ}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t_{PZH}			5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t_{PZL}			5	ns	C_L = 15 pF
Pulse Width Distortion[2]	PWD			10	ns	C_L = 15 pF
Propagation Delay Skew[3]	t_{PSK}			10	ns	C_L = 15 pF
Output Rise Time (10%−90%)	t_R		1	3	ns	C_L = 15 pF
Output Fall Time (10%−90%)	t_F		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)[4]	$\|CM_H\|$,$\|CM_L\|$	20	30		kV/µs	V_{cm} = 300 V
Channel-to-Channel Skew	t_{CSK}		3	5	ns	C_L = 15 pF
SYNC Timing						
SYNC Time Until Data Valid	t_{DVAL}			9	µs	
Internal Clock Off Time[11]	t_{OFF}			5	ns	
SYNC Pulse Width	t_{PWS}	10			µs	
Internal Clock Pulse Width	t_{PWI}	3.5		5	ns	
Dynamic Power Consumption[6]			200	340	µA/MHz	per channel
Magnetic Field Immunity[8] (V_{DD2}= 5V, 3V<V_{DD1}<5.5V)						
Power Frequency Magnetic Immunity	H_{PF}	2800	3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}	4000	4500		A/m	t_p = 8 µs
Damped Oscillatory Magnetic Field	H_{OSC}	4000	4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier[9]	K_X		2.5			

Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25°C.
4. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins on each side of the package are shorted.
6. Dynamic power consumption is calculated per channel and is supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 9.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 9).
10. If internal clock is used, devices will respond to DC states on inputs within a maximum of 9 µs. Outputs may oscillate if SYNC input slew rate is less than 1 V/ms.
11. t_{off} is the maximum time for the internal clock to shut down.

Application Information

Electrostatic Discharge Sensitivity

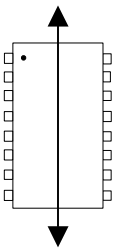
This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

The IL500-Series is fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. The IsoLoop Isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. NVE conducted compliance tests in the categories below:

EN50081-1
Residential, Commercial & Light Industrial
Methods EN55022, EN55014
EN50082-2: Industrial Environment
Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)
ENV50204
Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



Cross-axis Field Direction

Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. A magnetic field is created around the GMR Wheatstone bridge by detecting the edge transitions of the input logic signal and converting them to narrow current pulses. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

Power Supply Decoupling

Both power supplies to these devices should be decoupled with low ESR ceramic capacitors of at least 47 nF. Capacitors must be located as close as possible to the V_{DD} pins.

DC Correctness, EMC, and the SYNC Function

NVE digital isolators have the lowest EMC noise signature of any high-speed digital isolator on the market today because of the dc nature of the GMR sensors used. It is perhaps fair to include opto-couplers in that dc category too, but their limited parametric performance, physically large size, and wear-out problems effectively limit side by side comparisons between NVE's isolators and isolators coupled with RF, matched capacitors, or transformers.

The IL500-Series marks a departure from other NVE coupler families with the inclusion of a patented, controllable refresh clock. The clock ensures that outputs will be synchronized to inputs within 9 µs of the supply voltage passing the CMOS circuit's 1.5 V V_T threshold. Alternatively, on certain models the user can supply an external synchronization clock. There are several advantages to this form of control, the most important being that at power up the user no longer needs to design a synchronization circuit or add firmware to ensure the output is at the same logic level as the input. Unlike other technologies, however, the clock is not required for normal operation and can be gated off to reduce the EMC signature of the end product. This has many advantages in noise-critical applications such as hi-fi audio, motor control, and power conversion. It also allows the use of standard Power on Reset (POR) circuits, common in microcontroller applications, as the means of ensuring the output of the device is in the same state as the input a short time after power up. Figure 1 shows a practical Power on Reset circuit. Decoupling capacitors are omitted for clarity.

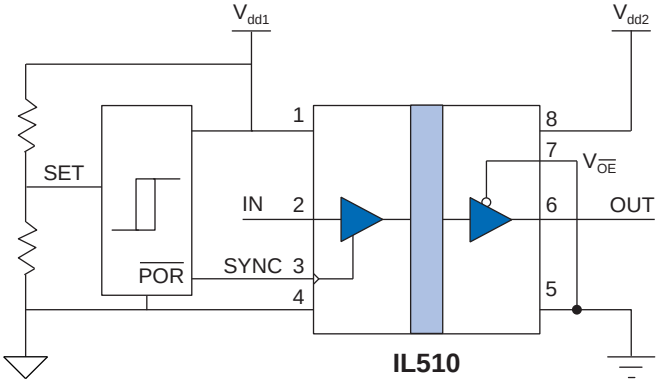


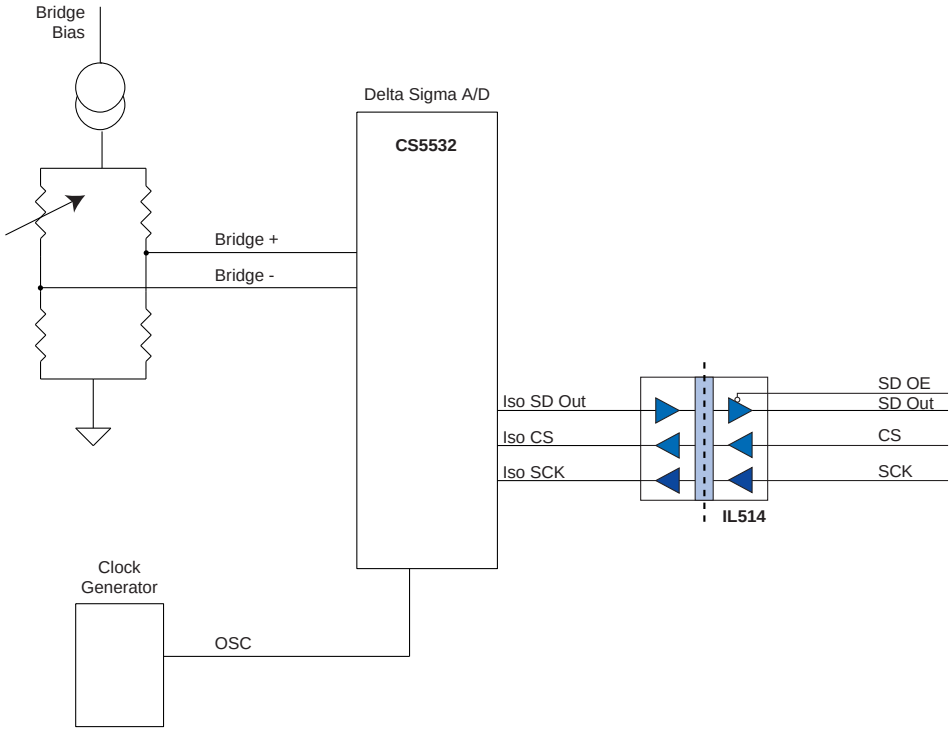
Fig. 1. Typical Power On Reset Circuit for IL510

If multiple devices are used on a board and the designer wants to use the refresh clock in continuous mode, the external clock signal can be provided to each IL5xx Isolator, without the beat-frequency noise problems inherent with competing isolator technologies.

The IL510 and IL515 have the SYNC function available to the user. The IL511, IL514, and IL516 are available in continuous clocking mode only (the user cannot turn off the refresh clock on those devices).

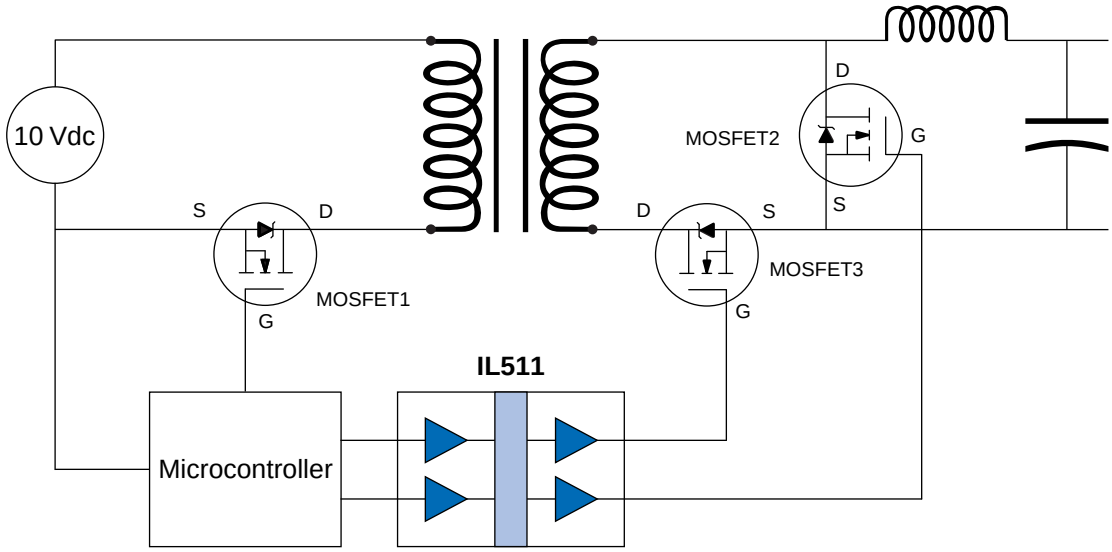
Illustrative Applications

Isolated A/D Converter



A delta-sigma A-D converter interfaced with the three-channel IL514. Multiple channels can easily be combined using the IL514's output enable function.

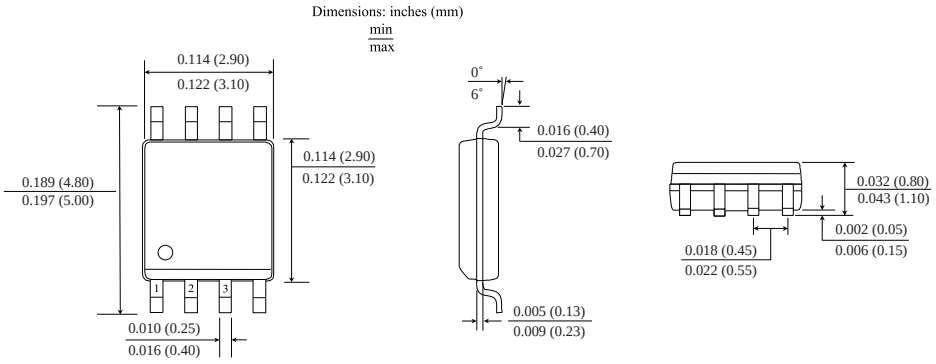
Intelligent DC-DC Converter With Synchronous Rectification



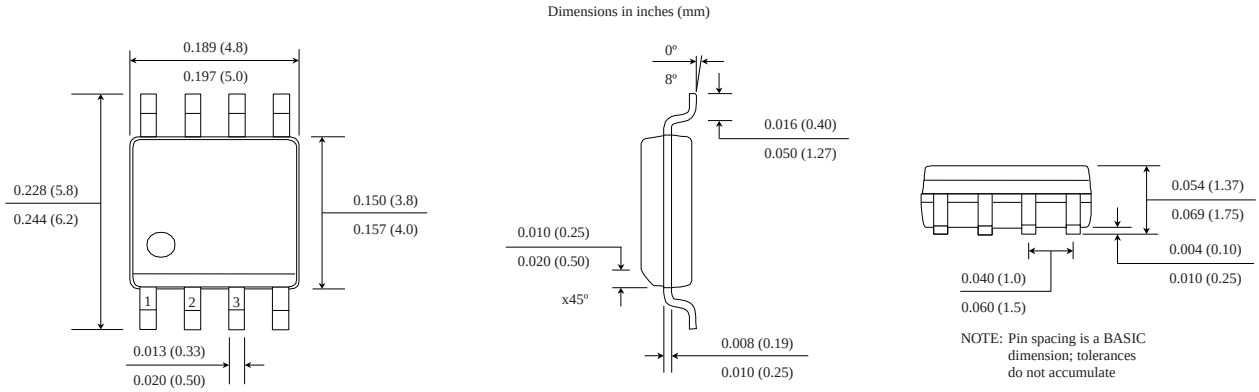
A typical primary-side controller uses the IL511 to drive the synchronous rectification signals from primary side to secondary side. IL511 pulse-width distortion of 10 ns minimizes MOSFET dead time and maximizes efficiency. The ultra-small MSOP package minimizes board area.

Package Drawings, Dimensions, and Specifications

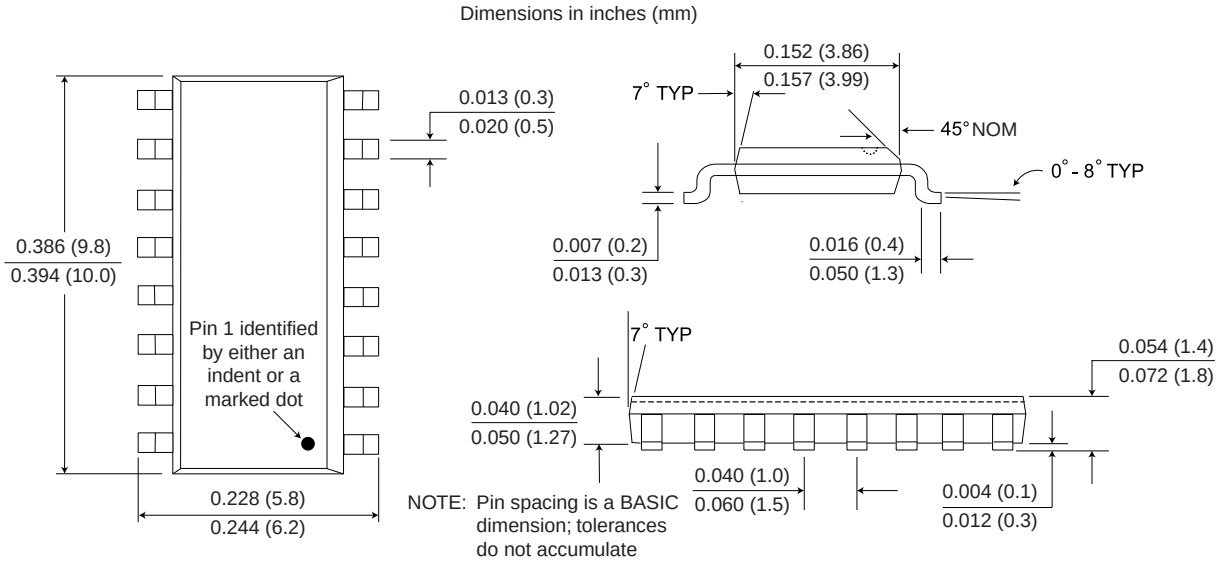
8-pin MSOP



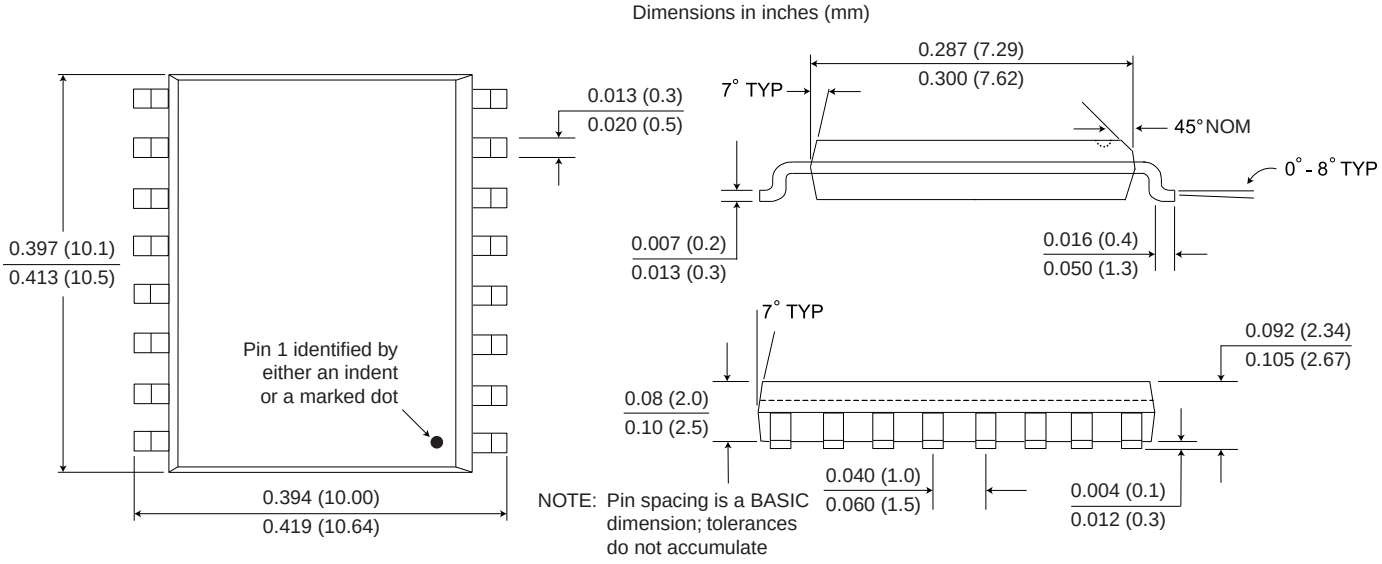
8-pin SOIC Package



16-pin 0.15" SOIC Package



16-pin 0.3" SOIC Package



Ordering Information

IL 5 16 - 3 E TR13

Bulk Packaging
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

Package
Blank = 80/20 Tin/Lead Plating
E = RoHS Compliant

Package Type
-1 = 8-pin MSOP
-3 = 0.15" 8-pin or 16-pin SOIC (not available for IL515)
Blank = 0.30" 16-pin SOIC

Channels
10 = 1 Drive Channel
11 = 2 Drive Channels
14 = 2 Drive Channels; 1 Receive Channel
15 = 4 Drive Channels
16 = 2 Drive Channels; 2 Receive Channels

Base Part Number
5 = 2 Mbps, DC-Correct

Product Family
IL = Isolators

RoHS COMPLIANT

ISB-DS-001-IL500-C **July 2008**	**Production release**
ISB-DS-001-IL500-B July 2008	Initial release
ISB-DS-001-IL500-A June 2008	Preliminary release

About NVE

An ISO 9001 Certified Company

NVE Corporation is a high technology components manufacturer having the unique capability to combine spintronic Giant Magnetoresistive (GMR) materials with integrated circuits to make high performance electronic components. Products include Magnetic Field Sensors, Magnetic Field Gradient Sensors (Gradiometer), Digital Magnetic Field Sensors, Digital Signal Isolators and Isolated Bus Transceivers.

NVE is a leader in GMR research and in 1994 introduced the world's first products using GMR material, a line of GMR magnetic field sensors that can be used for position, magnetic media, wheel speed and current sensing.

NVE is located in Eden Prairie, Minnesota, a suburb of Minneapolis. Please visit our Web site at www.nve.com or call (952) 829-9217 for information on products, sales or distribution.

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