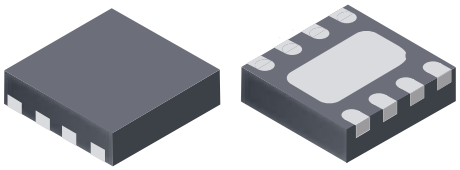
Ultra Small Mobile Phone Xenon Photoflash Capacitor Charger with IGBT Driver

Features and Benefits

- Ultra small 2 × 2 DFN/MLP-8 package
- Low quiescent current draw (0.5 µA max. in shutdown mode)
- Primary-side output voltage sensing; no resistor divider required
- Fixed 1.5 A peak current limit
- 1.3 V logic (V_{HI}(min)) compatibility
- Integrated IGBT driver with internal gate resistors
- Optimized for mobile phone, 1-cell Li+ battery applications
- Zero-voltage switching for lower loss
- >75% efficiency
- Charge complete indication
- Integrated 50 V DMOS switch with self-clamping protection

Package: 8-pin DFN/MLP (suffix EE)



2 mm × 2 mm, 0.60 mm height

Not to scale

Description

The Allegro® A8740 is a Xenon photoflash charger IC designed to meet the needs of ultra low power, small form factor cameras, particularly camera phones. By using primary-side voltage sensing, the need for a secondary-side resistive voltage divider is eliminated. This has the additional benefit of reducing leakage currents on the secondary side of the transformer. To extend battery life, the A8740 features very low supply current draw (0.5 µA max in shutdown mode). The IGBT driver also has internal gate resistors for minimum external component count. The charge and trigger voltage logic thresholds are set at 1.3 V_{HI}(min) to support applications implementing low-voltage control logic.

The A8740 is available in an 8-contact 2 mm × 2 mm DFN/MLP package with a 0.60 maximum overall package height, and an exposed pad for enhanced thermal performance. It is lead (Pb) free with 100% matte tin leadframe plating.

Typical Applications

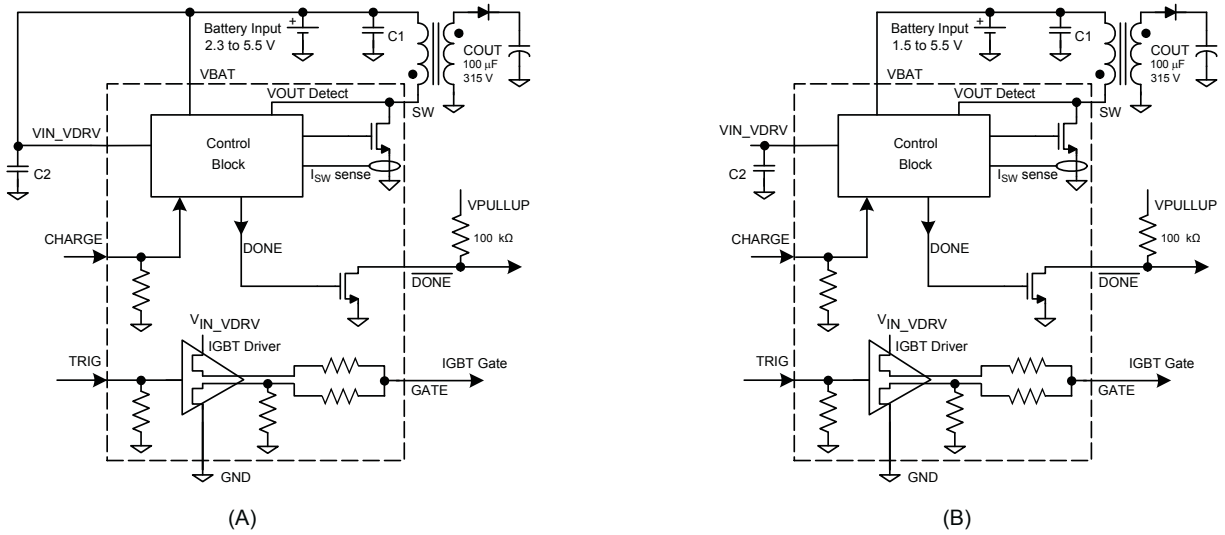


Figure 1. Typical applications: (A) with single battery supply and (B) with separate bias supply

Selection Guide

Part Number	Packing	Package
A8740EEETR-T	3000 pieces per reel	8-contact DFN/MLP with exposed thermal pad

Absolute Maximum Ratings

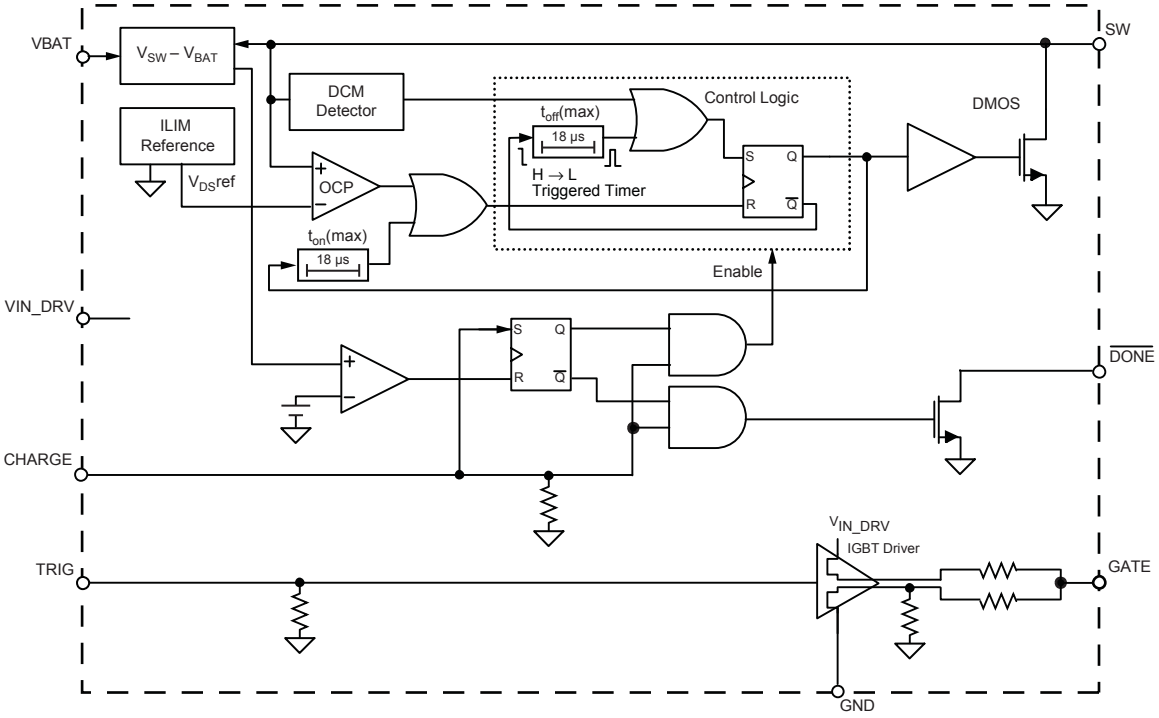
Characteristic	Symbol	Notes	Rating	Units
SW Pin	V_{SW}	DC voltage. (V_{SW} is self-clamped by internal active clamp and is allowed to exceed 50 V during flyback spike durations. Maximum repetitive energy during flyback spike: 0.5 µJ at frequency ≤ 400 kHz.)	–0.3 to 50	V
	I_{SW}	DC current, pulse width = 1 ms	3	A
VIN_DRV, VBAT Pins	V_{IN}		–0.3 to 6.0	V
CHARGE, TRIG, $\overline{\text{DONE}}$ Pins		Care should be taken to limit the current when –0.6 V is applied to these pins.	–0.6 to V_{IN} + 0.3 V	V
Remaining Pins			–0.3 to V_{IN} + 0.3 V	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

THERMAL CHARACTERISTICS may require derating at maximum conditions

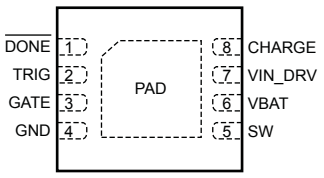
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB, based on JEDEC standard	49	ºC/W

*Additional thermal information available on Allegro Web site.

Functional Block Diagram



Pin-out Diagram



(Top View)

Terminal List

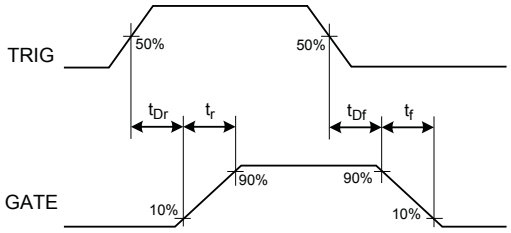
Number	Name	Function
1	$\overline{DONE}$	Open collector output, pulls low when output reaches target value and CHARGE is high. Goes high during charging or whenever CHARGE is low.
2	TRIG	IGBT trigger input.
3	GATE	IGBT gate drive output.
4	GND	Ground connection.
5	SW	Drain connection of internal DMOS switch. Connect to transformer primary winding.
6	VBAT	Battery voltage.
7	VIN_DRV	Input voltage. Connect to 3 to 5.5 V bias supply. Decouple V_{IN} voltage with 0.1 µF ceramic capacitor placed close to this pin.
8	CHARGE	Charge enable pin. Set this pin low to shut down the chip.
–	PAD	Exposed pad for enhanced thermal dissipation. Connect to ground plane.

ELECTRICAL CHARACTERISTICS Typical values are valid at V_{IN} = V_{BAT} = 3.6 V; T_A = 25°C, except ● indicates specifications guaranteed from −40°C to 85°C ambient, unless otherwise noted

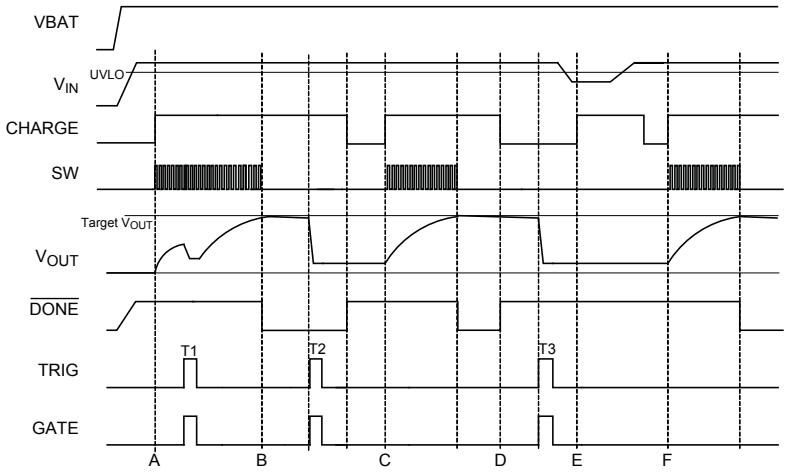
Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
VBAT Voltage Range[1]	V_{BAT}		●	1.5	–	5.5	V
VIN_DRV Voltage Range[1]	V_{IN}		●	2.3	–	5.5	V
UVLO Enable Threshold	V_{INUV}	V_{IN} rising		–	2.05	2.2	V
UVLO Hysteresis	$V_{INUV(hys)}$			–	150	–	mV
V_{IN} Supply Current	I_{IN}	Shutdown (CHARGE = 0 V, TRIG = 0 V)		–	0.02	0.5	µA
		Charging complete		–	50	100	µA
		Charging (CHARGE = V_{IN}, TRIG = 0 V)		–	2	–	mA
VBAT Pin Supply Current	I_{BAT}	Shutdown (CHARGE = 0 V, TRIG = 0 V)		–	0.01	1	µA
		Charging done (CHARGE = V_{IN}, $\overline{DONE}$ = 0 V)		–	–	5	µA
		Charging (CHARGE = V_{IN}, TRIG = 0 V)		–	–	50	µA
Current Limit							
Primary-Side Current Limit[2]	I_{SWLIM}			1.35	1.5	1.65	A
Switch On-Resistance	$R_{SWDS(on)}$	V_{IN_DRV} = 3.6 V, I_D = 600 mA, T_A = 25°C		–	0.4	–	Ω
Switch Leakage Current[1]	I_{SWLK}	V_{SW} = 5.5, over full temperature range	●	–	–	2	µA
CHARGE Pull-down Resistance	R_{CHGPD}			–	130	–	kΩ
CHARGE Input Voltage[1]	V_{CHARGE}	High, over input supply range	●	1.3	–	–	V
		Low, over input supply range	●	–	–	0.5	V
CHARGE On/Off Delay	t_{CH}	Time between CHARGE = 1 and charging enabled		–	20	–	us
Switch-Off Timeout	$t_{off(max)}$			–	18	–	µs
Switch-On Timeout	$t_{on(max)}$			–	18	–	µs
Output Comparator Trip Voltage[3]	$V_{OUTTRIP}$	Measured as V_{SW} – V_{BAT}		31.0	31.5	32.0	V
Output Comparator Voltage Overdrive	V_{OUTOV}	Pulse width = 200 ns (90% to 90%)		–	200	400	mV
$\overline{DONE}$ Output Leakage Current[1]	I_{DONELK}		●	–	–	1	µA
$\overline{DONE}$ Output Low Voltage[1]	V_{DONEL}	32 µA into $\overline{DONE}$ pin	●	–	–	100	mV
dV/dt Threshold for ZVS Comparator	dV/dt	Measured at SW pin		–	20	–	V/µs
IGBT Driver							
TRIG Input Voltage[1]	$V_{TRIG(H)}$	Input = logic high, over input supply range	●	1.3	–	–	V
	$V_{TRIG(L)}$	Input = logic low, over input supply range	●	–	–	0.5	V
TRIG Pull-Down Resistor	R_{TRIGPD}			–	130	–	kΩ
GATE Resistance to VIN_DRV	$R_{SrcDS(on)}$	V_{GATE} = 1.8 V		–	6.6	–	Ω
GATE Resistance to GND	$R_{SnkDS(on)}$	V_{GATE} = 1.8 V		–	50	–	Ω
Propagation Delay (Rising)[4,5]	t_{Dr}	Measurement taken at $\overline{DONE}$ pin, C_L= 6500 pF		–	25	–	ns
Propagation Delay (Falling)[4,5]	t_{Df}			–	60	–	ns
Output Rise Time[4,5]	t_r			–	80	–	ns
Output Fall Time[4,5]	t_f			–	700	–	ns
GATE Pull-Down Resistor	R_{GTPD}			–	20	–	kΩ

[1]Specifications throughout the range T_A = –40°C to 85°C guaranteed by design and characterization.
[2]Current limit guaranteed by design and correlation to static test.
[3]Specifications throughout the range T_A = –20°C to 85°C guaranteed by design and characterization.
[4]Guaranteed by design and characterization.
[5]See IGBT Drive Timing Definition diagram for further information.

IGBT Drive Timing Definition



Operation Timing Diagram



Explanation of Events

A: Start charging by pulling CHARGE to high, provided that V_{IN} is above UVLO level.

B: Charging stops when V_{OUT} reaches the target voltage

C: Start a new charging process with a low-to-high transition at the CHARGE pin.

D: Pull CHARGE to low to put the controller in low-power standby mode.

E: Charging does not start, because V_{IN} is below UVLO level when CHARGE goes high.

F: After V_{IN} goes above UVLO, another low-to-high transition at the CHARGE pin is required to start the charging.

T1, T2, T3 (Trigger instances): IGBT driver output pulled high whenever the TRIG pin is at logic high. It is recommended to avoid applying any trigger pulses during charging.

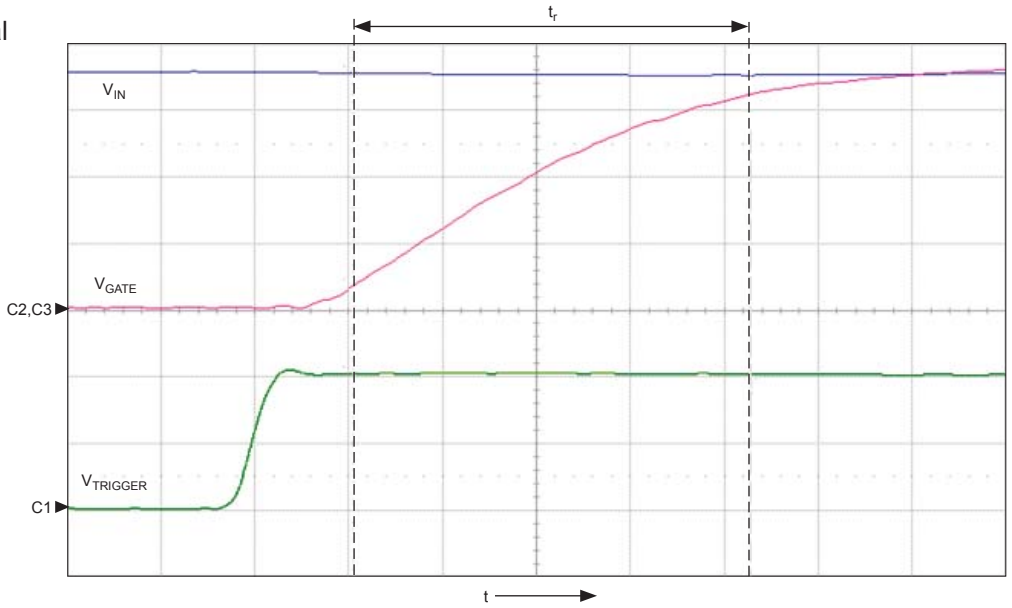
Characteristic Performance

IGBT Drive Performance

IGBT drive waveforms are measured at pin, with capacitive load of 6800 pF

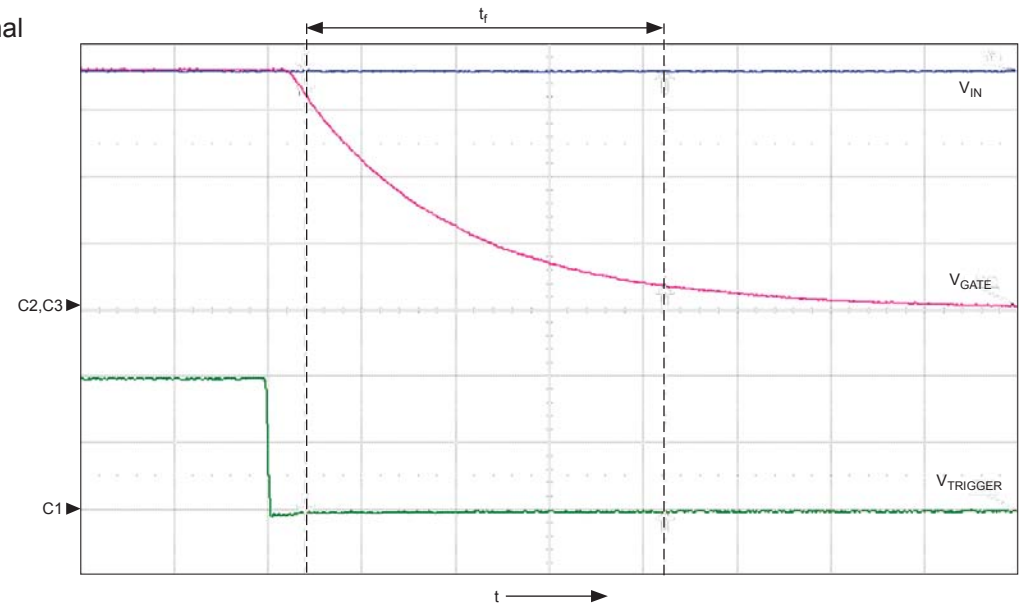
Rising Signal

Symbol	Parameter	Units/Division
C1	$V_{TRIGGER}$	1 V
C2	V_{GATE}	1 V
C3	V_{IN}	1 V
t	time	20 ns
Conditions	**Parameter**	**Value**
	t_{Dr}	21 ns
	t_r	85 ns
	C_{LOAD}	6.8 nF



Falling Signal

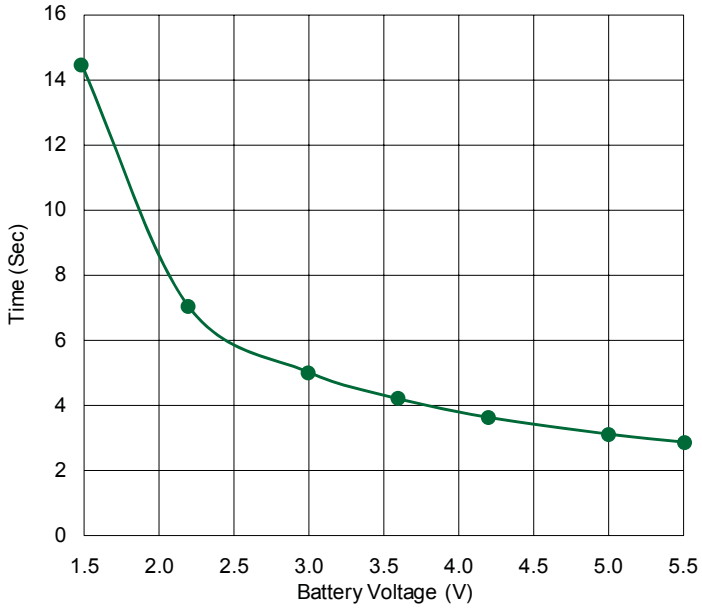
Symbol	Parameter	Units/Division
C1	$V_{TRIGGER}$	1 V
C2	V_{GATE}	1 V
C3	V_{IN}	1 V
t	time	200 ns
Conditions	**Parameter**	**Value**
	t_{Df}	80 ns
	t_f	765 ns
	C_{LOAD}	6.8 nF



Characteristic Performance

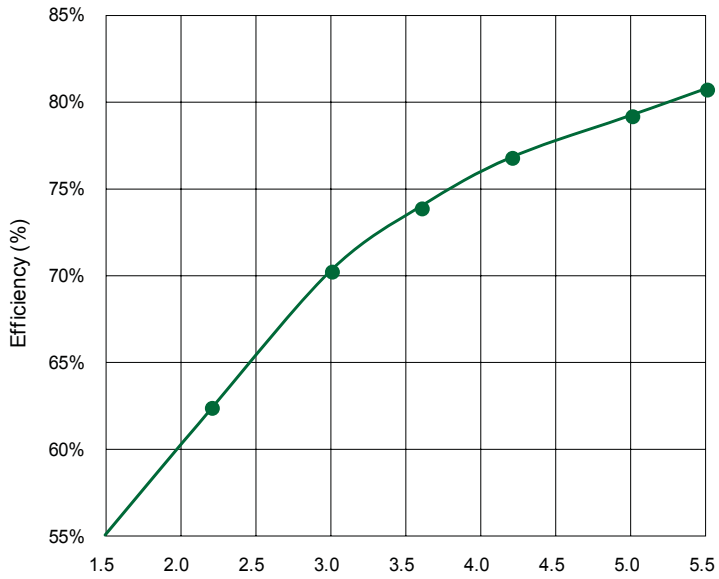
Charge Time versus Battery Voltage

Transformer $L_{PRIMARY}$ = 12.8 µH, N =10.25, V_{IN} =3.6 V, C_{OUT} = 100 µF / 330 V UCC, at room temperature



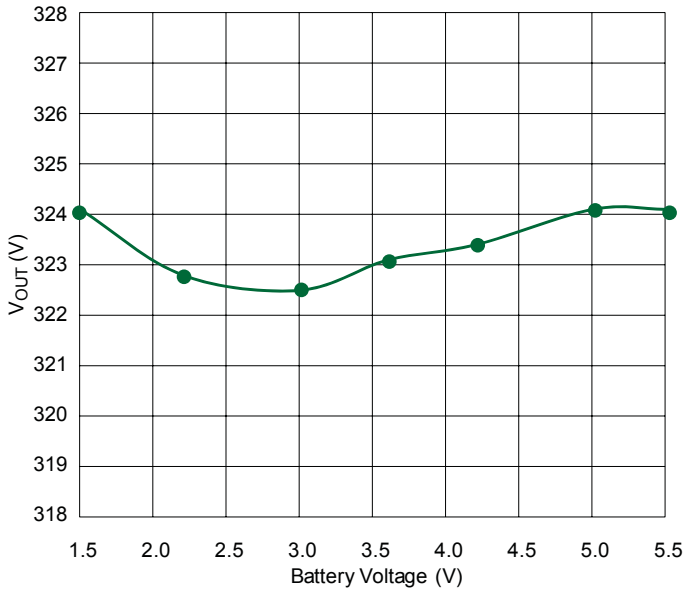
Efficiency versus Battery Voltage

Transformer $L_{PRIMARY}$ = 12.8 µH, N =10.25, V_{IN} =3.6 V, at room temperature



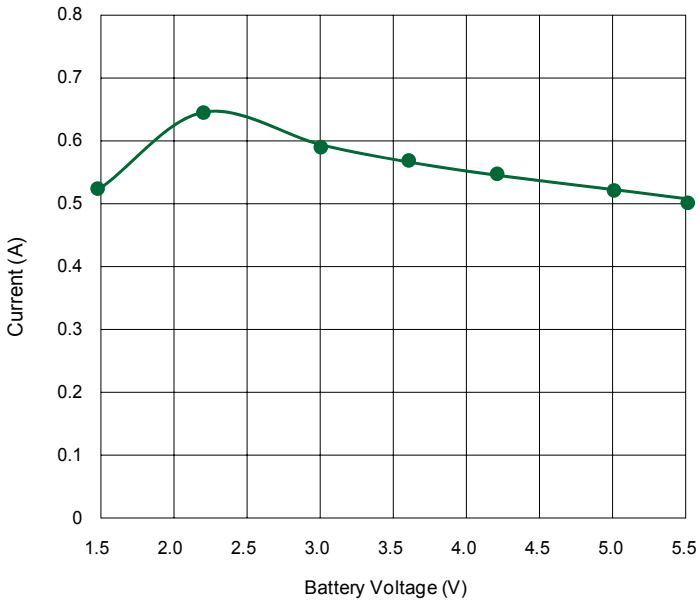
Final Output Voltage versus Battery Voltage

Transformer $L_{PRIMARY}$ = 12.8 µH, N =10.25, V_{IN} =3.6 V, at room temperature



Average Input Current versus Battery Voltage

Transformer $L_{PRIMARY}$ = 12.8 µH, N =10.25, V_{IN} =3.6 V, at room temperature



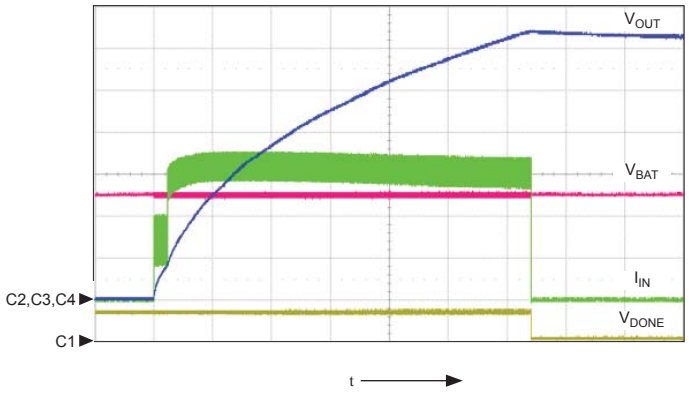
Note: Peak switch current is limited by the maximum on-time and di/dt of the transformer primary current; therefore, average input current drops at very low battery voltage.

Charging Waveforms

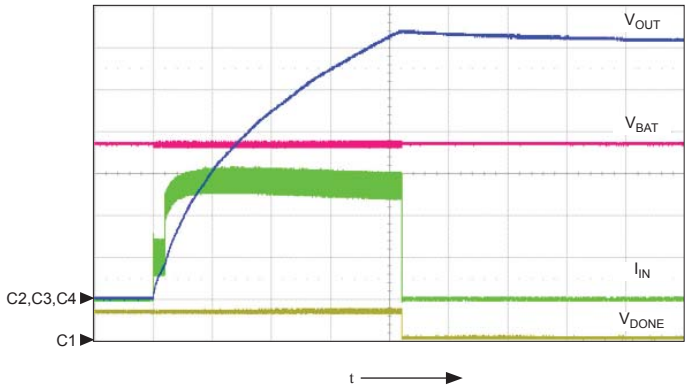
Output Capacitor Charging at Various Battery Voltages

Test conditions: V_{IN} = 3.6 V, C_{OUT} = 100 µF / 330 V UCC, transformer = T-16-024A ($L_{PRIMARY}$ =12.8 µH, N = 10.25), at room temperature
Oscilloscope settings: Ch1 = $\overline{DONE}$ (5 V / div), Ch2 = Battery Voltage (1 V / div), Ch3 = Output Voltage (50 V / div), Ch4 = Input Current (200 mA V / div), Time scale = 1 sec / div

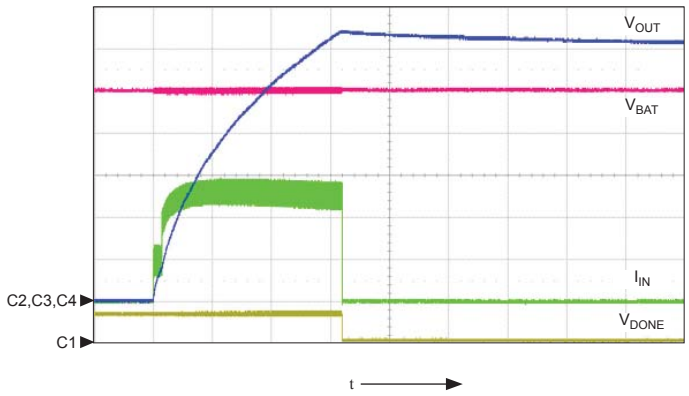
V_{BAT} = 2.5 V



V_{BAT} = 3.7 V



V_{BAT} = 5.0 V



Functional Description

General Operation Overview

The charging operation is started by a low-to-high signal on the CHARGE pin, provided that V_{IN} is above the V_{UVLO} level. It is strongly recommended to keep the CHARGE pin at logic low during power-up. After V_{IN} exceeds the UVLO level, a low-to-high transition on the CHARGE pin is required to start the charging. The $\overline{DONE}$ open-drain indicator is pulled low when CHARGE is high and target output voltage is reached.

When a charging cycle is initiated, the transformer primary side current, $I_{PRIMARY}$, ramps-up linearly at a rate determined by the combined effect of the battery voltage, V_{BAT}, and the primary side inductance, $L_{PRIMARY}$. When $I_{PRIMARY}$ reaches the current limit, I_{SWLIM}, the internal MOSFET is turned off immediately, allowing the energy to be pushed into the photoflash capacitor, C_{OUT}, from the secondary winding. The secondary side current drops linearly as C_{OUT} charges. The switching cycle starts again, either after the transformer flux is reset, or after a predetermined time period, t_{OFF}(max) (18 µs), whichever occurs first.

The A8740 senses output voltage indirectly on primary side. This eliminates the need for high voltage feedback resistors required for secondary sensing. Flyback converter stops switching when output voltage reaches:

$$V_{OUT} = K \times N - V_d ,$$

Where:

K = 31.5 V typically,

V_d is the forward drop of the output diode (approximately 2 V), and

N is transformer turns ratio.

Switch On-Time and Off-Time Control

The A8740 implements an adaptive on-time/off-time control. On-time duration, t_{on}, is approximately equal to

$$t_{on} = I_{SWlim} \times L_{PRIMARY} / V_{BAT} .$$

Off-time duration, t_{off}, depends on the operating conditions during switch off-time. The A8740 applies two charging modes: Fast Charging mode and Timer mode, according to the conditions described in the next section.

Timer Mode and Fast Charging Mode

The A8740 achieves fast charging times and high efficiency by operating in discontinuous conduction mode (DCM) through most of the charging process. The relationship of Timer mode and Fast Charging mode is shown in figure 2.

The IC operates in Timer mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 30 V (depending on transformer used). Timer mode is a fixed period, 18 µs, off-time control. One advantage of having Timer mode is that it limits the initial battery current surge and thus acts as a "soft-start." A time-expanded view of a Timer mode interval is shown in figure 3.

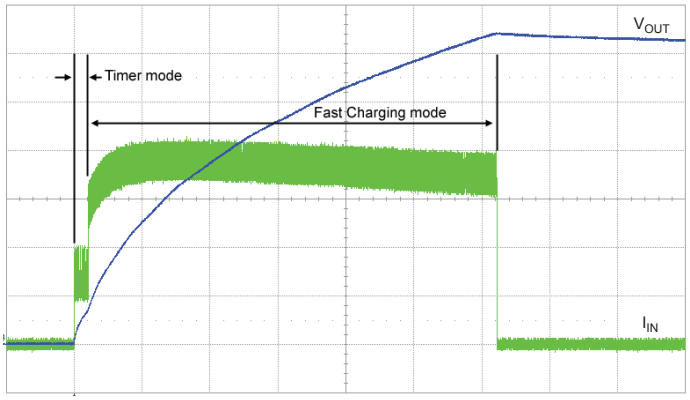


Figure 2. Timer mode and Fast Charging mode: t = 1 s/div; V_{OUT} = 50 V/div; I_{IN} = 150 mA/div., V_{IN} = V_{BAT} = 3.6 V; C_{OUT} = 100 µF/330 V; and ILIM = 1.0 A.

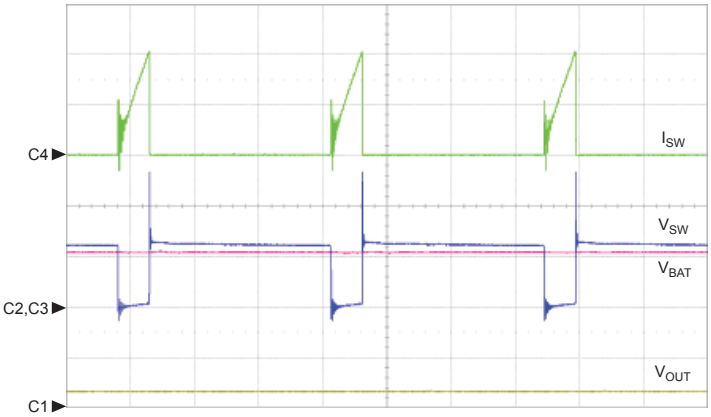


Figure 3. Expanded view of Timer mode: $V_{OUT} \leq$ 10 V, V_{BAT} = 5.5 V, Ch1: V_{OUT} = 20 V/div., Ch2: V_{BAT} = 5 V/div., Ch3: V_{SW} = 5 V/div., Ch4: I_{SW} = 750 mA/div., t = 5 µs / div.

As soon as a sufficient voltage has built up at the output capacitor, the IC enters Fast-Charging mode. In this mode, the next switching cycle starts after the secondary side current has stopped flowing, and the switch voltage has dropped to a minimum value. A proprietary circuit is used to allow minimum-voltage switching, even if the SW pin voltage does not drop to 0 V. This enables Fast-Charging mode to start earlier, thereby reducing the overall charging time. Minimum-voltage switching is shown in figure 4.

During Fast-Charging mode, when V_{OUT} is high enough (over 50 V), true zero-voltage switching (ZVS) is achieved. This further improves efficiency as well as reduces switching noise. A ZVS interval is shown in figure 5.

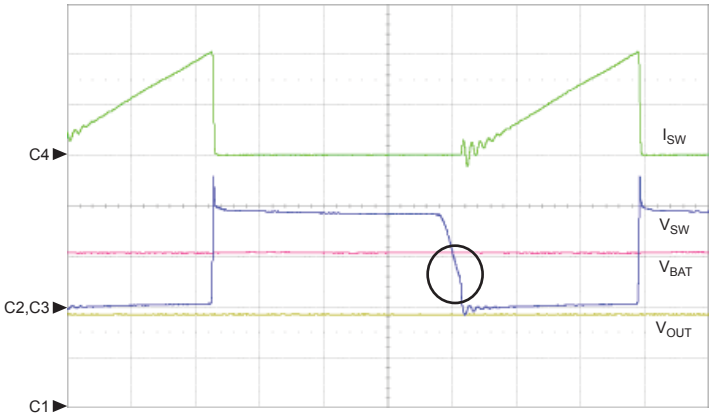


Figure 4. Minimum-voltage switching: $V_{OUT} \geq 35$ V, V_{BAT} = 5.5 V, Ch1: V_{OUT} = 20 V/div., Ch2: V_{BAT} = 5 V/div., Ch3: V_{SW} = 5 V/div., Ch4: I_{SW} = 750 mA/div., t = 1 µs / div.

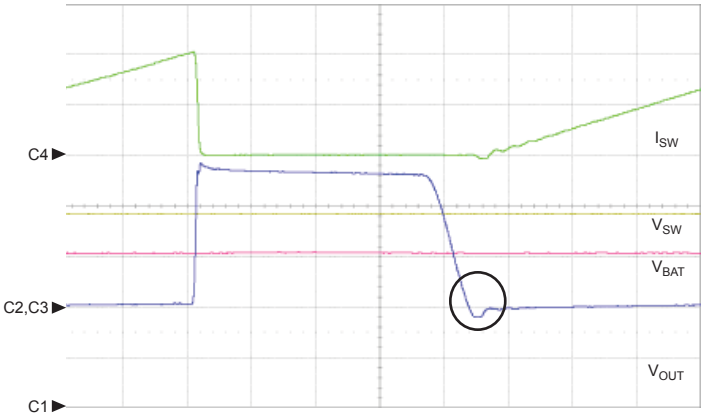


Figure 5. True zero-voltage switching (ZVS): V_{OUT} = 75 V, V_{BAT} = 5.5 V, Ch1: V_{OUT} = 20 V/div., Ch2: V_{BAT} = 5 V/div., Ch3: V_{SW} = 5 V/div., Ch4: I_{SW} = 750 mA/div., t = 0.5 µs / div.

Applications Information

Transformer Design

1. The transformer turns ratio, N, determines the output voltage:

$$N = N_S / N_P$$

$$V_{OUT} = 31.5 \times N - V_d \ ,$$

where 31.5 is the typical value of $V_{OUTTRIP}$, and V_d is the forward drop of the output diode.

2. The primary inductance, $L_{PRIMARY}$, determines the on-time of the switch:

$$t_{on} = (-L_{PRIMARY}/R) \times \ln(1 - I_{SWlim} \times R/V_{IN}) \ ,$$

where R is the total resistance in the primary current path (including $R_{SWDS(on)}$ and the DC resistance of the transformer).

If V_{IN} is much larger than $I_{SWlim} \times R$, then t_{on} can be approximated by:

$$t_{on} = I_{SWlim} \times L_{PRIMARY} / V_{IN} \ .$$

3. The secondary inductance, $L_{SECONDARY}$, determines the off-time of the switch. Given:

$$L_{SECONDARY}/L_{PRIMARY} = N \times N \text{ , then}$$

$$t_{off} = (I_{SWlim}/N) \times L_{SECONDARY}/V_{OUT}$$

$$= (I_{SWlim} \times L_{PRIMARY} \times N)/V_{OUT} \ .$$

The minimum pulse width for t_{off} determines what is the minimum $L_{PRIMARY}$ required for the transformer. For example, if ILIM = 1.5 A, N = 10, and V_{OUT} = 315 V, then $L_{PRIMARY}$ must be at least 4.2 µH in order to keep t_{off} at 200 ns or longer. These relationships are illustrated in figure 6.

In general, choosing a transformer with a larger $L_{PRIMARY}$ results in higher efficiency (because a larger $L_{PRIMARY}$ corresponds to a lower switch frequency and hence lower switching loss). But transformers with a larger $L_{PRIMARY}$ also require more windings and larger magnetic cores. Therefore, a trade-off must be made between transformer size and efficiency.

Leakage Inductance and Secondary Capacitance

The transformer design should minimize the leakage inductance to ensure the turn-off voltage spike at the SW node does not exceed the absolute maximum specification on the SW pin (refer to the Absolute Maximum Ratings table). An achievable minimum leakage inductance for this application, however, is usually compromised by an increase in parasitic capacitance. Furthermore, the transformer secondary capacitance should be minimized. Any secondary capacitance is multiplied by N^2 when reflected to the primary, leading to high initial current swings when the switch turns on, and to reduced efficiency.

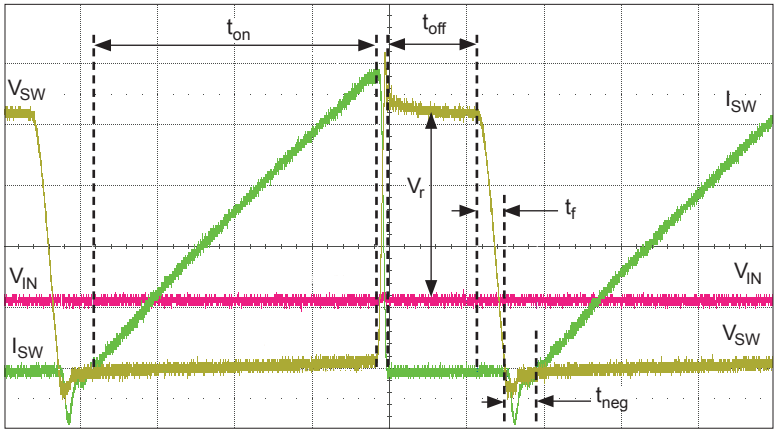


Figure 6. Transformer Selection Relationships

Input Capacitor Selection

Ceramic capacitors with X5R or X7R dielectrics are recommended for the input capacitor, C_{IN}. During initial Timer mode the device operates with 18 µs off-time. The resonant period caused by input filter inductor and capacitor should be at least 2 times greater or smaller than the 18 µs Timer period, to reduce input ripple current during this period. The typical input LC filter is shown in figure 7.

The resonant period is given by:

$$T_{res} = 2\,\pi\,(L \times C_{IN})^{1/2}\ .$$

The effects of input filter components are shown in figures 8, 9, and 10. It is recommended to use at least 10 µF / 6.3 V to decouple the battery input, VBAT , at the primary of the transformer. Decouple the VIN pin using 0.1 µF / 6.3 V bypass capacitor.

Output Diode Selection

Choose rectifying diodes, D1, to have small parasitic capacitance (short reverse recovery time) while satisfying the reverse voltage and forward current requirements. The peak reverse voltage of the diodes, V_{DPeak} , occurs when the internal MOSFET switch is closed. It can be calculated as:

$$V_{DPeak} = V_{OUT} + N \times V_{BAT}\,.$$

The peak current of the rectifying diode, I_{DPeak}, is calculated as:

$$I_{DPeak} = I_{PRIMARY\_Peak} / N\ .$$

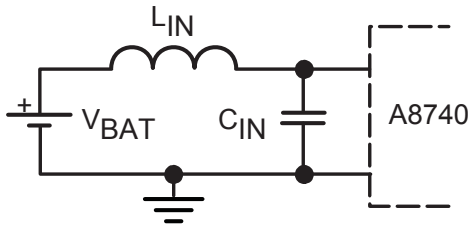


Figure 7. Typical input section with input inductance (inductance, L_{IN}, may be an input filter inductor or inductance due to long wires in test setup)

Effects of Input Filters

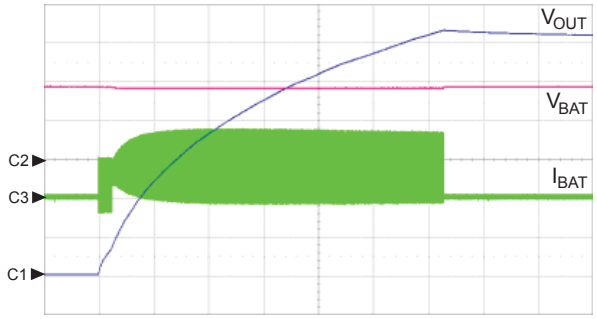


Figure 8. Input current waveforms with Li+ battery connected by 5-in. wire and decoupled by 4.7 µF capacitor, C_{OUT} = 100 µF, V_{IN} = V_{BAT} = 3.6 V, Ch1: V_{OUT} = 50 V/div, Ch2: V_{BAT} = 2 V/div, Ch3: I_{BAT} = 750 mA/div, t = 1 s/div

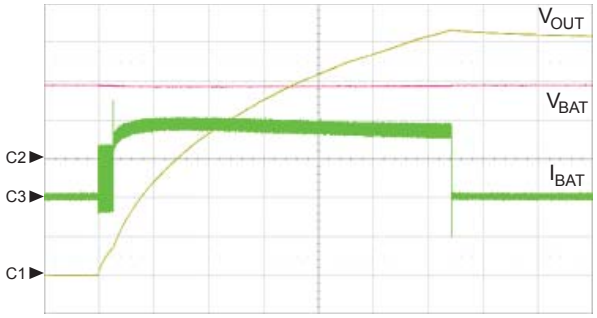


Figure 9. Input current waveforms with Li+ battery connected through 4.7 µH inductor and 4.7 µF capacitor, C_{OUT} = 100 µF, V_{IN} = V_{BAT} = 3.6 V, Ch1: V_{OUT} = 50 V/div, Ch2: V_{BAT} = 2 V/div, Ch3: I_{BAT} = 300 mA/div, t = 1 s/div

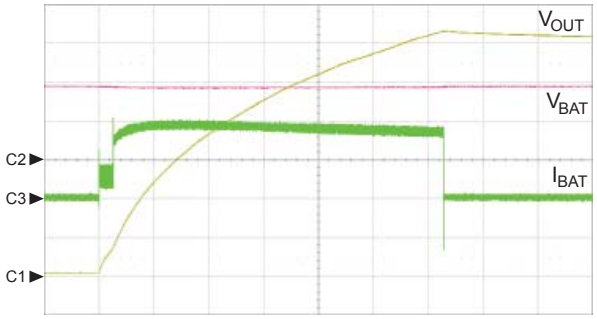


Figure 10. Input current waveforms with Li+ battery connected through 4.7 µH inductor and 10 µF capacitor, C_{OUT} = 100 µF, V_{IN} = V_{BAT} = 3.6 V, Ch1: V_{OUT} = 50 V/div, Ch2: V_{BAT} = 2 V/div, Ch3: I_{BAT} = 300 mA/div, t = 1 s/div

Layout Guidelines

Key to a good layout for the photoflash capacitor charger circuit is to keep the parasitics minimized on the power switch loop (transformer primary side) and the rectifier loop (secondary side). Use short, thick traces for connections to the transformer primary and SW pin. It is important that the $\overline{\text{DONE}}$ signal trace and other signal traces be routed away from the transformer and other switching traces, in order to minimize noise pickup. In addition, high voltage isolation rules must be followed carefully to avoid breakdown failure of the circuit board.

Avoid placing any ground plane area underneath the transformer secondary and diode, to minimize parasitic capacitance.

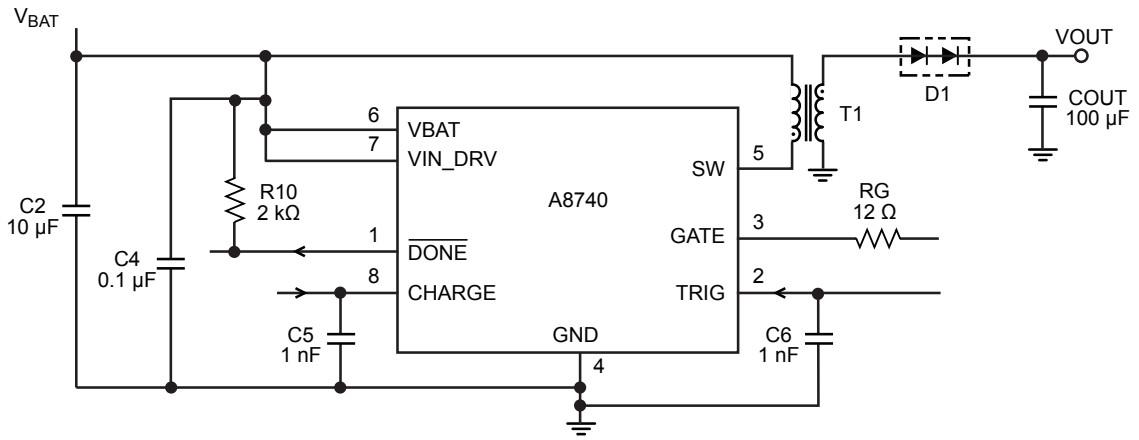
Connect the EE package PAD to the ground pad for better thermal performance. Use ground planes on the top and bottom layers below the IC and connect them through multiple thermal vias. Refer to the figures on page 18 for recommended layout.

Recommended Components

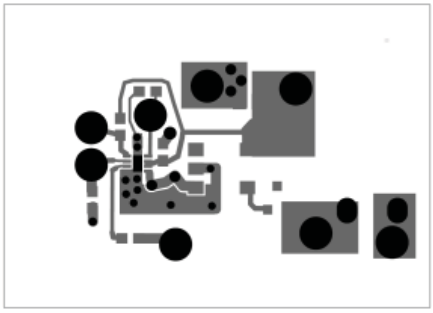
Component	Rating	Part Number	Source
C1, Input Capacitor	10 µF, ±10%, 6.3 V, X5R ceramic capacitor (0805)	JMK212BJ106K	Taiyo Yuden
C2	0.1 µF, 6.3 V X5R ceramic capacitor		
COUT, Photoflash Capacitor	100 µF / 330 V	EPH-31ELL101B131S	Chemi-Con
D1, Output Diode	2 x 250 V, 225 mA, 5 pF	BAV23S	Philips Semiconductor, Fairchild Semiconductor
T1, Transformer	$L_{PRIMARY}$ = 12.8 µH, N= 10.25, 6.5 × 8 × 4 mm	T-16-024A	Tokyo Coil Electric
	$L_{PRIMARY}$ = 6 µH, N= 10.4, 5.6 × 5.6 × 3 mm	LDT565630T-001	TDK

Recommended Layout

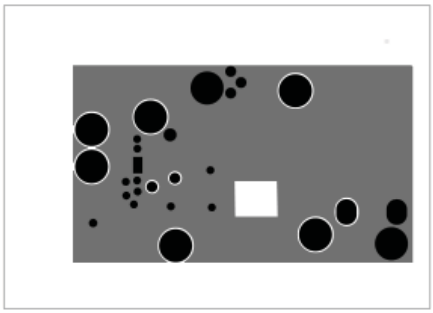
Schematic



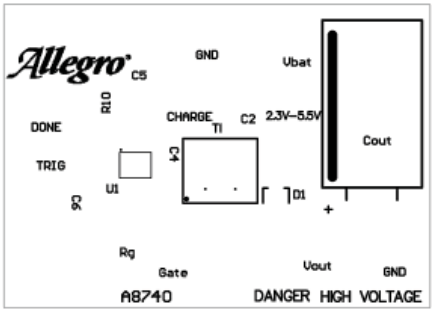
Top side



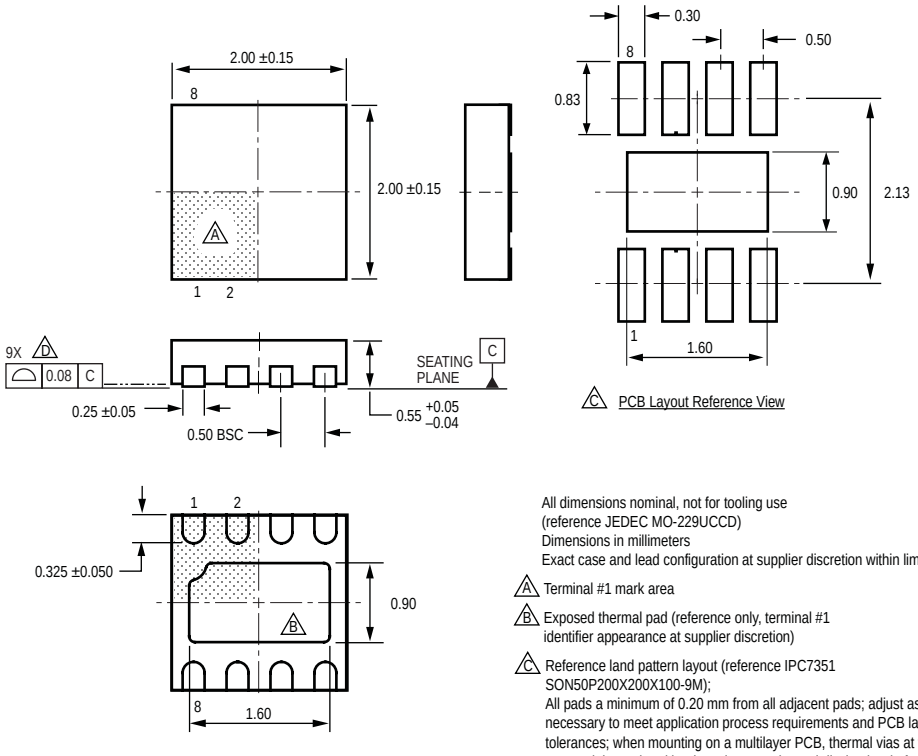
Bottom side



Top components



Package EE
8-Contact DFN with Exposed Thermal Pad



All dimensions nominal, not for tooling use
(reference JEDEC MO-229UCCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P200X200X100-9M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

For the latest version of this document, visit our website:

www.allegromicro.com